## Supporting Information

## Programmable, Electroforming-free TiO<sub>x</sub>/TaO<sub>x</sub> Heterojunction-based Non-volatile Memories

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**Figure S-1** | **a**, SEM image of arrays of memristor devices fabricated with  $TiO_x/TaO_x$  active layers of different junction sizes on a SiO<sub>2</sub>/Si substrate. **b**, SEM image (left) and EDX elemental maps (center, right) of a typical heterojunction memristor with a 5×5 µm<sup>2</sup> junction size. The  $TiO_x$  layer (green) was deposited on a Pt layer (purple) as the bottom electrode (horizontal I-bar) followed by the Pt layer (purple) as the top electrode (vertical I-bar), while the  $TaO_x$  layer (red) was sandwiched between the  $TiO_x$  and the bottom electrode.



**Figure S-2** Depth-profiling XPS spectra of **a**, C 1s and **b**, Pt 4f regions for the as-deposited 60nm-thick  $TaO_x$  film on a Pt film supported on a SiO<sub>2</sub>/Si substrate. The carbonaceous layer of the sample arising from ambient handling was removed after 5 s of sputtering, revealing a carbon free sample. The signal for Pt layer beneath the  $TaO_x$  layer is very weak because 300 s of Arsputtering was not sufficient to remove the  $TaO_x$  layer completely.



**Figure S-3** AFM image of the  $TaO_x$  film to illustrate the surface roughness for a scan area of  $5 \times 5 \ \mu m^2$ . The roughness analysis was performed along its diagonal direction and found to be 0.84 nm RMS.



**Figure S-4**| **a**, LRS current level vs compliance current. **b**, Retention characteristics for the  $TiO_x/TaO_x$  memristor (10×10 µm<sup>2</sup> junction size) at different read-out voltages. For different read

voltages, a very stable read current was observed even after long retention, which confirms the stability of these devices.



**Figure S-5** SET voltages of 300 memristor devices (marked by cell number) fabricated on the same chip. The similar switching voltages of these devices show the accuracy and reproducibility of our fabrication process.

**Table S1** Comparison of various memristor device architectures with single-layer and multilayer switching matrices and their respective electroforming and SET/RESET voltages. Our device out-performs all the devices based on not just single-layer switching matrices but also multilayer switching matrices. The device made by Bessonov et al. exhibits a lower SET/RESET voltage than our device but at the expense of a shorter lifetime (because of the oxidation-prone silver nanowire in ambient) along with a rather complex process.

Device Structure	Electroforming/	SET/RESET	Ref.
	Activation	Voltage	
	voltage		
Single-layer Matrix			
AFM Tip/SrTiO <sub>3</sub> /Pt-Au	-5 V	±4 V	Szot et al. (2006) <sup>[1]</sup>
Pt/TiO <sub>2</sub> /Pt	NA	2/3 V	Kwon et al. (2010) <sup>[2]</sup>
Pt/TiO <sub>2</sub> /Pt	-6 V	±0.6	Strachan et al. (2011) <sup>[3]</sup>
Pt/Ta <sub>2</sub> O <sub>5</sub> /Pt	-10 V	+0.6/-0.8 V	Strachan et al. (2011) <sup>[4]</sup>
Ti-Pt/TiO <sub>2</sub> /Au-pt	-14 V	+3/+2.5 V	Strukov et al. (2012) <sup>[5]</sup>
ZnO Nanorods	4 V	±2 V	Park et al. (2013) <sup>[6]</sup>
Pt/TiO <sub>2</sub> /Pt	-8 V	±4 V	Jiang et al. (2013) <sup>[7]</sup>
Pt/TiO <sub>2</sub> /Pt	Forming-free	+3.6/-4 V	Salaoru et al. (2013) <sup>[8]</sup>
Au NP/SrTiO <sub>3</sub> interface	10 V	+4/-6 V	Hou et al.(2014) <sup>[9]</sup>
$TaO_x$ , $HfO_x$ , $TiO_x$	-5 V	±2 V	Wedig et al. (2015) <sup>[10]</sup>
Ta2O5	+2-3.2 V	+0.45-0.65	Zaffora et al. (2017) <sup>[11]</sup>
TiO <sub>x</sub>	1.5 V	+0.6	Srivastava et al. (2017) <sup>[12]</sup>
Multilayer Matrix			
Pt/Ta <sub>2</sub> O <sub>5-x</sub> /TaO <sub>2-x</sub> /Pt	-3 V	-1/+2 V	Lee et al. (2011) <sup>[13]</sup>
Pt/TiO <sub>x</sub> /TiO <sub>y</sub> /TiO <sub>x</sub> /Pt	-10 V	±1.5 V	Bae et al. (2012) <sup>[14]</sup>
Pt/Ta <sub>2</sub> O <sub>5</sub> /HfO <sub>2-x</sub> /TiN	-10 V	±3-4 V	Yoon et al. (2014) <sup>[15]</sup>
Pd/Si:Ta <sub>2</sub> O <sub>5-x</sub> /TaO <sub>v</sub> /Pd	4-10 V	-1to -1.5 V	Kim et al. (2014) <sup>[16]</sup>
Pt/Nb-SrTiO <sub>3</sub> -Sm <sub>2</sub> O <sub>3</sub>	Forming-free	10 V	Lee et al. (2014) <sup>[17]</sup>
interface	_		
Pt/HfO <sub>2</sub> /Hf/Pt	2.5 V	±1.5 V	Breuer et al. (2015) <sup>[18]</sup>
Ag/MoO <sub>x</sub> /MoS <sub>2</sub> /Ag	Forming-free	±0.2 V	Bessonov et al. (2015) <sup>[19]</sup>
Ta/TaO <sub>x</sub> /TiO <sub>2</sub> /Ti	Forming-free	±6 V	Wang et al. (2015) <sup>[20]</sup>
Au/BaTiO <sub>3</sub> /NiO/Pt	+6 V	±1 V	Li et al. (2016) <sup>[21]</sup>
Pt/HfOx/HfO2/Pt	+3-10 V	+2-4 V	Cho et al. (2017) <sup>[22]</sup>
Pt/TiO <sub>x</sub> /TaO <sub>x</sub> /Pt	Forming-free	+0.5/-0.7 V	This work

**Table S2** Reduction in the magnitudes of SET ( $V_{SET}$ ) and RESET ( $V_{RESET}$ ) voltages with decreasing stopping voltages ( $V_{STOP}$ ).

V <sub>STOP</sub> (V)	V <sub>SET</sub> (V)	V <sub>RESET</sub> (V)
2.5	0.634	-2.315
2.0	0.574	-1.906
1.5	0.535	-1.548
1.0	0.512	-1.044
0.5	0.500	-0.732

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