Electronic Supplementary Information

Template-assisted vapour-liquid-solid growth of InP nanowires on (001) InP and Si substrates

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Template deposition

The Zn-doped *p*-type (001) InP substrates with resistivity less than 0.005 Ω-cm were coated with 520 nm of SiO_x by PECVD. Table 1 shows all relevant process parameters.

Table 1: Process parameters for SiO_x deposition using PECVD

Time (min)	N_2O flow (sccm)	Ar flow (sccm)	SiH_4 flow (sccm)	RF power (Watt)	ICP power (Watt)	Pressure (mTorr)	Temperature (˚C)
14	24	30	6	100	1000	15	200

The As-doped n-type (001) Si substrates with resistivities between 0.001-0.005 Ω-cm were coated with a 1 μm thick SiO_2 layer, thermally grown by wet oxidation.

The 25 nm thick SiN_x layer was deposited with PECVD using parameters shown in Table 2.

Table 2 Process parameters for SiN_x deposition

Time (s)	Ar flow (sccm)	NH_3 flow (sccm)	SiH_4 flow (sccm)	RF power (Watt)	ICP power (Watt)	Pressure (mTorr)	Temperature (˚C)
40	50	11.5	10	200	300	15	200

Template patterning

To prepare the Cr hard mask, wafers with a deposited oxide layer were first placed in a thermal evaporator to deposit 50 nm and 100 nm of Cr on InP and Si substrates, respectively. After Cr deposition the wafers were spin coated with the e-beam resist ARP 6200-15. A spin speed of 2000 rpm resulted in a coating thickness of 580 nm.

The wafers were subsequently transferred to a Voyager EBL system (Raith GmbH) and exposed with an acceleration voltage of 50 kV, an aperture size of 40 μm and a dose of 440 $\mu Ascm^{-2}$. The pattern was designed with a hole diameter of 80 nm. After exposure the openings widened to 100

nm. The exposed samples were developed in amyl acetate for 2 min followed by 20 sec of rinsing in isopropanol (IPA). Then the wafers were diced into 1x1 cm^2 chips using a Disco DAD 3320 automatic dicer.

Template etching

Cr etching

The Cr etching was done in an ICP-RIE process using an Oxford plasmalab system 100 equipment. A 6" sapphire wafer was used as a carrier during the etching. The sample was mounted on the carrier using a double-sided thermal tape manufactured by Nitto[1] in order to improve the thermal conduction between the sample and carrier to establish a uniform heat distribution in the sample. This tape also made the sample removal simple after the Cr etching by heating it to 150 °C for 1 min. The samples were etched using a (Cl_2 + O_2)-recipe with Cl_2 and O_2 flows of 20 sccm and 2 sccm, respectively. The RF and ICP powers were 10 W and 1000 W, respectively. The process pressure was set to 10 mTorr. This gives a Cr etch rate of 18 nm/min for our feature size. Based on this etch rate, we deliberately over-etched the samples by 20%.

Dry etching of SiO_x template on InP substrates

A 4" Si wafer was used as a carrier for the template etching with the sample mounted using the abovementioned conductive tape. The samples were etched using a (C_4F_8 + O_2)-recipe with C_4F_8 and O_2 flows of 30 sccm and 3.3 sccm, respectively. A process pressure of 6 mTorr was chosen and the RF and ICP powers were set to 250 W and 2000 W, respectively. The measured etch rate was 435 nm/min and we over-etched the samples by 5% based on this etch rate. Subsequently the Cr mask was removed by etching for 360 s using the abovementioned Cr etch recipe.

Dry etching of SiO_2 template on Si substrates

For Si substrates we avoided over-etching of the oxide template due to the poor Si/SiO_2 selectivity of the etching process. Instead, an HF dipping prior to the PED effectively removed any remaining oxide from the bottom of holes. After oxide etching the samples were first immersed into hot, 70 °C, EKC 265 for 30 min. and then moved to the Cr etch solution, Cr 18, for 3 min, followed by 3 min rinsing in flowing DI water.

Template seeding with Au particles

For the PED step, the 1x1 cm^2 samples were mounted on a cathode fabricated by Yamamoto. 160 ml of a pure 24K gold solution was poured into the designated container supplied with a platinum-plated titanium anode. The applied current pulse had a peak current density of 25.5 mA/cm^2, a frequency of 20 Hz and a duty cycle of 20%. For PED on Si substrates, the samples were first dipped into a 1:100 mixture of hydrofluoric acid (HF) and water for 5 minutes, followed by a 5 min rinsing step in 99.5 % ethanol. The deposition was completed after 180 and 160 cycles for InP and Si substrates, respectively. The illumination required for PED on *p*-type substrates was provided by a series of LEDs, emitting at 405 nm, embedded in a paddle moving back and forth in front of the cathode.

TA-VLS growth of axial InP/InAs NW heterostructures on (001) Si substrates

Growth of InP/InAs NW heterostructures on (001) Si is still under investigation. In an attempt to grow guided NWs where half of the NW comprised InAs and InP, respectively, we first annealed the sample at 800 °C for 10 min. in an AsH_3 ambient with a molar fraction of $\chi AsH_3 = 2.09\times10^{-3}$. Subsequently, the AsH_3 supply was turned off and a 20 s InP nucleation step was initiated by

introducing precursors with molar fractions of $\chi TMIn = 2.04\times10^{-6}$ and $\chi PH_3 = 2.47\times10^{-2}$ into the reactor. The sample was then cooled down to 420 °C in a PH_3/H_2 ambient. Subsequently, the intended InP section was grown for 5 min. using the above mentioned molar fractions of TMIn and PH_3. Then the supply of PH_3 was replaced by AsH_3 with a molar fraction of 2.09×10^{-3} and growth was carried out for another 5 min. Figure S1a shows a TEM image of a grown NW revealing a high density of stacking faults along the NWs. HRTEM confirmed that the NWs are grown along [001] with a ZB crystal structure (Figure S1b). Interestingly, no traces of InP were found as shown in Figure S1c.

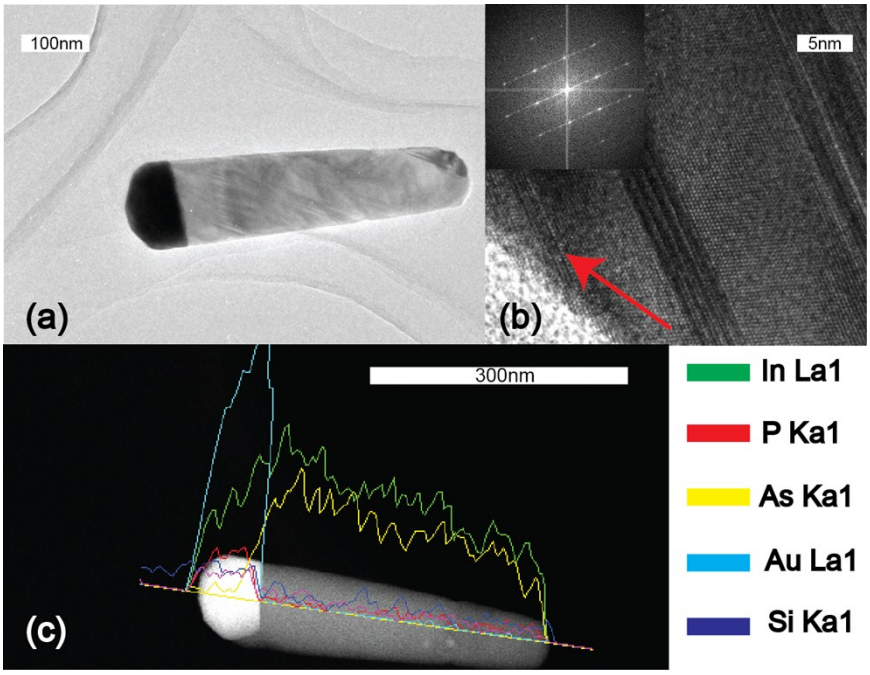

Figure S1: TEM study of NWs intended to comprise two segments of equal length of InP and InAs. a) TEM image of a NW showing a high density of defects along the NW. b) HRTEM of the NW showing a [001] crystal orientation. Twin defects are clearly resolved. c) STEM/EDS image of a NW with no observed traces of InP.

References

1 Thermal Release Sheet for Electronic Component Processing REVALPHA | Nitto in Europe, https://www.nitto.com/eu/en/products/group/e_parts/electronic/001/, (accessed August 29, 2019).