Supporting Information to

Facile 3D integration of Si nanowires on Bosch-etched sidewalls for stacked channel transistors

Ruijin Hu, Haiguang Ma, Han Yin, Jun Xu, Kunji Chen and Linwei Yu*

National Laboratory of Solid State Microstructures/School of Electronics Science and Engineering/Collaborative Innovation Center of Advanced Microstructures, Nanjing University, Nanjing, 210093, P. R. China.
Email: yulinwei@nju.edu.cn

Contents

Section 1 Structural characterizations of single silicon nanowire

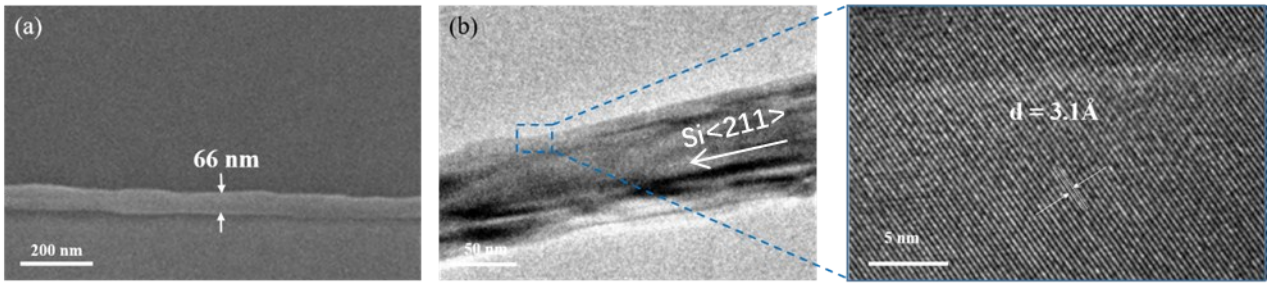

Fig. S1 (a) and (b) show, respectively, the scanning electron microscopy (SEM) image and the transmission electron microscopy (TEM) images of a selected single SiNW with a diameter of ~66 nm.