Room temperature single electron transistor based on a size-selected aluminium cluster: supplementary information

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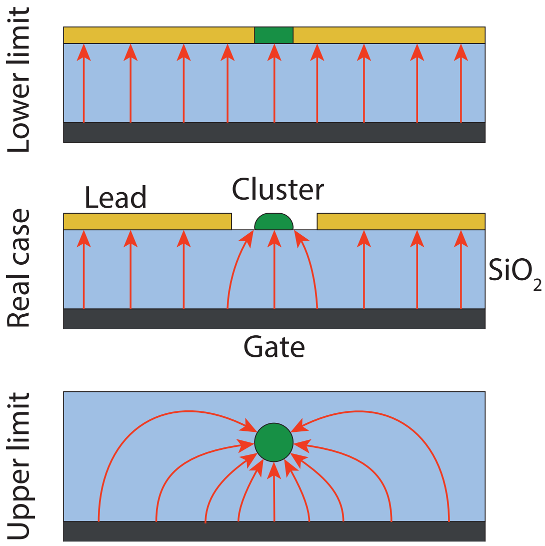

FIG. 1: Illustrations for the used models for cluster-gate capacitance estimation. The cluster-gate coupling increases from the upper sub-figure downwards. Red arrows stand for electric field lines when gate is positively charged in comparison to the cluster and the leads.

I. CAPACITANCE LIMITS

The capacitance between a deposited cluster and the backgate (C_G) heavily depends on electric field distribution between them. Partially shielding the electrostatic interaction between the cluster and the gate (see Figure 1b), metallic leads add up to the complexity of the C_G estimation. The lower limit of C_G can be obtained when the leads are enlarged to cover the whole plane as it is presented in the Figure 1a. As $U_{SD} \ll U_G$ and the cluster is much stronger coupled to the leads than to the gate, the electric field distribution is similar to the geometry of the flat capacitor. In this case C_G is calculated from the flat capacitor formula, assuming the plate area to be equal to the cluster footprint on the substrate. Using the earlier estimated island size in Sec.III, $C_{Gmin} = 8 \times 10^{-22}\,$F. The upper limit of C_G is estimated assuming the cluster is not shielded by the leads (see Figure 1c). This substantially increases the electrostatic interaction between them and makes the electric field distribution rather complicated. Thus, the upper limit is calculated using an approximated formula of an unshielded sphere in a medium over a conductive plane [1, 2]: $C_{Gmax} = 2\pi\epsilon d \cdot (1 + 0.5 \log(1 + d/(2h))) = 3 \times 10^{-19}\,$F, where $\epsilon = 3.7\epsilon_0$ is a dielectric permittivity of silica.

[1] J. Crowley, Proceedings of the Electrochemical Society of America Annual Meeting on Electrostatics , Paper D1, pp 1 (2008).

[2] S. Banerjee, S. J. McCarty, and E. F. Nelsen, in *Proc. 2015 ESA Annu. Meeting Electrostatics* (2015).

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