Electronic Supplementary Material (ESI) for Sustainable Energy & Fuels.
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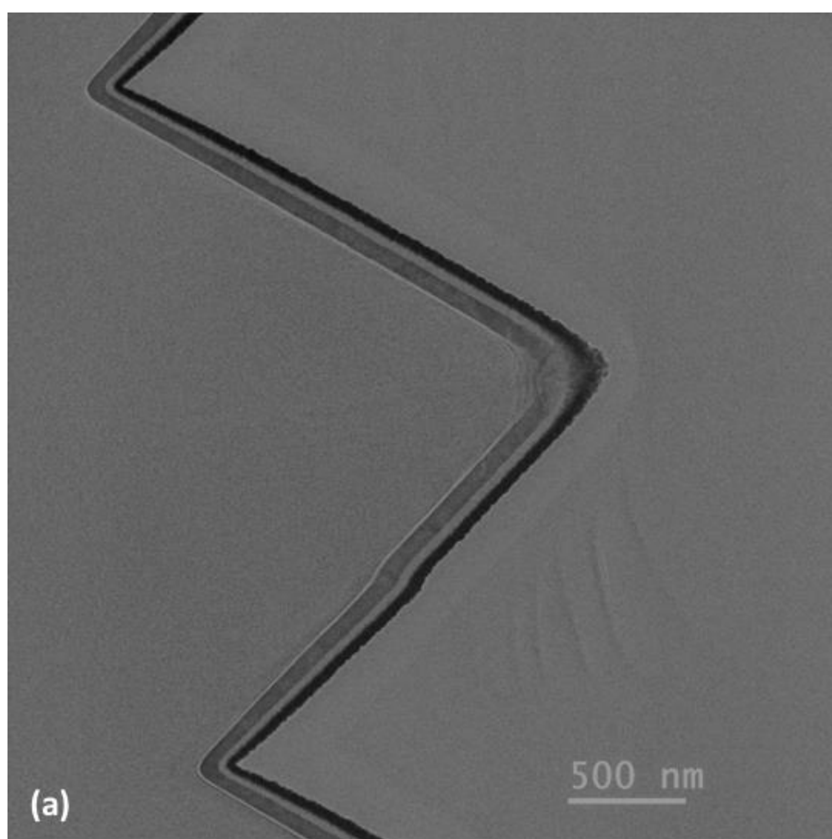
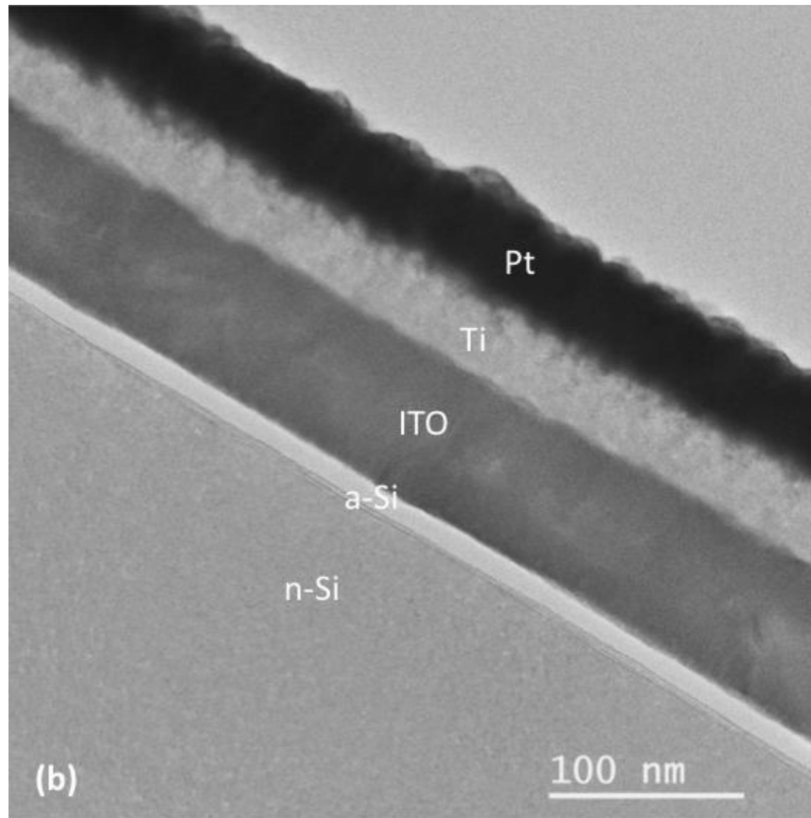
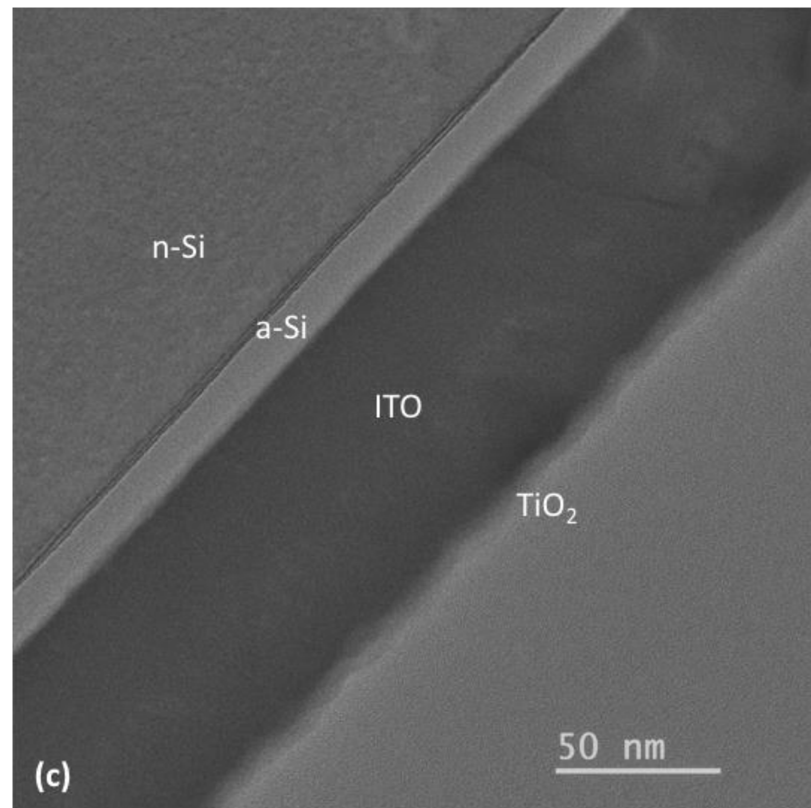
Supplementary Information

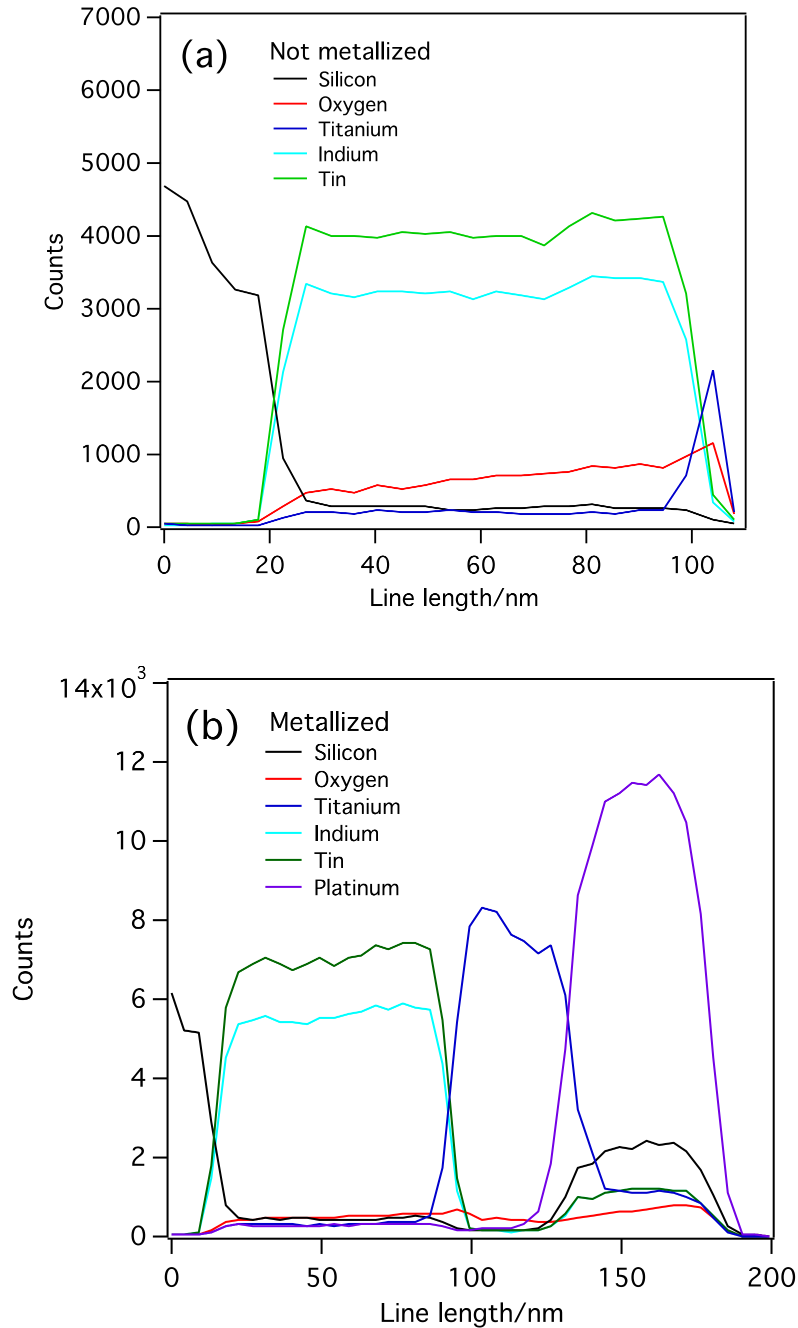
S1 – (a) Cross section TEM image of one of the cones of the silicon HIT cell device with ALD TiO_2 layer and Ti/Pt metallization; (b) high-resolution TEM image depicting the layers of the device; (c) a high-resolution TEM image of one device without metallization to better show the amorphous ALD TiO_2 on top of the ITO.



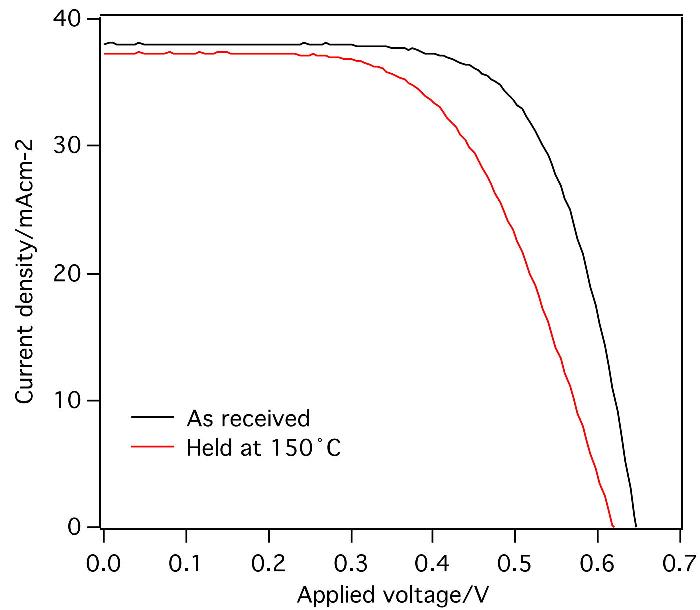

Pt
Ti
ITO
a-Si
n-Si
(b)
100 nm


n-Si
a-Si
ITO
TiO_2
(c)
50 nm

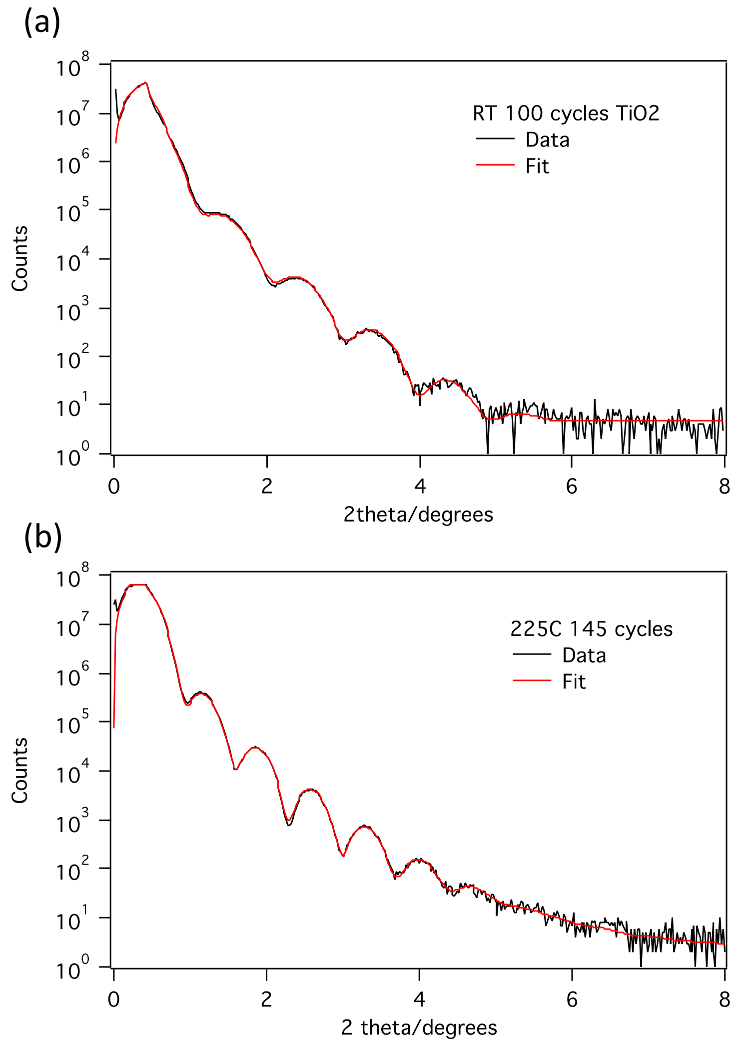
S2 – Energy dispersive x-ray spectroscopy (EDS) line scans for (a) non-metallized device and (b) metallized device, starting from the n-Si bulk region. In both cases there is about 80 nm of ITO TCO layer on top of the silicon. The non-metallized device shows a thin layer of TiO_2 on the surface, while the metallized sample shows the 50 nm of Ti and 50 nm Pt deposited on top.



S3 - I-V data for an as-received HIT cell compared to one that was held at 150°C in the ALD chamber for 20 hours prior to measurement shows performance degradation even without any deposition, proving that the cell degradation was due to the temperature and not the TiO_2.

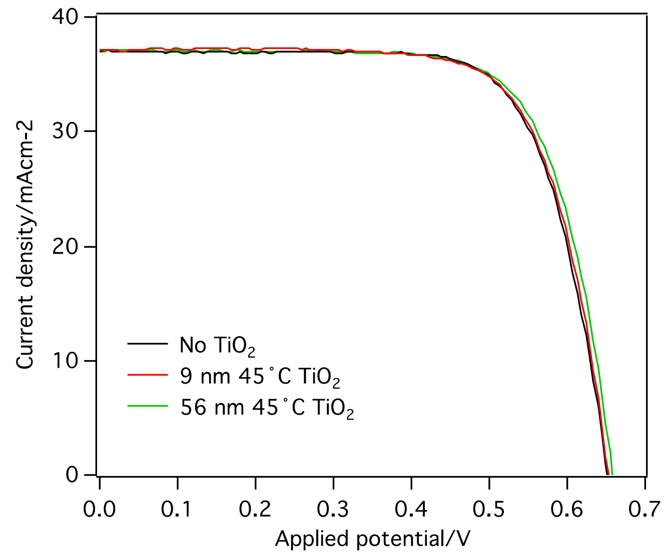


S4 – Measured data and fitted XRR spectrum for (a) 100 cycles of TiO_2 deposited at 45 °C, (b) 145 cycles of TiO_2 deposited at 150 on n^+Si (100) wafer, showing a higher growth per cycle number and lower density for the film deposited at lower temperature.

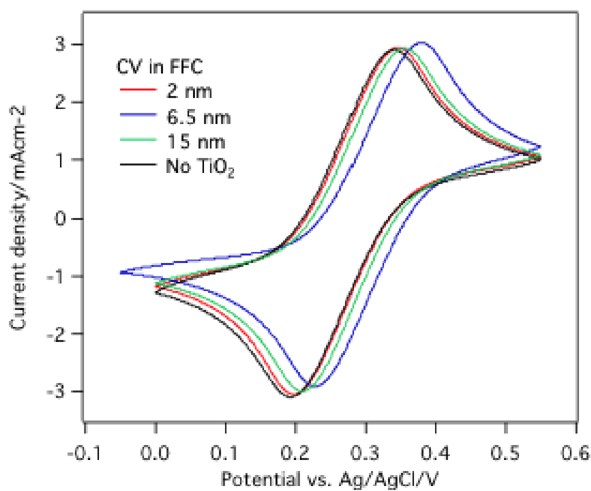


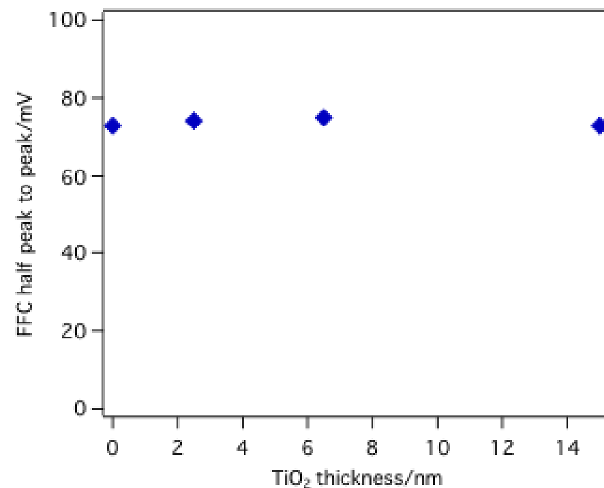
ALD TiO_2 film	Fitted TiO_2 density/gcm^{-3}	Fitted TiO_2 thickness/nm	Growth rate/Å$cycle^{-1}$
45 °C 100 cycles	3.77	8.96	0.9
150 °C 145 cycles	3.92	12.03	0.83

S5 – I-V data for a HIT cell with no ALD TiO_2 (black) and a HIT cell with a 9 nm (red) and 56 nm (green) ALD TiO_2 layer deposited at 45° C, with 50 nm Ti/Pt metal deposited on top, showing that samples with varying ALD TiO_2 thicknesses have identical photovoltaic performances.

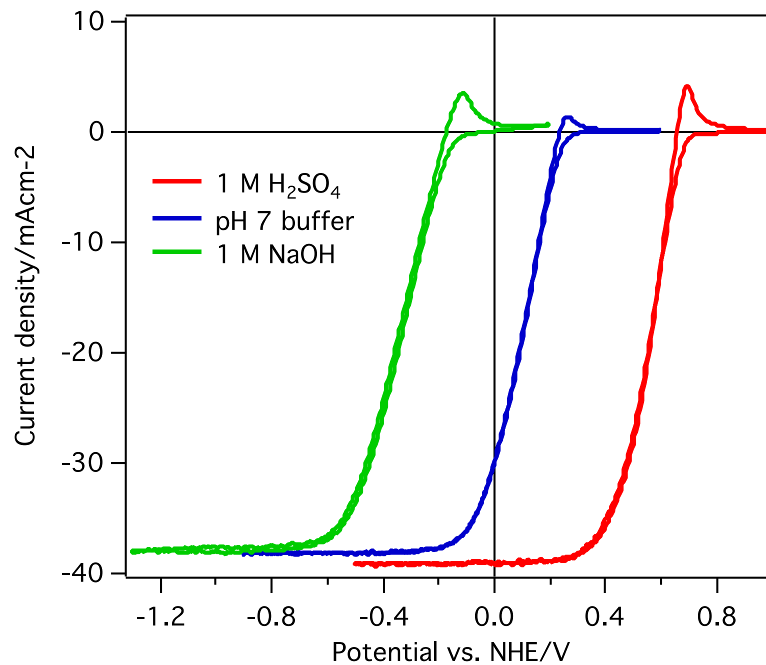


S6 – Degenerately-doped n-type silicon wafers with resistivity of 0.001 – 0.005 ohmcm^{-2} were purchased from University Wafer. The native SiO_2 thickness was measured by ellipsometry to be about 2.0 nm. TiO_2 of thicknesses 2.5 nm, 6.0 nm and 15 nm were deposited using ALD. In addition, an n$^+$Si sample that did not undergo ALD was included. All the samples were metallized with 50 nm of Ti and 50 nm of Pt at the top, while 100 nm of Al was deposited at the back to form an ohmic contact. Metallization was done by e-beam evaporation. Cyclic voltammetry in 10 mM ferri/ferrocyanide (10mM $K_3Fe(CN)_6$, 10mM $K_4Fe(CN)_6$, and 1M KCl) shows similar half peak-to-peak splitting of between 73 to 75 mV for all 4 samples, proving that the addition of the ALD TiO_2 layer does not produce much of a barrier to the flow of electrons from the n$^+$Si due to the good alignment between the valence bands of the Si and the TiO_2.

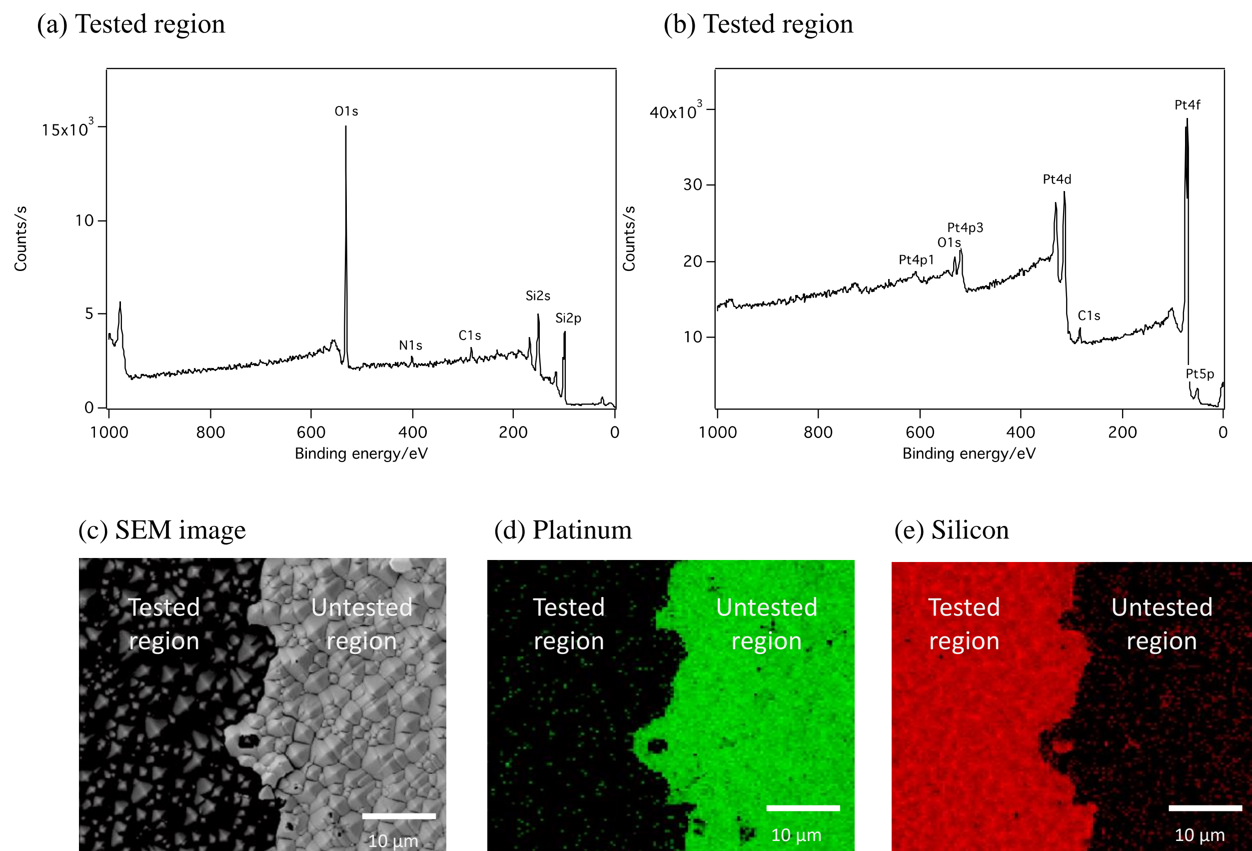




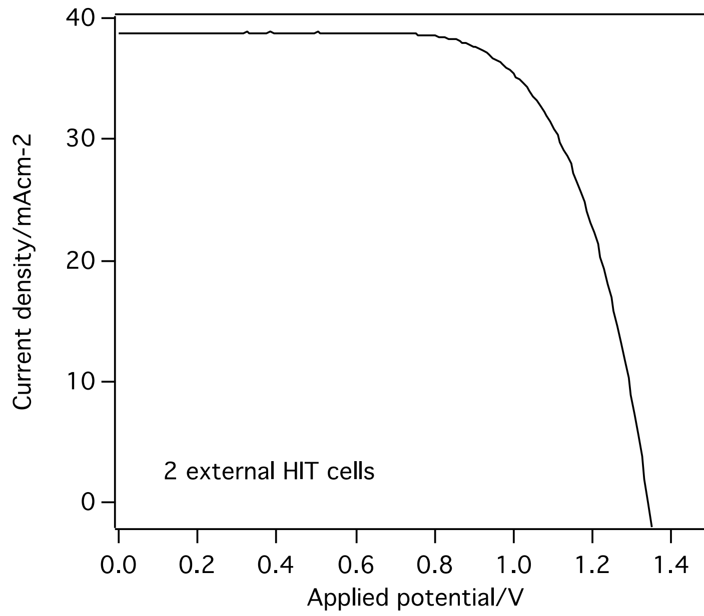
S7 – ALD TiO_2-protected Si HIT photocathode under 1 sun illumination in 1 M H_2SO_4 (pH 0), phosphate buffer (pH 7) , as well as 1 M NaOH (pH 14). These CV scans were taken with a three-electrode set up with an Ag/AgCl reference electrode.



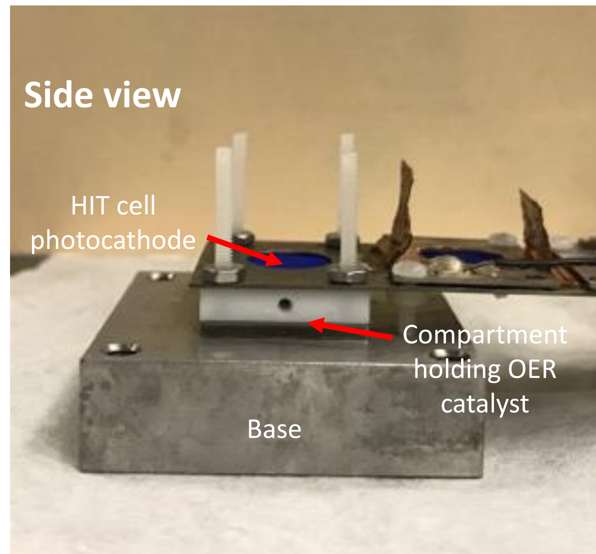
S8 – XPS survey scans of the tested (figure 3a) shows no presence of any the Pt catalyst, with only the underlying silicon detected along with adventitious carbon, oxygen, and nitrogen, unlike an untested region (figure 3b) which shows strong Pt peaks. Auger mapping (figure 3c-e) done on the edge of the tested region confirms that only silicon is left in the tested region.



S9 – Solid state current-voltage plots for 2 external HIT cells used to provide additional photovoltage for unassisted water splitting.

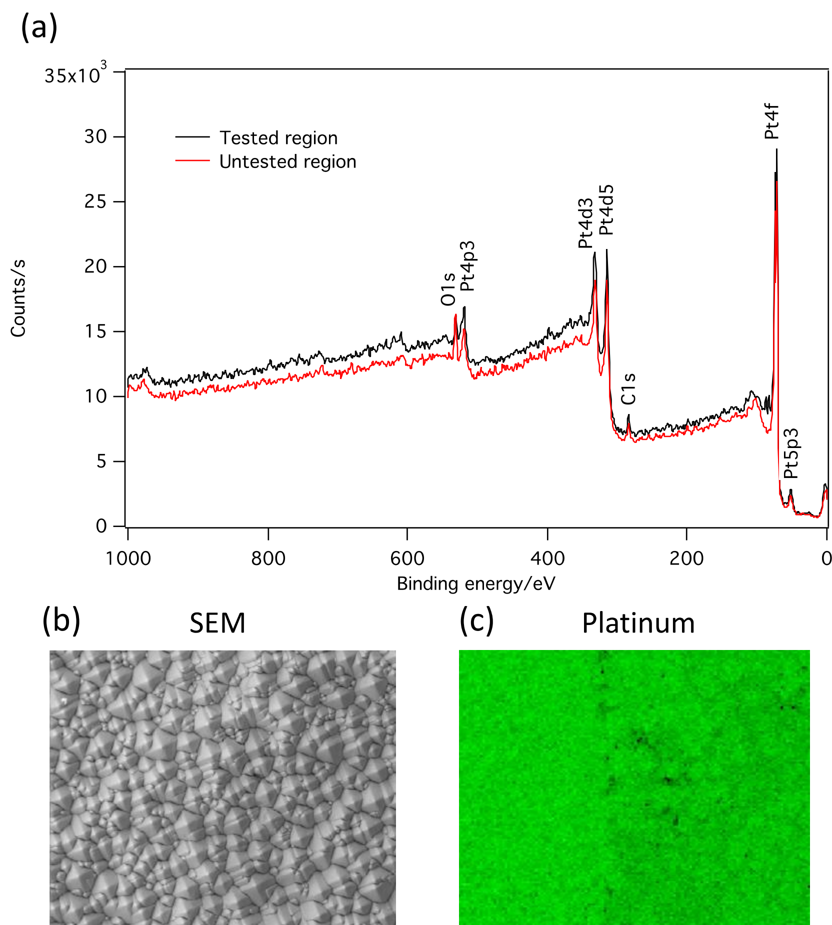


S10 – Top and side-view photographs of the flow cell structure. The three HIT cells are assembled side-by-side and electrically connect with alligator clips during operation. One of the HIT cells sits above a Teflon flow cell in which the electrolyte flows through, and the system is pressure-sealed.

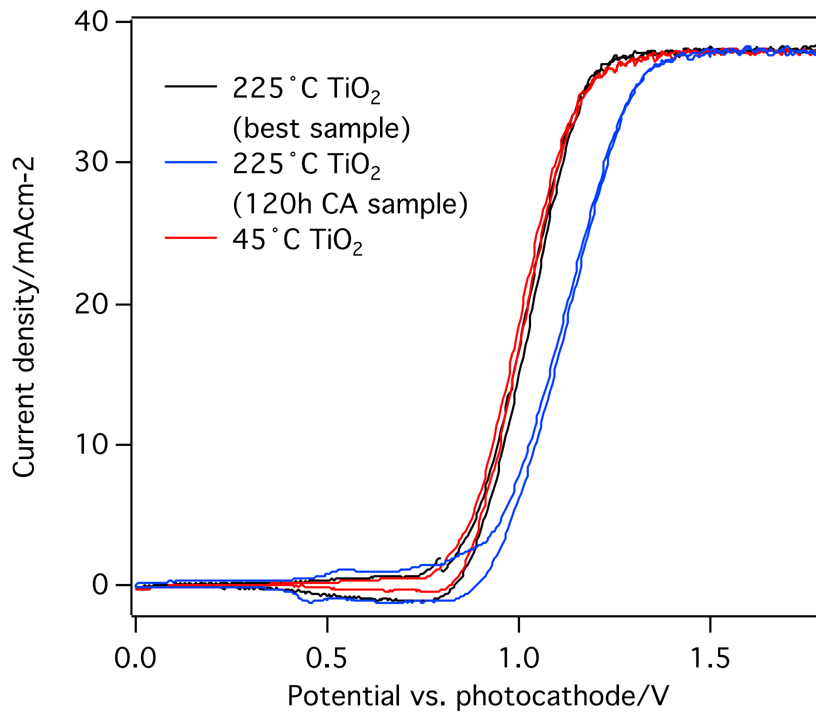


S11 – Resistance correction is done by conducting electrochemical impedence spectroscopy under open circuit conditions. From the resulting Nyquist plot we extract the solution resistance from the high frequency intercept for the real impedance, and subtract it from the overall potential using the equation $V_{corrected} = V_{uncorrected} - R_s$ x current where R_s is the solution resistance extracted. Impedence spectra is collected between 1 MHz and 10 mHz, and the solution resistance for the 1 M H_2SO_4 electrolyte is typically 2-3 ohms.

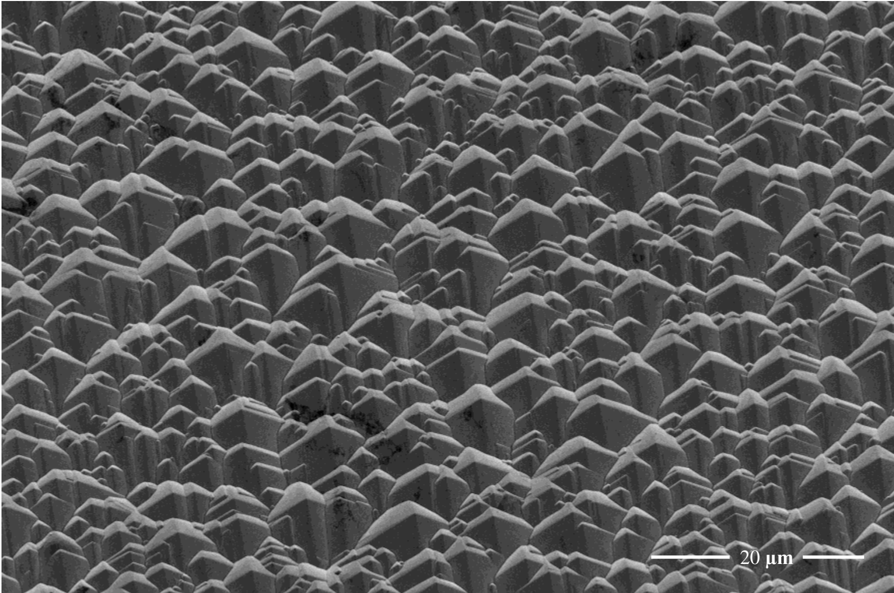
S12 – (a) XPS survey scans of the tested sample in both the tested region and untested region show the presence of the Pt HER catalyst and adventitious carbon and oxygen; (b) SEM image of the boundary between the tested and untested region showing no discernable change in the morphology after 120 hours of testing; (c) Auger mapping confirming little change in the Pt coverage in the tested and untested regions.

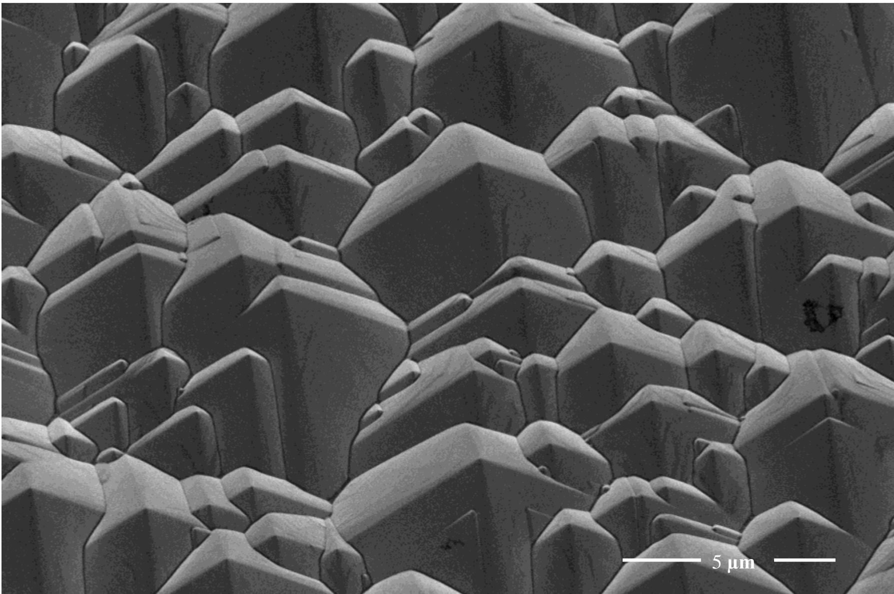


S13 – The best performing HIT cell with ALD TiO_2 deposited at 150° C shows similar water splitting performance as a typical 45° C deposited HIT cell (these are tested with just a single HIT cell with an IrOx on porous Ti OER catalyst).

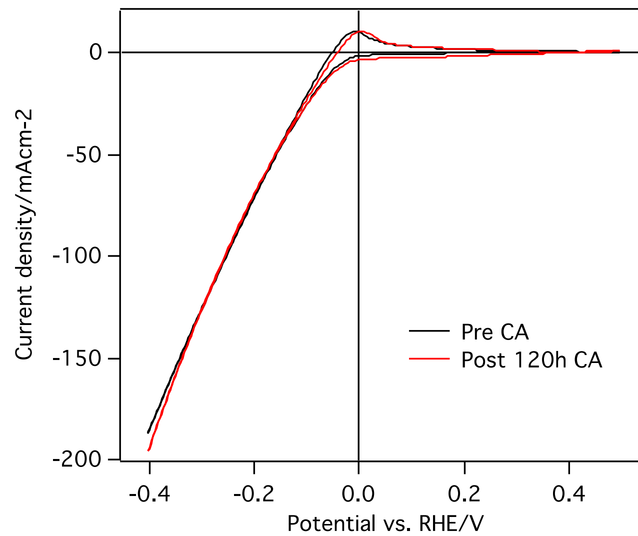


S14 – SEM image of as-received Si HIT cell taken at a 30° tilt showing the surface roughness is on the micrometer scale.

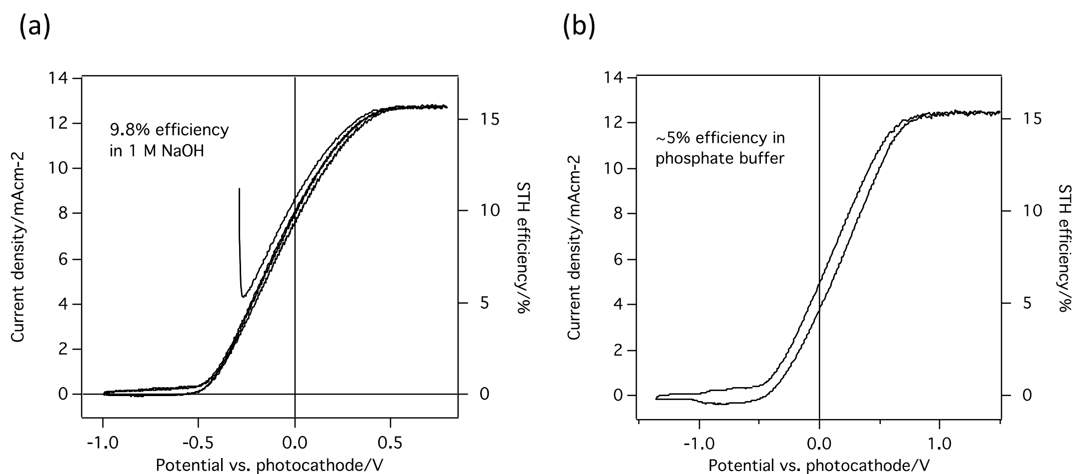




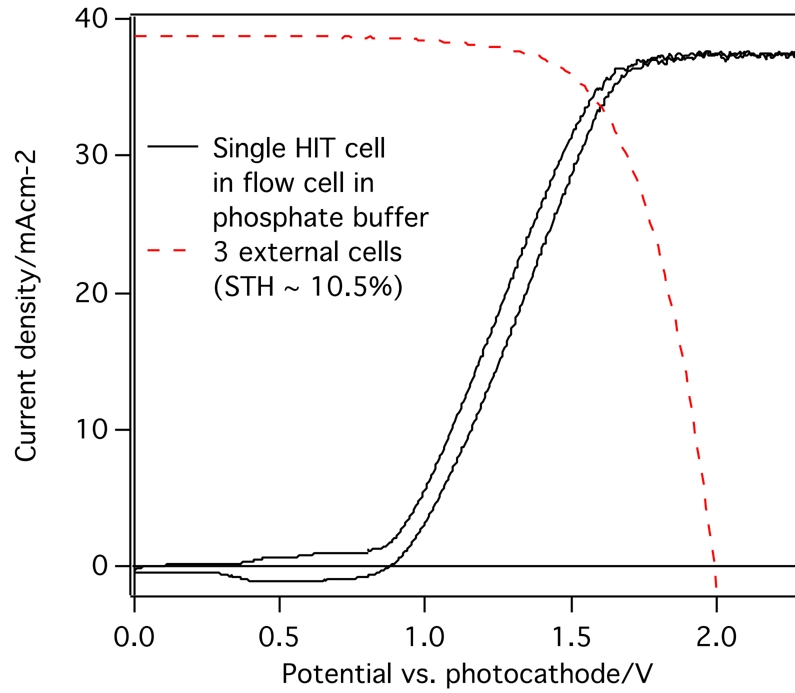
S15 – Cyclic voltammetry scan of 100 nm Al/n^+Si/10 nm TiO_2/50 nm Ti/50 nm Pt sample in 1 M H_2SO_4 before any testing and after 120 hours of chronoamperometry at -0.15V vs. RHE applied potential. In the absence of a ITO layer there is no observable degradation in the HER performance after 120 hours of continuous operation.



S16 - J-V curve for triple cell device in a two-electrode configuration tested in 1 M NaOH and pH 7 phosphate buffer electrolyte, showing a lower STH efficiency of 9.8% and about 5% respectively without any resistance correction owing to the lower activity of the IrO_x catalyst in base and phosphate buffer, and to the higher solution resistance of the buffer solution.



S17 – CV scan of a single HIT cell with IrO_x on Ti OER catalyst in phosphate buffer solution and solid-state IV curve from 3 external HIT cells. The point where the curves intersect indicate a STH efficiency of 10.5%.



S18 - Sunpreme combines Hybrid Cell Technology (HCT) with proven processes from the microelectronics industry to develop a simplified toolset and process for copper metallization on bifacial Si heterojunction cells. The result yields over 24% efficiency with a production ready process using standard production n-type Cz c-Si wafers (large area cell 244.3cm2). Thin film a-Si:H layers are deposited by plasma enhanced chemical vapor deposition (PECVD) on both sides of an n-type Cz c-Si substrate, thus realizing the solar cell emitter and the back surface field layer of the solar cell. Due to the comparatively low conductivity of doped a-Si:H, the use of transparent, conductive layers (TCO) on top of the a-Si:H films is required as both a conductive and antireflective layer. The cell starts from grid patterning through Cu electrochemical plating to achieve 20um width and 30um height fingers. All Cu metallization process and equipment use optimized PCB industry standard concepts to handle thin, fragile silicon wafers in high volume manufacturing.