About Degradation and Regeneration Mechanisms of NiO Protective Layers Deposited by ALD on Photoanodes

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Supporting Information



Fig. S. 1: p^+n -Si photoanode, where a 0.5 cm² active area (darker region) was lithographically defined by SiO₂ passivation on a silicon n-type wafer (0.1-0.5 ohm.cm resistivity), ALD-protected and further Ag paint soldered to a Cu wire and isolated with thermoplastic.



Fig S. 2: transmittance measurements of NiO layers grown at 100 (black), 200 (red) and 300 °C (blue) on top of glass substrates.

<u>V vs RHE</u>	<u>R1 / Ohm</u>	<u>R2 / Ohm</u>	<u>C2/F</u>	<u>R3 / Ohm</u>	$\underline{CPE3} \cdot \underline{T} / \underline{F} \cdot \underline{S}^{A3-1}$	<u>A3</u>
1.1	2.293	426.9	1.40E-06	<i>3.01E+18</i>	1.01E-04	0.83
1.2	2.229	428.9	1.39E-06	5.10E+11	1.38E-04	0.83
1.3	2.093	419.1	1.38E-06	7244	<i>4.89E-04</i>	0.76
1.4	2.407	430.1	1.37E-06	<i>6.46E</i> +11	<i>4.43E-04</i>	0.87
1.5	2.054	430.5	1.36E-06	6104	<i>3.11E-04</i>	0.88
1.6	2.13	371.1	1.35E-06	447.9	2.74E-04	0.83
1.7	2.223	246.1	1.32E-06	179.2	2.39E-04	0.82
1.8	2.366	144.7	1.25E-06	97.5	1.93E-04	0.85
1.9	1.822	82.2	1.19E-06	56.59	2.05E-04	0.85

Table S. 1: EIS fitted values of Fig. 6a using the modelled circuit presented in Fig. 6a (inset).



Fig. S. 3: EIS measurements of a Ni Foil and a protected p^+ -Si with 100 °C NiO by ALD at similar current values and thus, at different potential using the modelled circuit presented in Fig. 6a (inset). Results are presented in Table S. 2.

<u>t / h</u>	<u>R1 / Ohm</u>	<u>R2 / Ohm</u>	<u>C2/F</u>	<u>R3 / Ohm</u>	<u>CPE3-T / F·S⁴³⁻¹</u>	<u>A3</u>
Ni Foil	2.15	0	0	26.04	8.92E-04	0.89
100 °C NiO p+-						
Si	2.99	41.96	1.16E-06	18.9	3.80E-04	0.78

Table S. 2: EIS fitted values of Fig. S. 3 using the modelled circuit presented in Fig. 6a (inset).

<u>t / h</u>	<u>R1 / Ohm</u>	<u>R2 / Ohm</u>	<u>C2/F</u>	<u>R3 / Ohm</u>	$\underline{CPE3-T/F\cdot S^{A3-1}}$	<u>A3</u>
0	2.9	41.9	1.16E-06	18.9	<i>3.80E-04</i>	0.78
1	3.6	52.8	1.16E-06	36.3	2.63E-04	0.78
3	3.5	54.3	1.14E-06	35.8	2.48E-04	0.79
6	3.6	55.2	1.14E-06	35.7	2.51E-04	0.79
9	3.8	57.1	1.13E-06	35.3	2.36E-04	0.80
12	3.6	55.7	1.16E-06	34.3	2.46E-04	0.80
15	4.0	59.7	1.12E-06	37.1	2.41E-04	0.79
18	3.5	57.7	1.18E-06	35.8	2.56E-04	0.78
21	3.7	56.8	1.14E-06	33.8	2.40E-04	0.79
24	3.8	56.1	1.13E-06	32.8	2.45E-04	0.79

Table S. 3: EIS fitted values of Fig. 6c using the modelled circuit presented in Fig. 6a (inset).



Fig. S. 4: Stability measurement of the same sample represented in Fig. 6b in a logarithmic time scale and the correspondent fitting of the measured values, polarized at 1.9 V vs RHE in 1 M KOH.



Fig. S. 5: selected spots where the EDX measurements presented in Table S.1 were performed.

Spectrum 2		Spectrum 3			
Element	Weight%	Atomic%	Element	Weight%	Atomic%
СК	15.84	28.17	СК	30.38	48.55
ОК	15.34	20.49	O K	8.57	10.28
F K	7.06	7.94	F K	1.73	1.75
Al K	0.29	0.23	Al K	0.00	0.00
Si K	52.31	39.79	Si K	56.13	38.36
S K	0.14	0.10	S K	0.08	0.05
Ni K	9.01	3.28	Ni K	3.12	1.02
Totals	100.00		Totals	100.00	

Table S. 4: EDX quantifications of spots selected in Fig. S. 5, presenting significant extra Ni and O where bumps are visible by SEM.



Fig. S. 6: SEM images of NiO layers grown on top of Si at deposition temperatures of 200 °C (left) and 300 °C (right) after 100 cycles between 1.1 and 2 V vs RHE in 1 M KOH electrolyte in dark conditions. No morphology changes can be seen.



Fig. S. 7: p^+n -Si photoanode protected with NiO deposited at 100 °C and measured under 1 sun illumination in 1 M KOH. red) 1000 h stability measurement at 1.7 V vs RHE cycled 6 times every 12, 48 or 3h. black) measured current density at more anodic potential (1.8 V vs RHE), where the current density is limited by the number of minority carriers photogenerated in the p-n junction.



Fig. S. 8: a) SEM top view image of the n^+p -Si photoanode NiO protected at 100 °C presenting very few etched regions. Zoom in two of the etching regions, where b) a few tens of nanometers hole can be seen and c) a particle is present, both probable fabrication defects of the NiO layer allowing KOH to etch the silicon beneath