Electronic Supplementary Material (ESI) for Journal of Materials Chemistry C.
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Supporting Information

High Performance Multilevel Photonic Memory Based on Vertical Organic Filed Effect Transistor with Ultrashort Channel Length

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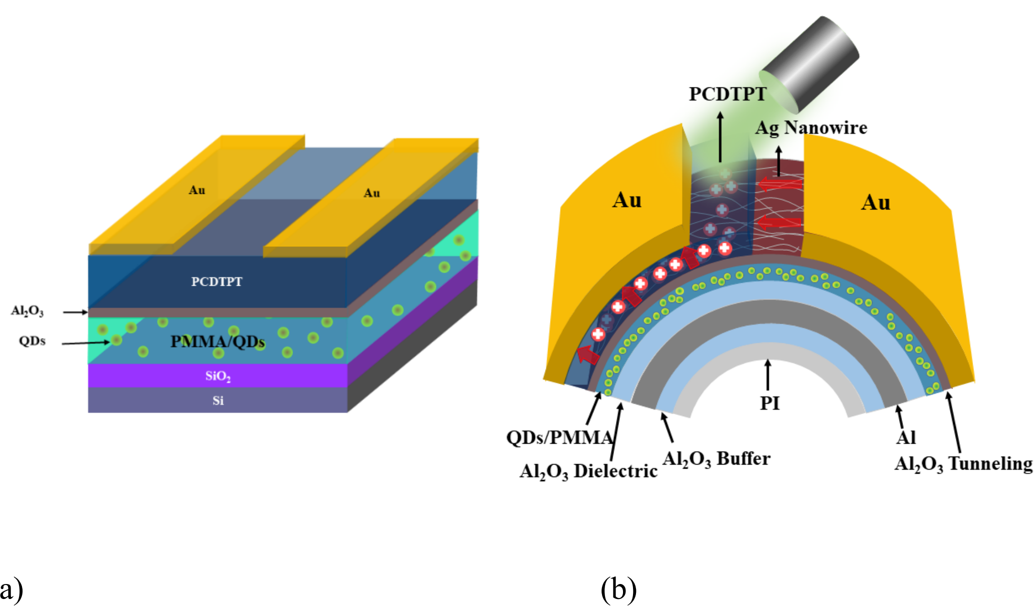

(a) (b)

Figure S1. Schematic diagram of the (a) planar photo memory device and (b)flexible vertical memory device.

Device Fabrication

Fabrication process of flexible vertical memory device

For the preparation of flexible memory device, the glass was used as bottom substrate and PI solution was deposited onto the glass substrate by blade coating with a blade gap of 100um. The substrate temperature and blade velocity were maintained at 50 °C and 10 mm/s. Subsequently the obtained film was annealed at 80 °C for 12 h, 120 °C for 1 h, 180 °C for 1 h, 250 °C for 1 h and 300 °C for 0.5 h inside a vacuum oven successively. Then 100 nm Al_2O_3 was deposited on the top of PI as the buffer layer by ALD. The bottom Al gate electrode was prepared by thermal evaporation followed by deposition of 100 nm Al_2O_3 as a blocking dielectric layer with the same ALD process conditions described above. The deposition of PMMA/QDs, Al_2O_3 tunneling layer, AgNws, PCDTPT, and the source and drain electrodes were following the same process as the rigid device as mentioned above. Figure S2 showed the fabrication flow for a rigid multilevel non-volatile photo memory device.

Fabrication process of vertical optical memory array

To obtain the regular memory array, PCDTPT (4mg/mL), which was dissolved in chloroform with 20 vol % 2-chlorophenol, were performed by inkjet-printing on a piezoelectric inkjet printing system (MicroFab, Jetlab II) with a nozzle diameter of 60 µm. The volume, velocity, the substrate condition and angle deviation of in-flight drops were controlled by optical module. The deposition of the droplets was controlled by varying the driving voltage, printing speed, droplet size, and substrate temperature.

Driving voltage of 80 V and frequency of 1000 Hz with a 200 pL droplet size and substrate temperature at 60 °C was applied to obtain a uniform deposition of PCDTPT layer. The Ag ink droplet ejection was performed by a driving voltage of 40 V and a frequency of 1000 Hz with a 150 pL droplet size at room temperature.

Fabrication process of planar optical memory devices

The structure of planar optical memory device was Si/SiO_2/PMMA/QDs/PCDTPT/Au source–drain. A heavily p-doped Si with a 100 nm thick thermally grown SiO_2 was used as the gate electrode and blocking dielectric layer. Subsequently, the PMMA/QDs solution was spin-coated onto the SiO_2 blocking dielectric layer to form a charge-trapping layer. A 4 nm Al_2O_3 tunneling layer was formed on the floating-gate layer by atomic layer deposition (ALD) under deposition temperature of 200°C. Drain and source electrodes were deposited by thermal evaporation through a shadow mask with channel length and width defined as 30 μm and 1000 μm, respectively.

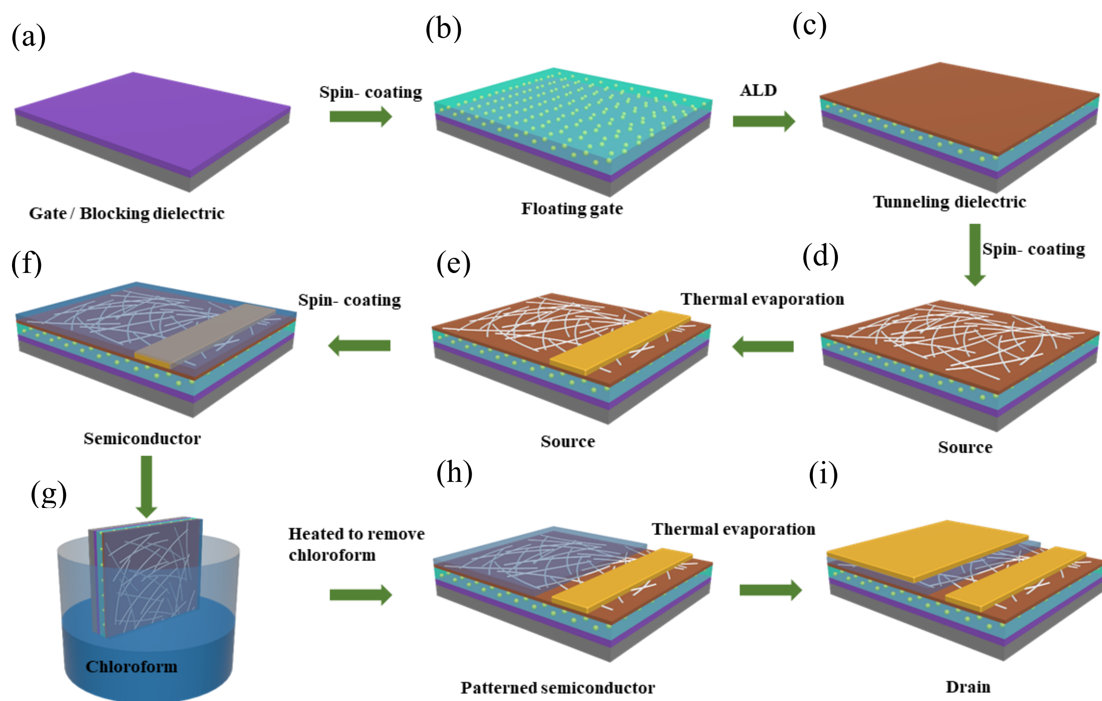

Figure S2. Schematic illustration of the fabrication flow for a rigid vertical photo memory device (a) and (b) spin coating of PMMA/QDs solution on the SiO_2, (c) deposition of Al_2O_3 tunneling layer by atomic layer deposition (ALD), (d) spin coating of AgNws to form mesh source, (e) deposition of gold electrode by thermal evaporation using a sophisticated shadow mask, (f) spin coating of PCDTPT, (g)partially immersed the device in the chloroform solvent by a dip method to pattern organic semiconductor layer, (h) patterned organic semiconductor, (i) thermally evaporated gold as drain electrode.