Electronic Supplementary Material (ESI) for Journal of Materials Chemistry C.

Bilayered $BaSnO_3$ thin film transistors on silicon substrates

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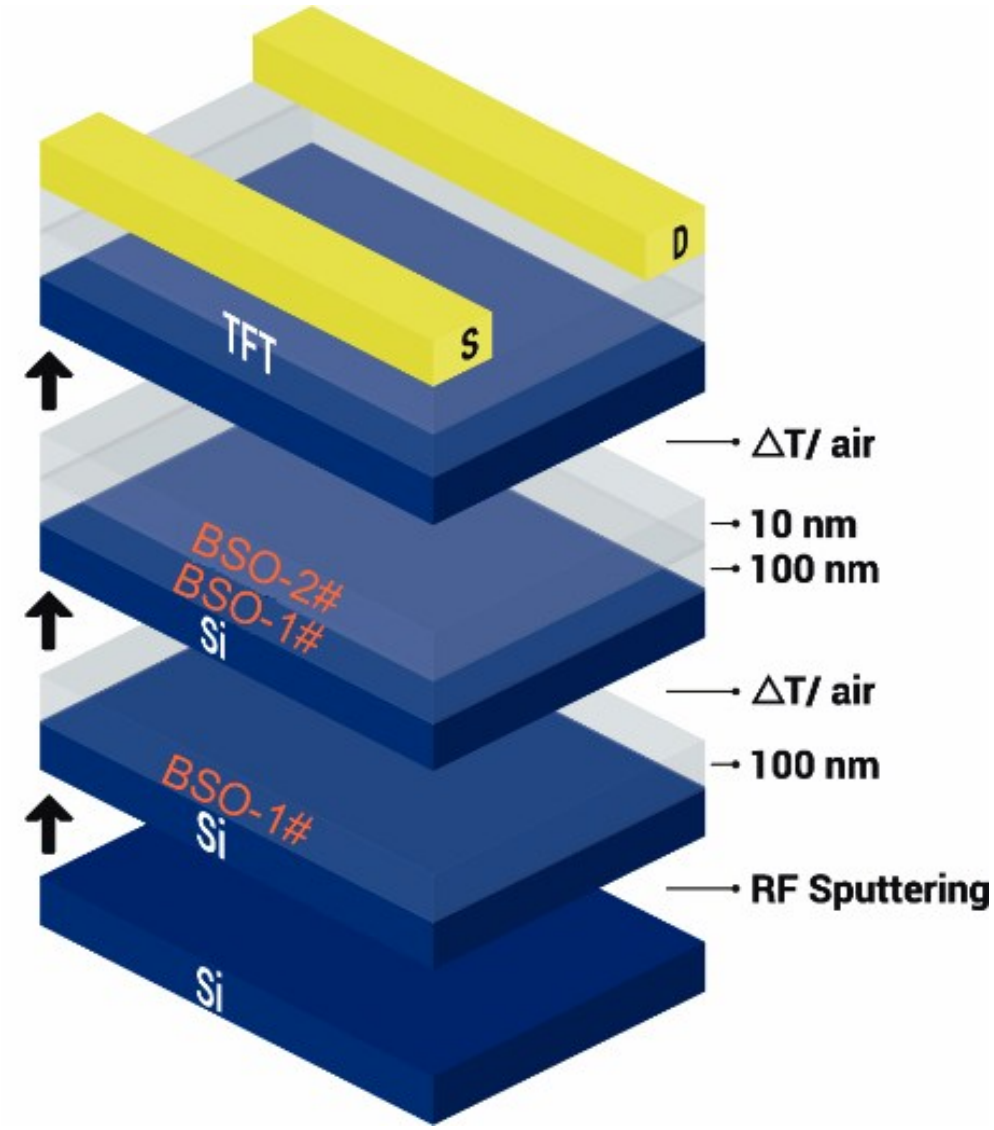

Figure S1. A diagram shows the preparation process for BSO TFTs.

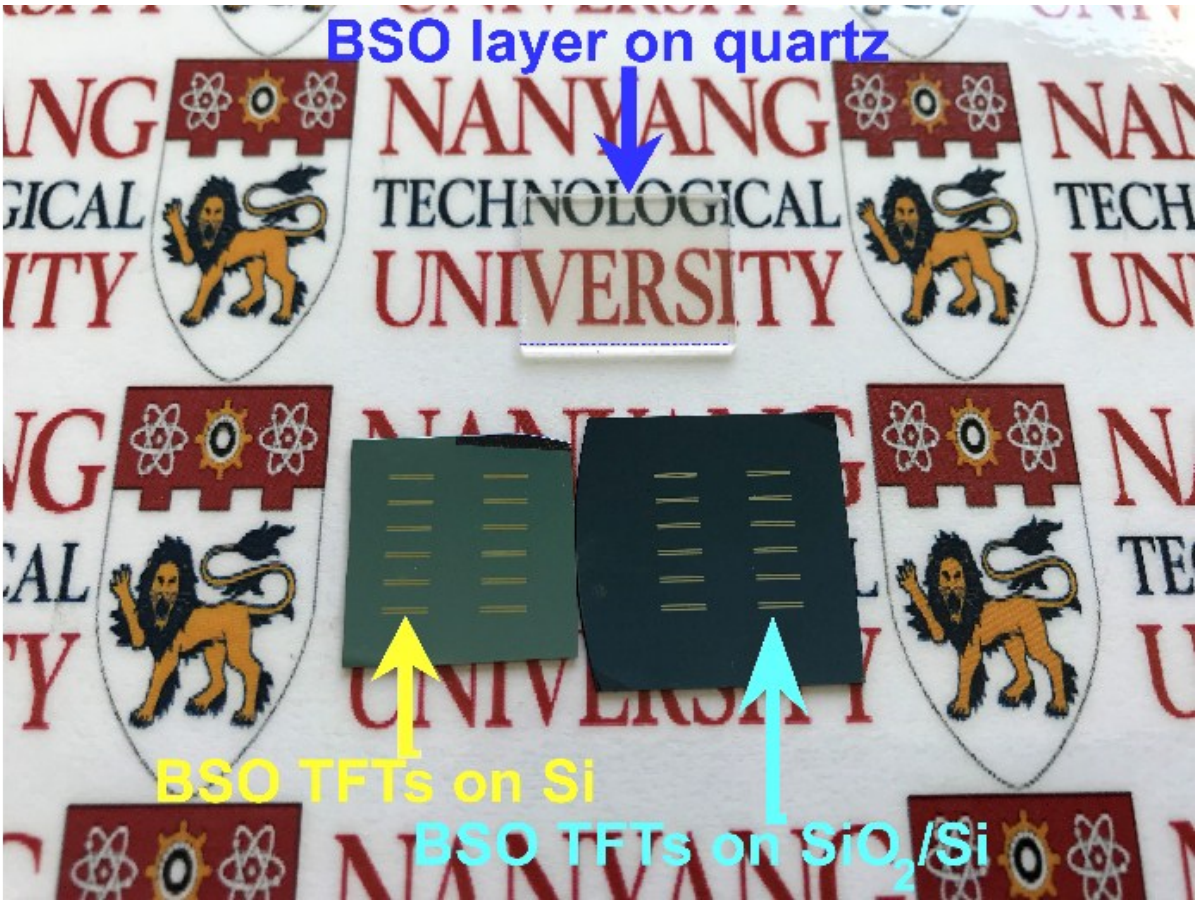

Figure S2. A picture shows the BSO TFTs on silicon and SiO_2/Si substrates.

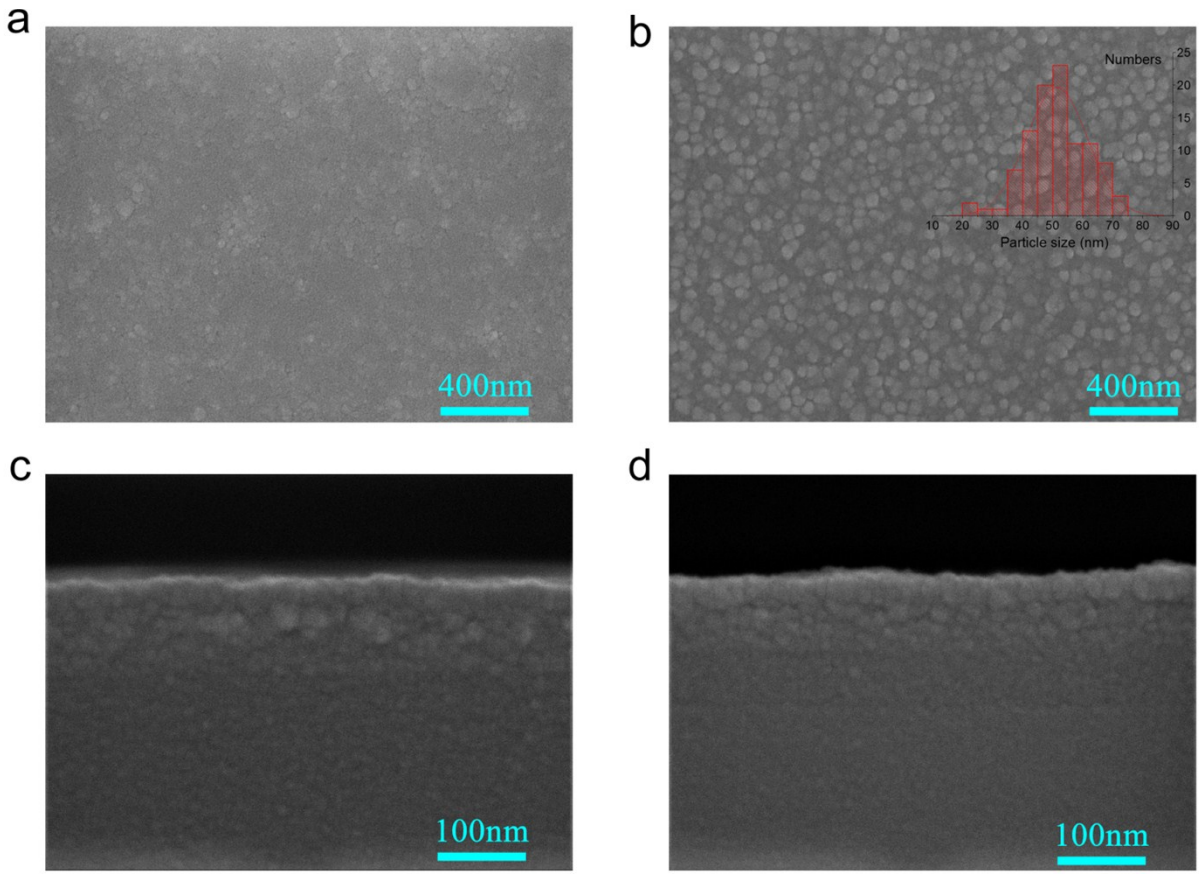

Figure S3. SEM images of $BaSnO_3$ thin films deposited with a RF power of 50W and annealed in ambient air for 1 hour at 1000℃. Surface morphology of BSO thin films deposited on (a) Si and (b) SiO_2/Si substrates. Cross-sectional images of BSO thin films on (c) Si and (d) SiO_2 (100 nm, thermal oxidation)/Si.

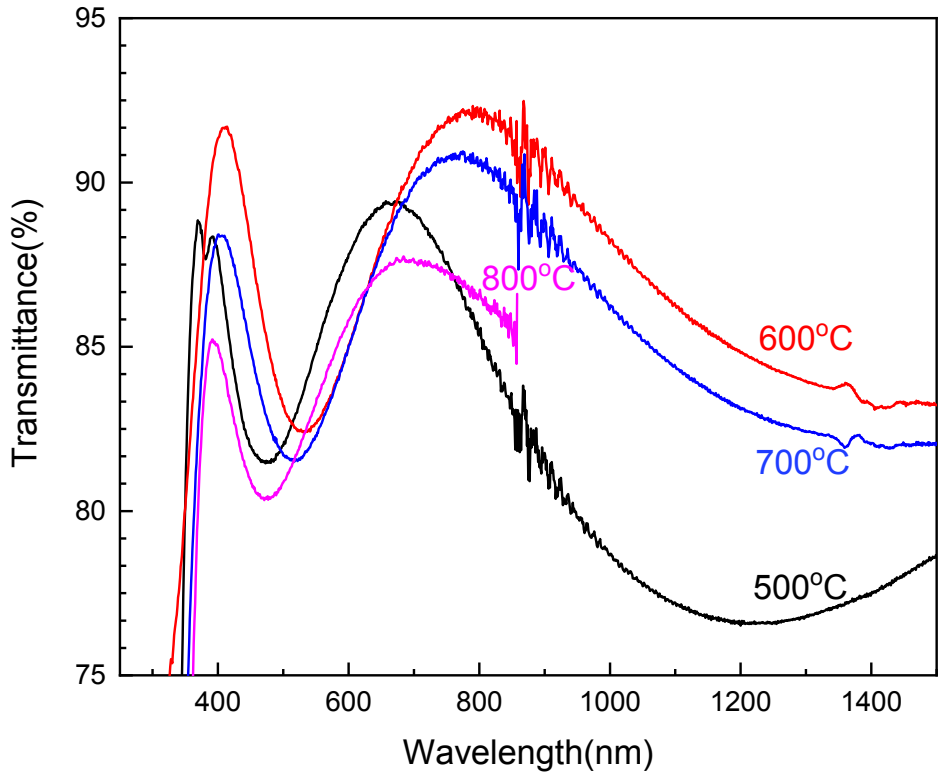

Figure S4. The transmittance curves of 75W-BSO(100nm) samples on B-Si glass with wavelength changed between 250nm and 1500nm, the annealing temperature are changed from 500°C to 800°C .

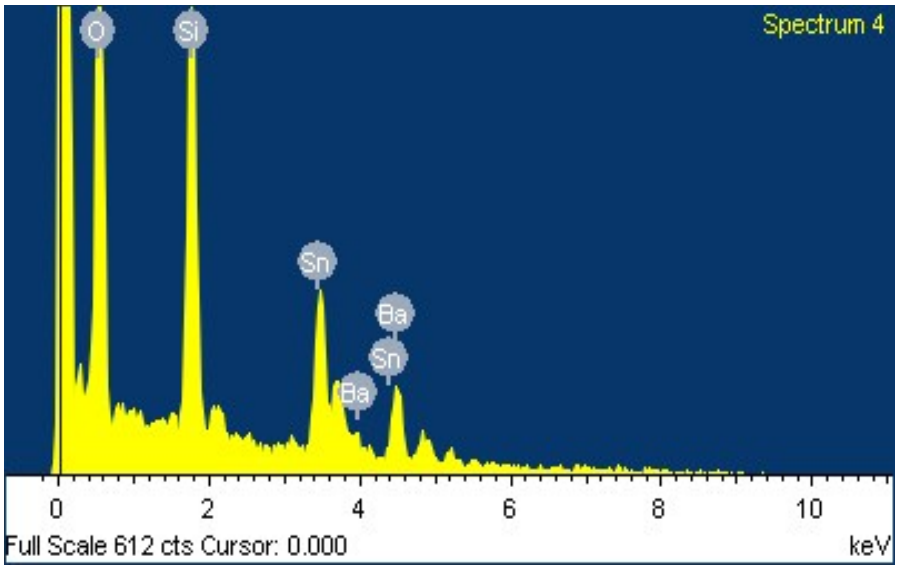

Figure S5. Typical EDX spectrum of 75 W sputtered BSO thin film on silicon substrate

Table TS1. EDX data summary of BSO thin films with high and low power

Sputter power	O K (Atomic%)	Si K (Atomic%)	Sn L (Atomic%)	Ba L (Atomic%)	Total (Atomic%)
75W	67.96	16.04	8.69	7.31	100
50W	18.15	77.68	0.91	0.76	100

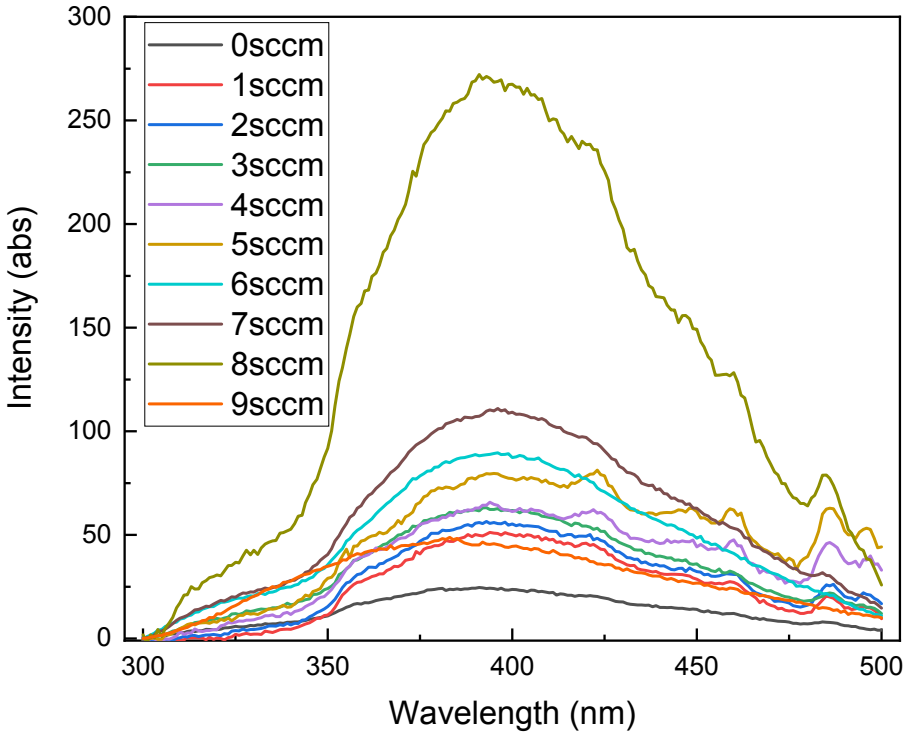

Figure S6. The PL spectrum of BSO samples on Boron-silicon glass with thickness of 100nm prepared at different oxygen content at room temperature, the sputtering power is 50W, and all the process pressure is kept at 3.0mTorr. The annealing temperature of these BSO samples are 700°C in air condition, and the annealing time is 1h for all the samples.

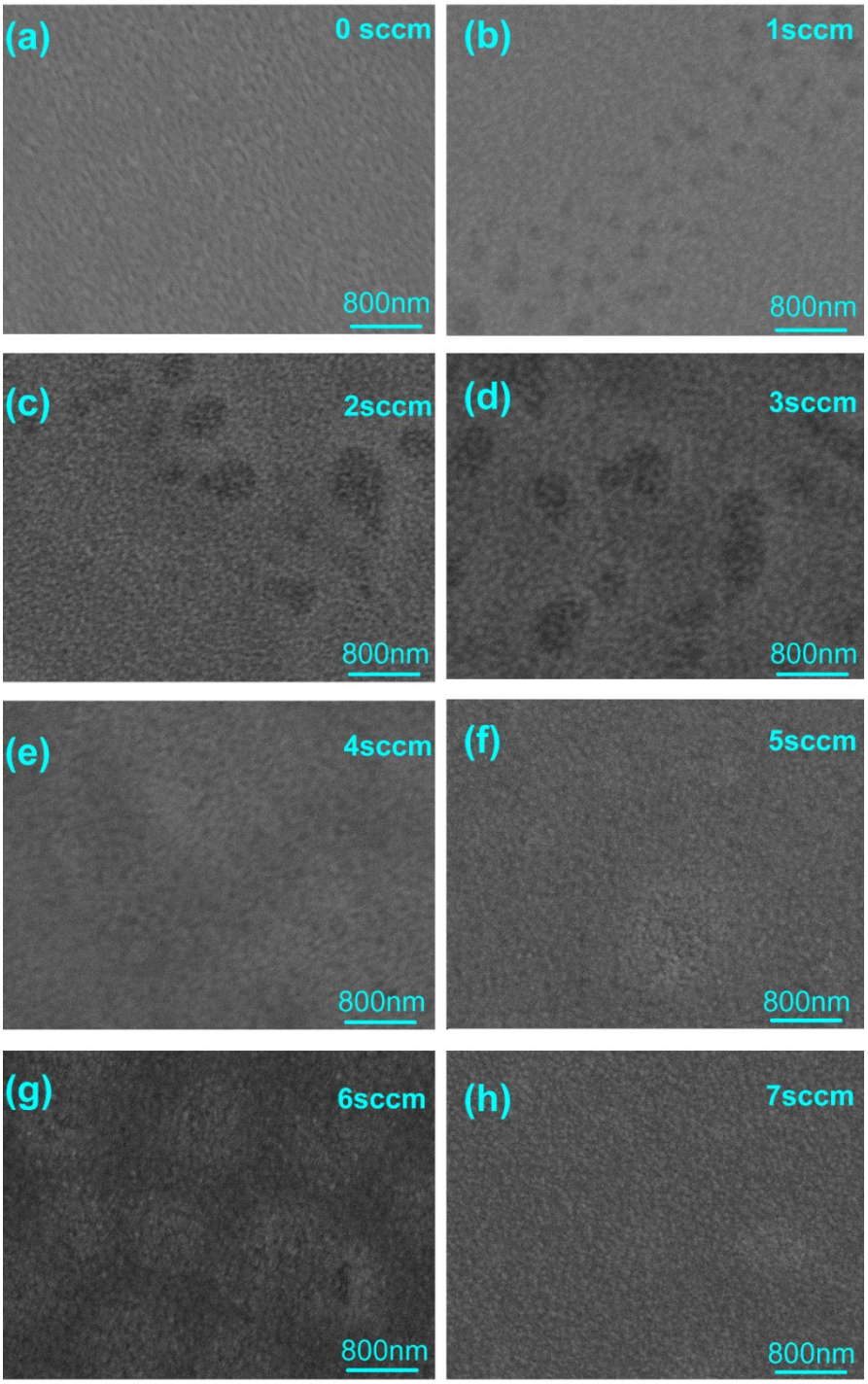

Figure S7. a series SEM images of 100nm-BSO thin films on silicon substrate with different O2 partial during preparation process, and the air annealing temperature of all the films is 850°C.

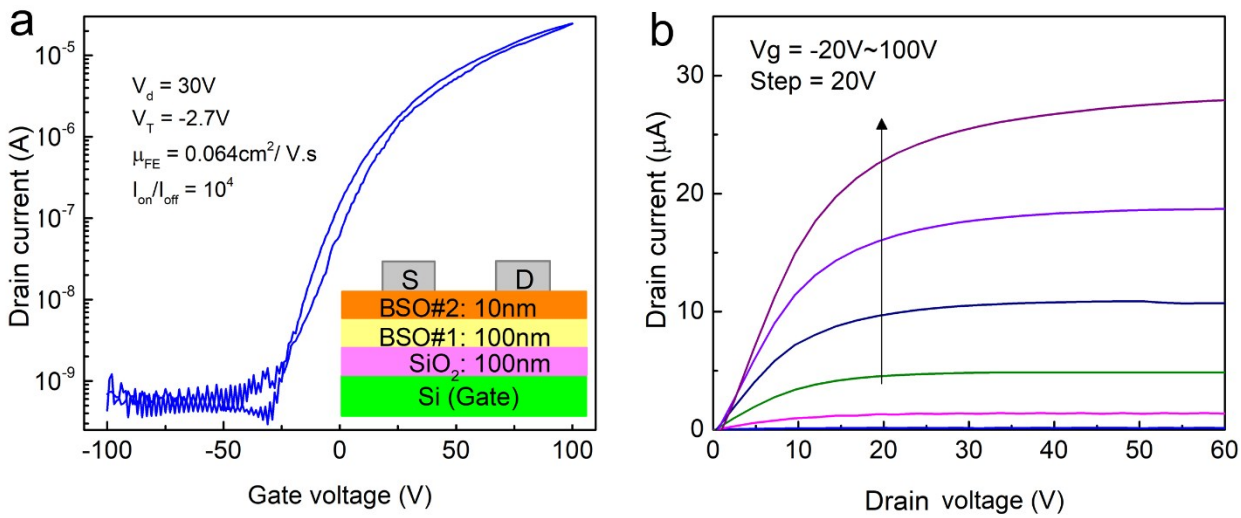

Figure S8. Transfer (a) and output (b) curves of BSO TFTs (W/L= 4000 μm/100 μm) on SiO_2/Si substrate. The bilayer BSO thin films were prepared using the following parameters: BSO#1, 50W, 3mTorr, Ar: O_2=5:8, 100nm; BSO#2, 50W, 3mTorr, Ar: O_2=7:7, 10nm.

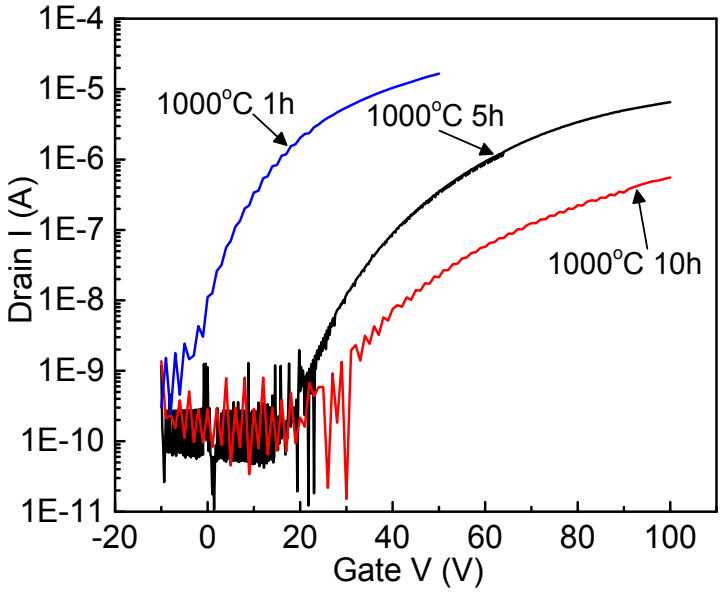

Figure S9. Id-Vg curves of BSO TFTs on Si substrate with different annealing times of BSO dielectric layer.

Table TS2. TFT device properties with different annealing durations of BSO dielectric layer.

Annealing hours of BSO-1# at 1000°C (h)	Device size	Threshold Voltage (V)	Field effect Mobility	On/Off ratio
1	75/4000 μm	-1.1V	7.86E-02	10^4
5	75/4000 μm	18.79V	1.43E-02	10^4
10	75/4000 μm	32.9V	3.21E-04	10^3

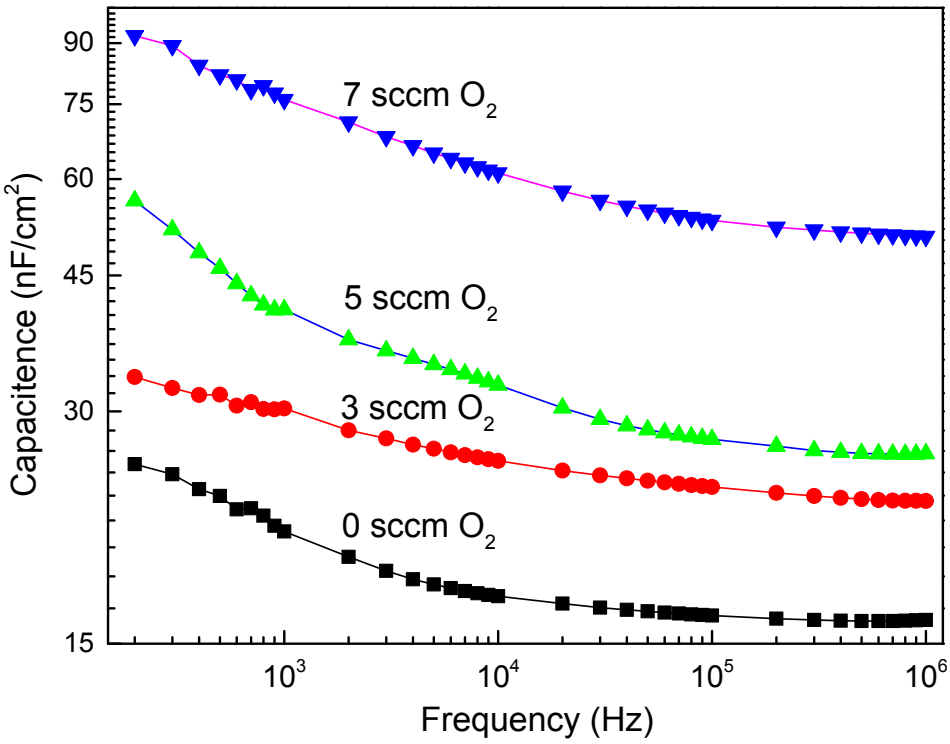

Figure S10. C-f curves of BSO on Si substrate with different O_2 content during the sputtering process. The thickness of BSO was 100 nm, sputtering power was 50 W, the vacuum pressure was 3 mTorr, and the annealing time was 1 hour at 1000℃.

Table TS3. AC Hall results of sputtering BSO (RF power=50W) thin films

Annealing temperature	Geometric size (mm^2)	Carrier mobility ($cm^2/V.s$)	Carrier density ($/cm^3$)
600℃	7×7	2.55	1.97×10^{16}
750℃	7×7	5.23	1.39×10^{14}
800℃	7×7	10.35	1.67×10^{14}
850℃	7×7	22.02	1.33×10^{14}
900℃	7×7	18.32	2.23×10^{13}
950℃	7×7	11.82	3.77×10^{13}
1000℃	7×7	6.33	3.21×10^{13}

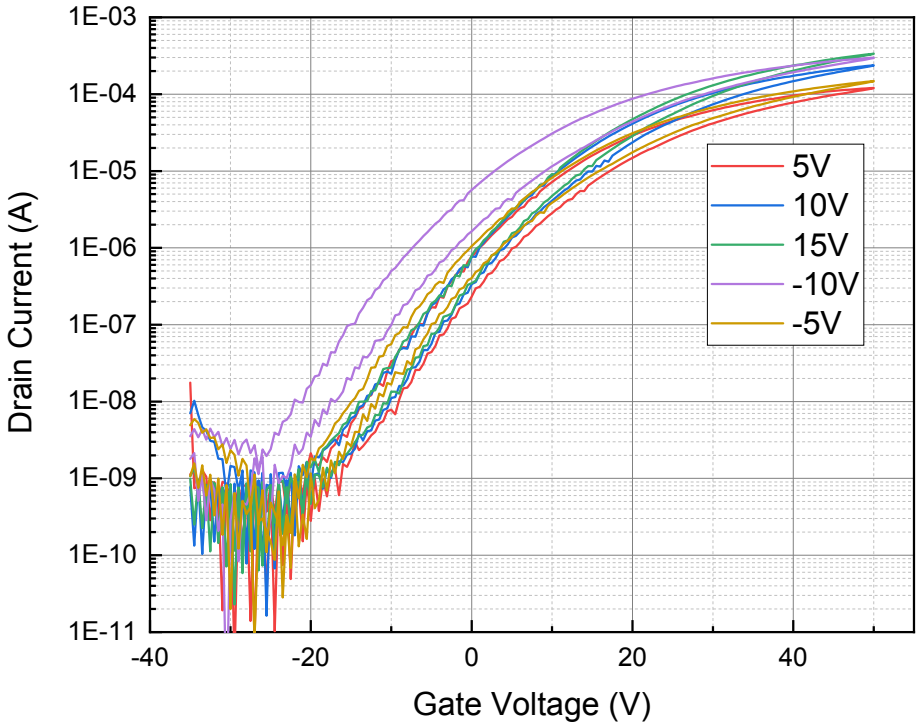

Figure S11. The different drain voltage influence on the transfer cuve of BSO bilayer TFT on siclicon substrate, the drain voltage are changed from -10V to 15V.

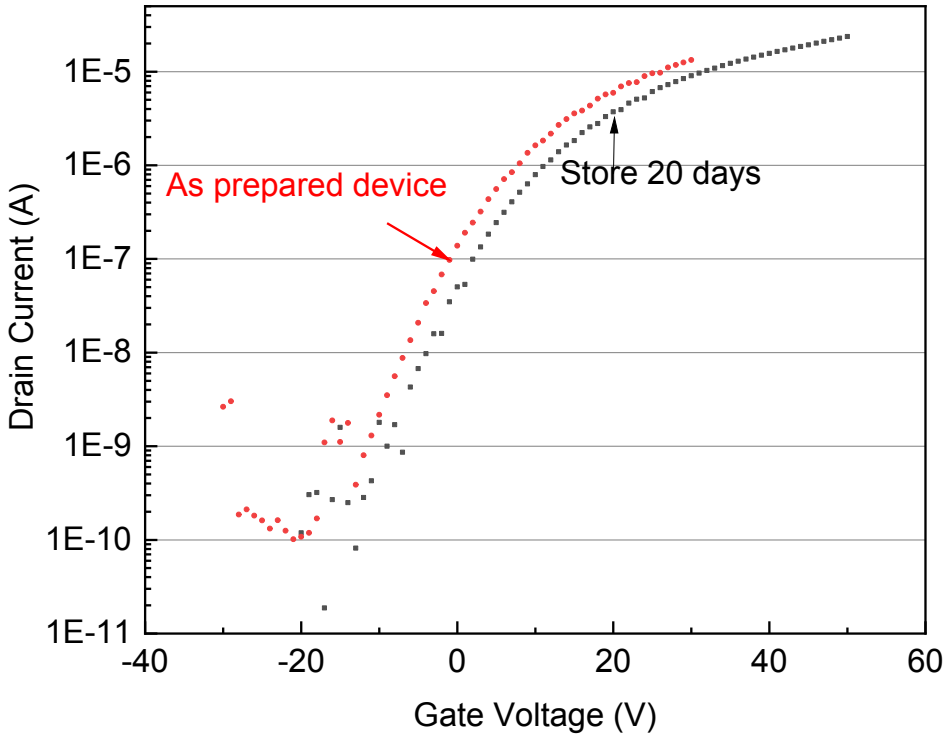

Figure S12. The stability of BSO TFTs on silicon substrate.