## **Supporting information**

## Vertically Conductive MoS<sub>2</sub> Pyramids with High Density of Active Edge Sites for Efficient Hydrogen Evolution

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Figure S1. Schematic CVD growth parameters and source distance adjustment for  $MoS_2$  pyramids growth on silica substrates.

The silica substrate was cleaned by acetone, ethanol and DI-water in sequence and dried with nitrogen. Then, the substrate was placed face-down above a crucible containing 3 mg of  $MoO_3$  (99.95%, Aladdin) and loaded into a 4 cm diameter quartz tube three-zone CVD furnace (OTF-1200X). The whole process was performed at atmospheric pressure, using ultra-high-purity Ar (99.999 %) as carrier gas. Another crucible containing 500 mg of sulfur (99.99 %, Aladdin) was located upstream. The distance between the S crucible and the growth substrate was varied to control the morphology of  $MoS_2$  pyramids. The furnace temperature was ramped up to 300 °C with a rate of 20 °C/min and kept constant for 10 min. Then, the temperature was ramped up to 730 °C with a rate of 50 °C/min. After 10 min at 730 °C, the furnace was cooled down with the heater removed. The Ar flow rate was 50 sccm (standard cubic centimeter per minute) when the temperature stayed at 730 °C and 200 sccm during temperature ramp up and the cooling.



Figure S2. (a) Photograph of five samples placed on different positions (marked in Figure S1) in the tubular furnace with the growth of  $MoS_2$  pyramids by CVD. (b-f) the corresponding SEM images of the five samples (S1, S2, S3, S4 and S5). The distances between the S crucible and this five samples (S1, S2, S3, S4 and S5) are 15, 30, 45, 60 and 75 cm, respectively.



Figure S3. TEM images of (a, b) a dispersed  $MoS_2$  pyramid and (c) the corresponding SAED patterns. TEM images of (d, e) two overlapped  $MoS_2$  pyramids and (c) the corresponding SAED patterns.



Figure S4. AFM images and the corresponding height profiles of (a, b) a MoS<sub>2</sub> flake and (c, d) a MoS<sub>2</sub> pyramid.



Figure S5. SEM images of MoS<sub>2</sub> pyramids with (a, b) right-handed spiral and (c, d) left-handed spiral.

According to Burton-Cabrera-Frank theory,<sup>[1]</sup> spiral dislocations can cause the growth of spiral structures. To form a spiral dislocation core in the MoS<sub>2</sub> spiral, a sliding plane, that is, a spiral defect, needs to be generated at the bottom layer, otherwise the growth will follow the in-plane growth mode and generate a single layer of  $MoS_2$ .<sup>[2–4]</sup> In our experiments, the occurrence of spiral defects is mainly due to the roughness of the surface of the growth substrate. Under the same growth conditions,  $MoS_2$  grown on SiO<sub>2</sub>/Si substrates whose surface can reach atomic smoothness is a single-layer or few-layer structure. Once a spiral dislocation is generated, it will remain active and gradually grow in the vertical direction, because continuous growth at the boundary position of the dislocation center is energetically favorable. At the same time, the exposure boundary continues to grow, and a 60° angle is preferentially formed on each single layer (each rotation is 120° to expose the low-energy zigzag boundary<sup>[5]</sup>). Finally, because the upper MoS<sub>2</sub> layer is formed later with a shorter growth time, the upper layer will be smaller, so the whole will grow into a three-dimensional atomic layer spiral pyramid structure.<sup>[2]</sup>



Figure S6. SEM images of (a) monolayer MoS<sub>2</sub> flakes, (b) dispersed MoS<sub>2</sub> pyramids and (c) overlapped MoS<sub>2</sub> pyramids for electrochemical measurements.



Figure S7. SEM images of dispersed MoS<sub>2</sub> pyramids (a) before and (b) after HER process.

	MoS <sub>2</sub> pyramids	MoS <sub>2</sub> pyramids	MoS <sub>2</sub> flakes
Equivalent circuit	CPE <sub>dl</sub> R <sub>overall</sub> R <sub>ct, dl</sub>		
$R_{overall}(\Omega)$	1.4	2.3	2.2
$R_{ct,dl}(\Omega)$	22.8	278.6	1628
CPE <sub>dl</sub> (F)	7.56E-5	5.78E-5	6.03E-5
n <sub>dl</sub>	0.85	0.91	0.90

Table S1. The fitting results of impedance plots shown in Figure 5 using the equivalent circuit in its inset.

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