

Supporting Information

Multilevel Vertical Photonic Memory Transistor Based on Organic

Semiconductor/Inorganic Perovskite Quantum Dots Blends

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The fabrication process of photonic memory transistor based on organic semiconductor/inorganic perovskite QDs blends

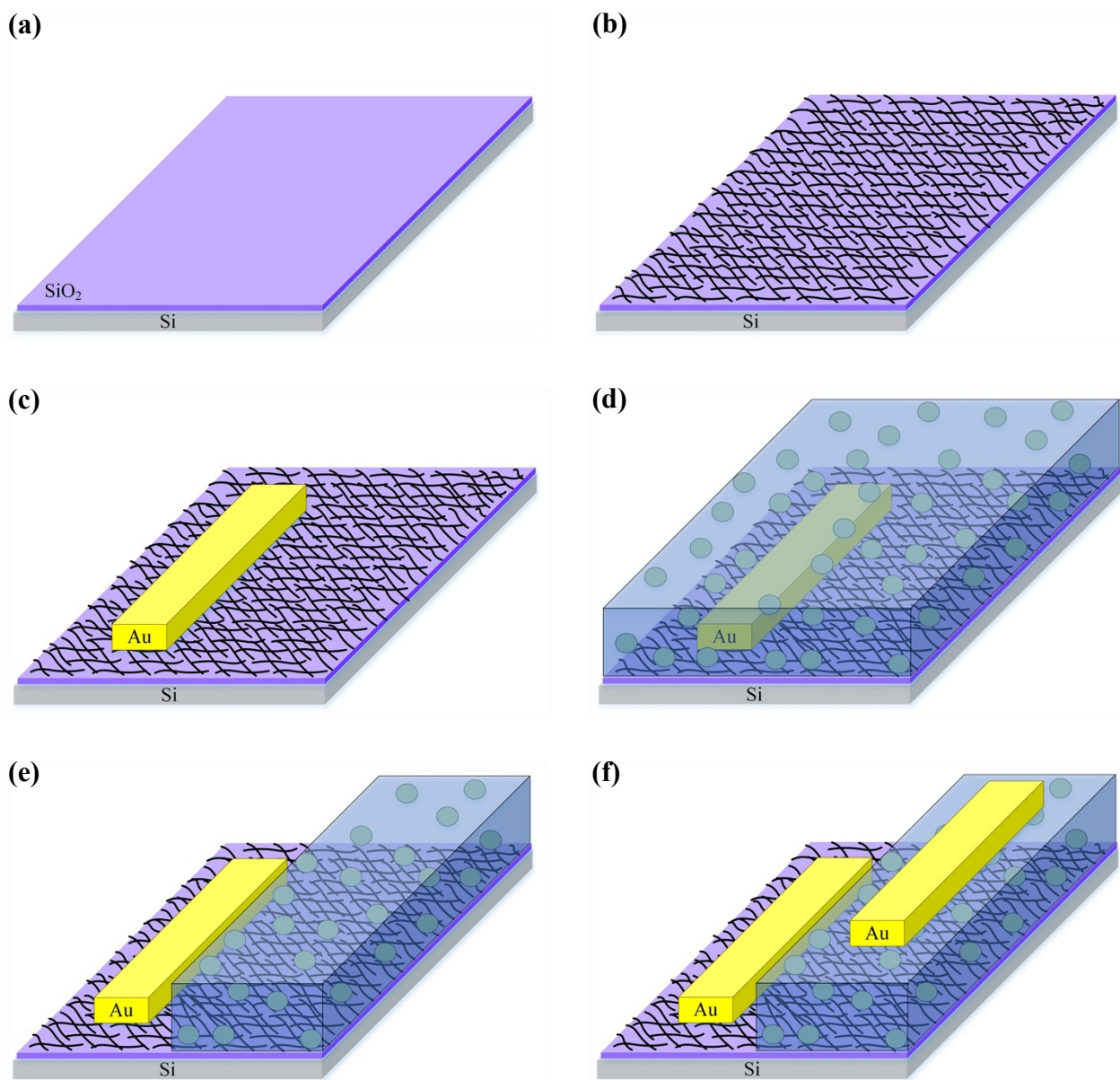


Figure S1. Schematic illustration of fabrication process of devices. (a) the precleaned SiO₂ substrate, (b) coating of Ag nanowires, (c) thermal evaporation of gold as source electrode, (d) coating of prepared PCDTPT/perovskite QDs precursor solution, (e) partly immersed in chloroform to remove the unwanted part of blending film to obtain naked source electrode, (f) thermal evaporation of gold as drain electrode.

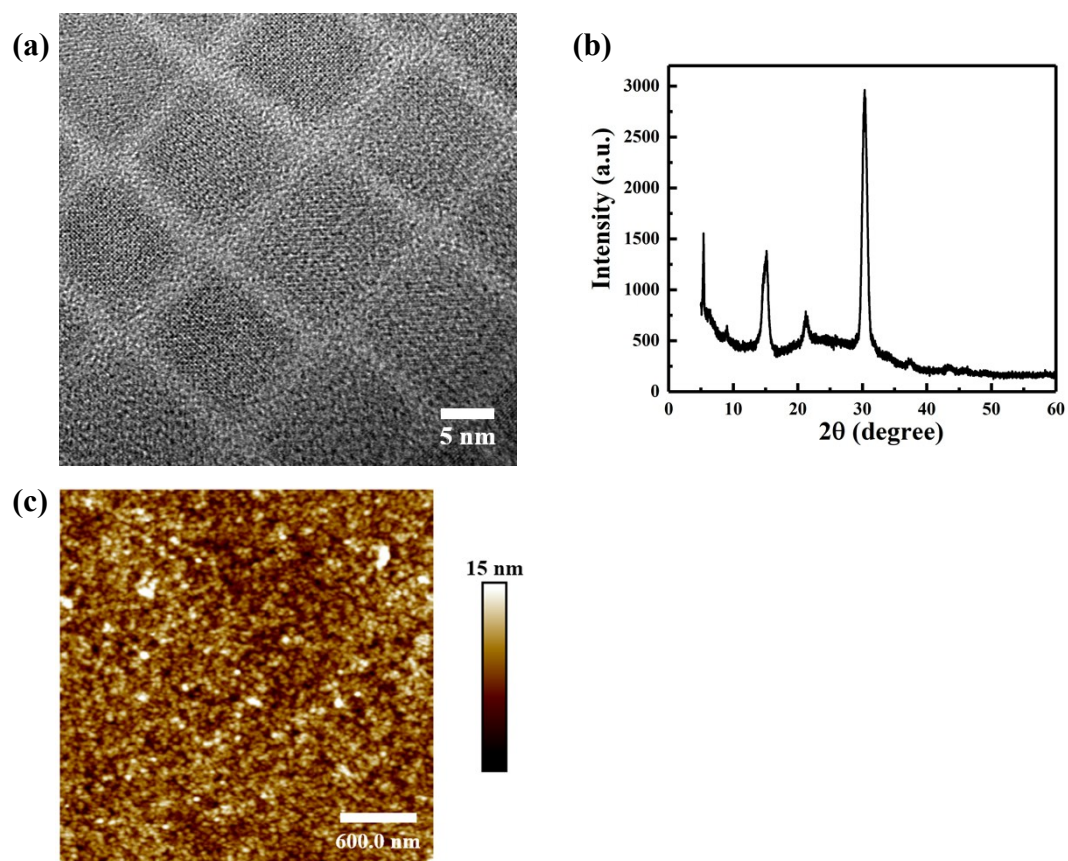


Figure S2. (a) the TEM image of the dispersed and highly ordered perovskite QDs, (b) the X-ray diffraction pattern of the perovskite QDs and (c) AFM image of blend film.

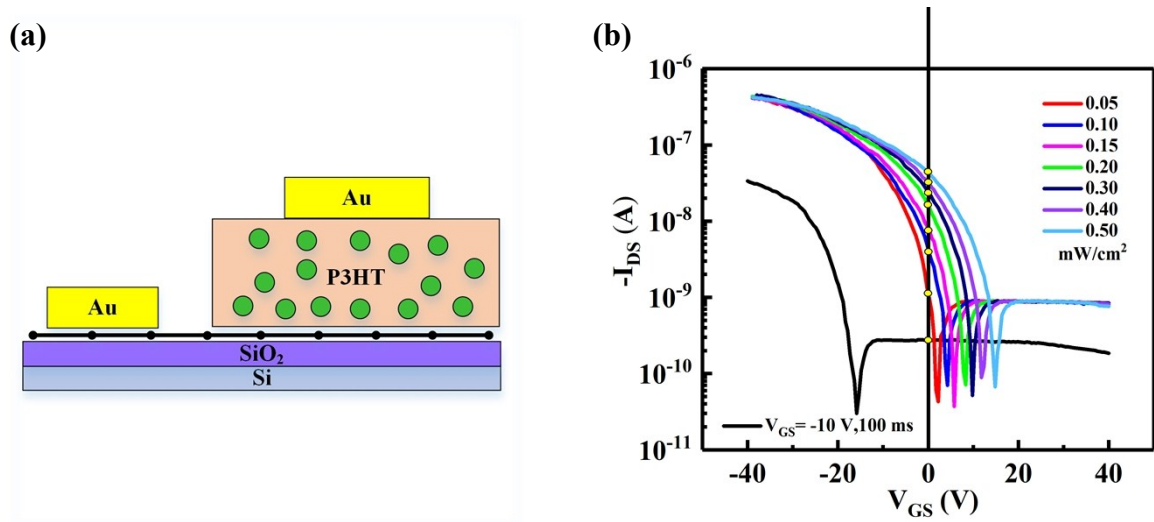


Figure S3. (a) The device structure of the photonic memory transistor based on P3HT/CsPbBr₃ perovskite QDs blends, (b) the corresponding transfer curves of photonic memory under UV light (300 nm, 0.5 s) with different light intensity.

Table S1. Partial ASCII Code Interconversion Table

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ASCII value	character	Bin ⁱ	Oct ⁱⁱ	Hex ⁱⁱⁱ	ASCII value	character	Bin	Oct	Hex
65	A	0100 0001	101	41	78	N	0100 1110	116	4E
66	B	0100 0010	102	42	79	O	0100 1111	117	4F
67	C	0100 0011	103	43	80	P	0101 0000	120	50
68	D	0100 0100	104	44	81	Q	0101 0001	121	51
69	E	0100 0101	105	45	82	R	0101 0010	122	52
70	F	0100 0110	106	46	83	S	0101 0011	123	53
71	G	0100 0111	107	47	84	T	0101 0100	124	54
72	H	0100 1000	110	48	85	U	0101 0101	125	55
73	I	0100 1001	111	49	86	V	0101 0110	126	56
74	J	0100 1010	112	4A	87	W	0101 0111	127	57
75	K	0100 1011	113	4B	88	X	0101 1000	130	58
76	L	0100 1100	114	4C	89	Y	0101 1001	131	59
77	M	0100 1101	115	4D	90	Z	0101 1010	132	5A

ⁱ Binary

ⁱⁱ Octal

ⁱⁱⁱ Hexadecimal