Supplementary Material for Chemical Communications
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Electronic Supporting Information

Detailed experimental section:

CdS nanostructures were synthesized in a quartz tube, heated with a three-zone furnace. The quartz tube was with a diameter of 2.5 cm and length of 65 cm. The three-zone furnace was with a length of 45 cm. For three-zone hot-wall furnaces, the set temperature is achieved at the central portion of the furnace, about 12 cm in length. The furnace temperature ramps down to lower temperatures at the furnace entrance and exit. In the present work, we collected the deposits with quartz or silicon plates at locations near the furnace entrance with collection temperatures of 250, 350, and 400°C, corresponding to furnace temperatures of 350, 450, and 550°C, respectively. The molecular single-source precursor, $Cd(S_2CNProp_2)_2$, had been proven capable of growing CdS nanowires with the VLS mechanism at low temperatures in our previous study. The depositions were run at an amount of 0.1 gram of precursor for 6 hr. The precursor was used up at the end of the deposition.

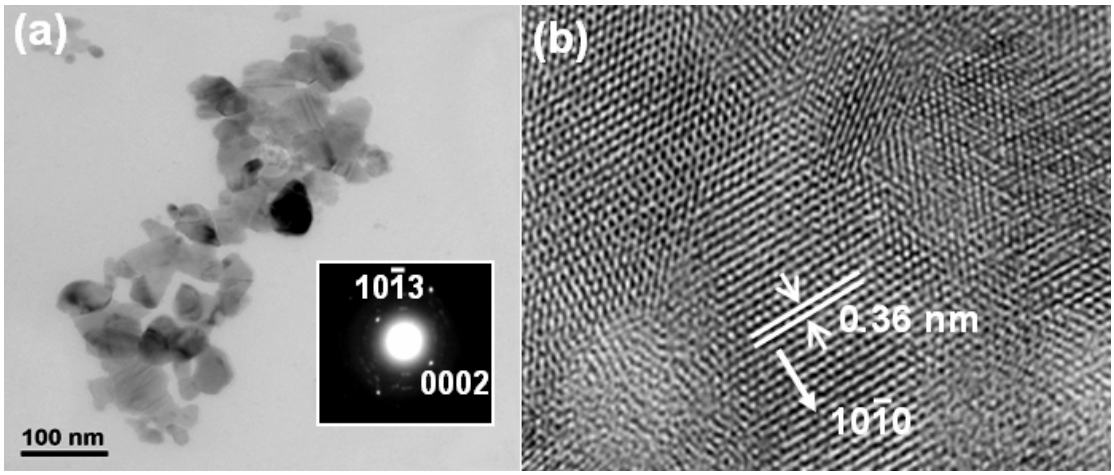

Figure S1. (a) TEM image of CdS nanoparticles, freed from the quartz substrate with ultrasonic agitation, obtained at the furnace temperature of 350°C. The inset is the corresponding SAED pattern. (b) Enlarged HRTEM image of the CdS nanoparticles with the *d*-spacing and lattice plane indicated.

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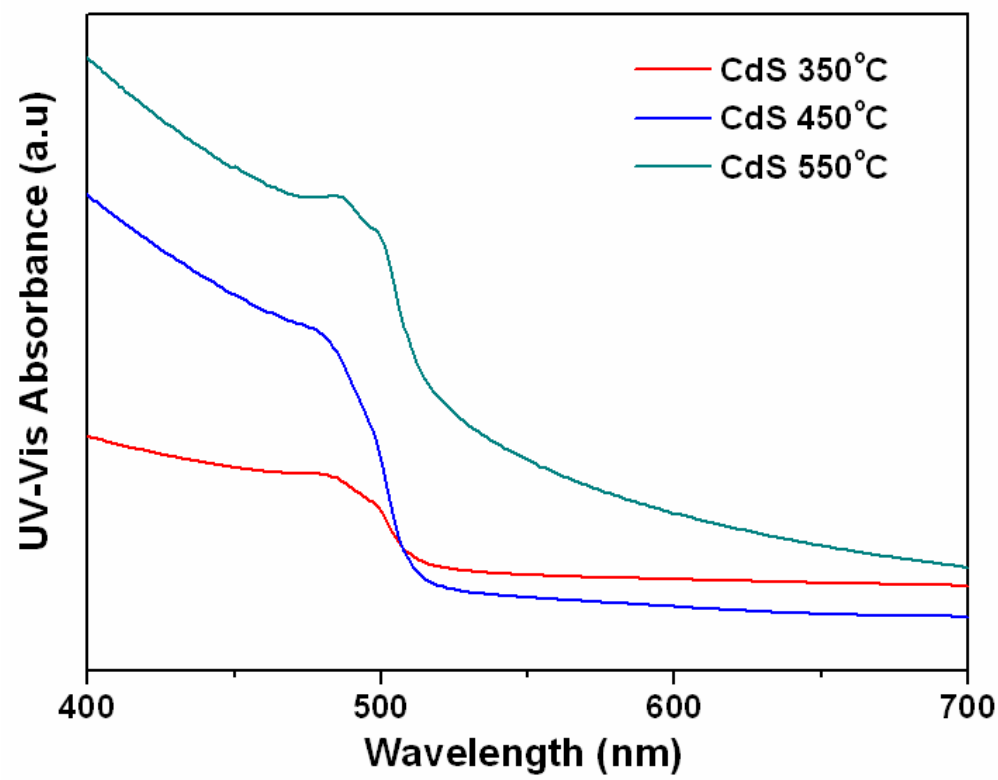

Figure S2. UV-visible absorption spectra of the as-prepared CdS nanostructures. An absorption edge at around 500 nm was observed for the three nanostructures, confirming to the direct band gap energy of bulk hexagonal CdS crystals (E_g=2.5 eV, corresponding to an absorption edge of 496 nm).

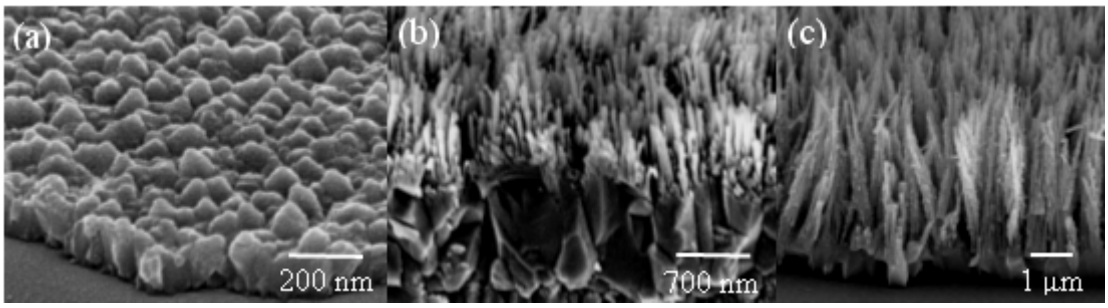

Figure S3. SEM images of the CdS nanostructures grown on Si(100) substrate. (a) nanoparticle-film prepared at 350°C. (b) bundles of quasi-aligned nanowire prepared at 450°C. (c) bundles of well-aligned nanowires prepared at 550°C. The CdS nanostructures grown on Si(100) substrate possessed similar morphologies to those grown on quartz substrate.

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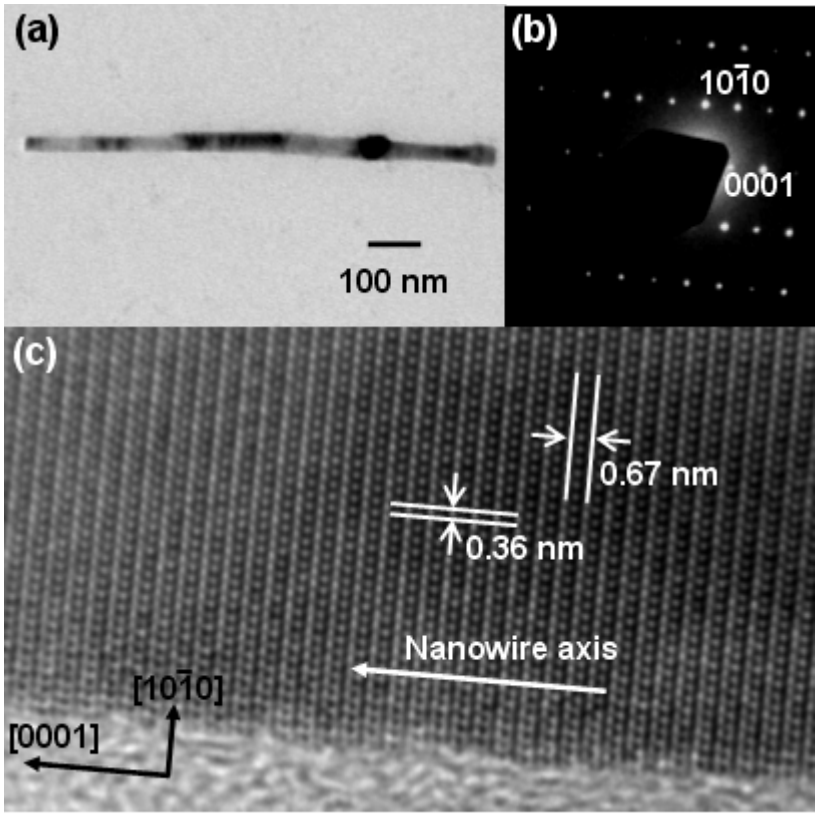

Figure S4. (a) TEM image of CdS nanowires, freed from the Si(100) substrate with ultrasonic agitation, obtained at the furnace temperature of 450°C. (b), (c) The corresponding SAED pattern and enlarged HRTEM image with the *d*-spacing, lattice planes, and growth direction indicated.

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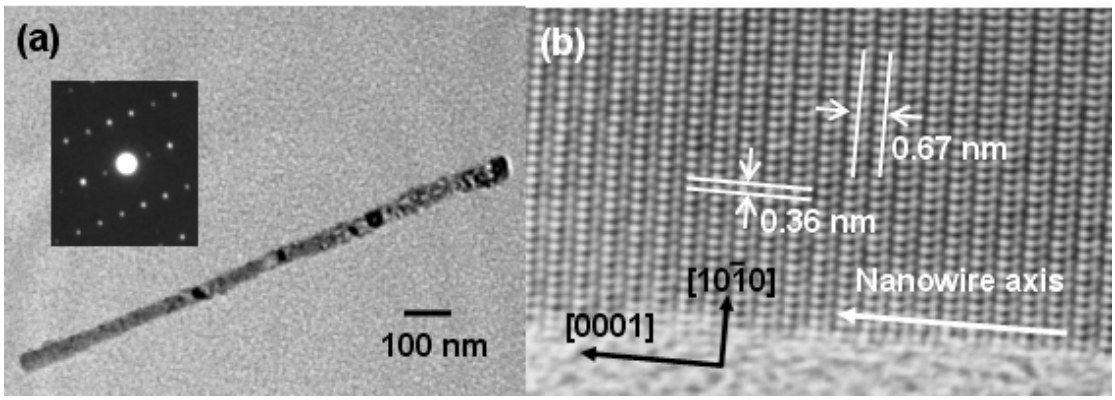

Fig. S5. (a) TEM image of a free-standing CdS nanowire, freed from the Si(100) substrate with ultrasonic agitation, prepared at the furnace temperature of 550°C. The inset of (a) is the corresponding SAED pattern. (b) Enlarged HRTEM image with the *d*-spacing, lattice planes, and growth direction indicated.