Electronic Supplementary Material (ESI) for Chemical Communications

Imaging the Belousov–Zhabotinsky reaction in real time using an ion sensitive array

Balazs Nemeth[a], Christoph Busche[b], Soichiro Tsuda[c], Leroy Cronin[*b] and David R. S. Cumming[*a]

[a] *Electronics Design Centre, School of Engineering, University of Glasgow, G12 8LT (UK), E-mail: David.Cumming.2@glasgow.ac.uk, Web: http://www.gla.ac.uk/schools/engineering/staff/davidcumming/*

[b] *WestCHEM, School of Chemistry, University of Glasgow, G12 8QQ (UK), E-mail: Lee.Cronin@glasgow.ac.uk; Web: http:// www.croninlab.com*

[c] *Exploratory Research for Advanced Technology (ERATO), Japan Science and Technology Agency, Yamadaoka 1-5, Suita, Osaka 565-0871 Japan, Email: tsuda-soichiro@bio.eng.osaka-u.ac.jp*

ISFET array

The 4476.4µm x 4323µm large sensor chip was fabricated in an unmodified 0.35µm four-metal CMOS process; the on-chip 64x64-pixel ISFET sensor array occupied an area of 715.8µm x 715.8µm. A Silver/silverchloride (Ag/AgCl) reference electrode was used to set electric voltage bias in the electrolyte during the BZ measurements. Fig. S1 demonstrates the architecture of the sensor array as well as the schematic of the pixel circuits.

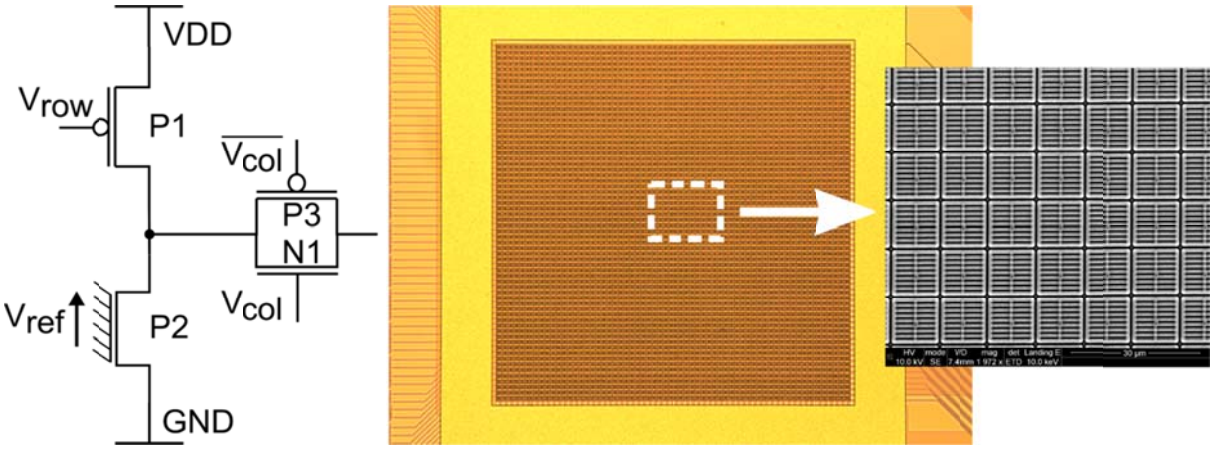

Fig. S1 Schematic of the pixel circuits and the fabricated ISFET array

The P1 PMOS transistor performs multiple functionalities; on the one hand row addressing connecting to the input row-selector multiplexers, on the other hand providing a sufficient current of approximately 16µA for the pixel circuit as load transistor. The gate voltage of P1 rises to 1.2V if the pixel is activated, acting as a current source for the P2 ISFET that is connected in a source-follower configuration. The gate voltage of the ISFET transistor is controlled by the Ag/AgCl reference electrode through the electrolyte and the passivation layer.

The pixels in the same row are connected to the same output channel thus they have to be separated from the output if inactivated. The transmission-gate switch circuit guarantees that only one pixel has exclusive access to the output rail in a matrix row avoiding eventual current leakage problems between pixel units. The switches are controlled using a 6/64 decoder circuitry.

Operating principles

The system-level operation principles of the 64x64-pixel sensor array are demonstrated in Fig. S2. It is shown that pixels are activated when the respective address code is sent to the digital input terminals of the ISA chip which identifies the units, pixels are deactivated otherwise. A pixel address is transferred as an 8-bit data frame and is divided on-chip into row and column sets. The first 6 bits are routed to the input of the 6/64-type column decoder circuit to select the appropriate matrix column for readout. The last two bits are connected to the input and output line selector demultiplexers and multiplexers to choose the appropriate analogue channels.

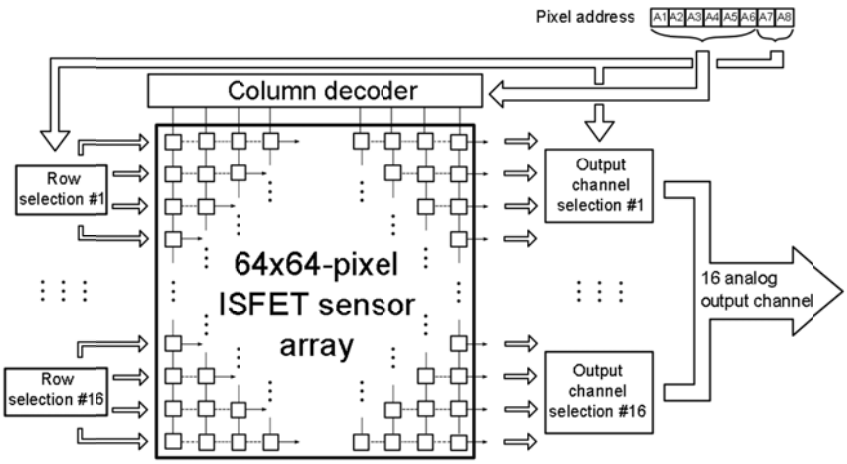

Fig. S2: System level operation principles of the 64x64-pixel ISFET sensor array

Data recording

The demand for high-speed data recording and high data throughput capability requires parallelization in the acquisition process. One digital pixel address frame therefore identifies 16 pixels at once and the continuous data readout is carried out on 16 analogue channels simultaneously. The rows of the ISA are grouped into sixteen 4-row blocks to match the number of available output channels. The addressing is implemented in a sequential manner inside the groups of four rows; hence the complete readout of the 64x64-pixel ISA takes as long as the readout of four lines does, using the parallelized data acquisition. The readout of the 64x64-pixel ISA takes 256 time units because there are 256 pixels in a 4-row block which furthermore implies a 58 FPS (frame per second) data acquisition speed at a sampling rate of 66µs per pixel. The acquired complete data frames of the sensor array are dispatched by the real-time system to the host computer. The 58 FPS data acquisition rate indicates therefore a minimal bandwidth need of 0.91 MB/s, 54.6 MB/min. The measurements were performed on PXI-Express platform from National Instruments to meet the hardware requirements.

Encapsulation

It is important to encapsulate the devices to avoid potential short circuits between bonding wires. Thus a sealant (epoxy glue) was deposited, exposing only the essential regions of the nitride layer to the electrolyte.

pH calibration

The pH calibration a concentration series was made and the array was flushed several times between the measurements with 1) demineralised water and 2) the next solution. The 20 mV/pH sensitivity is demonstrated in Fig. S3 and S4.

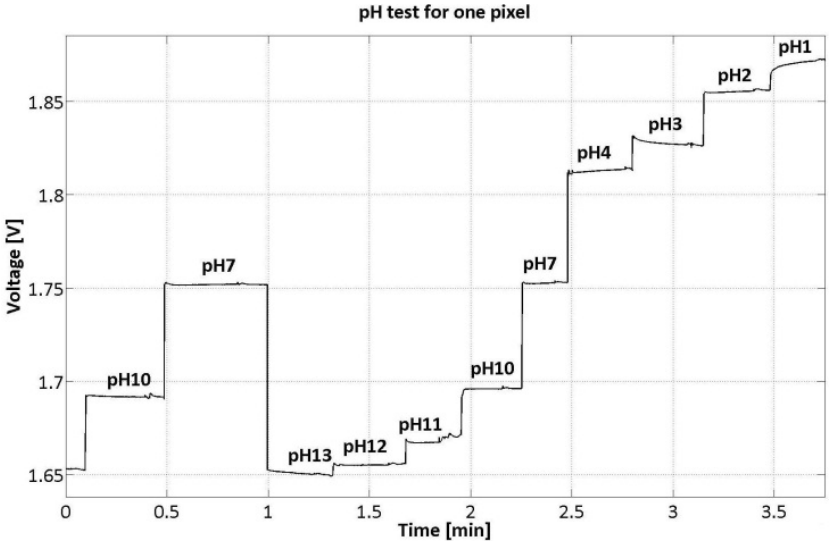

Fig. S3: Voltage output values of the ISFET array corresponding to different pH levels

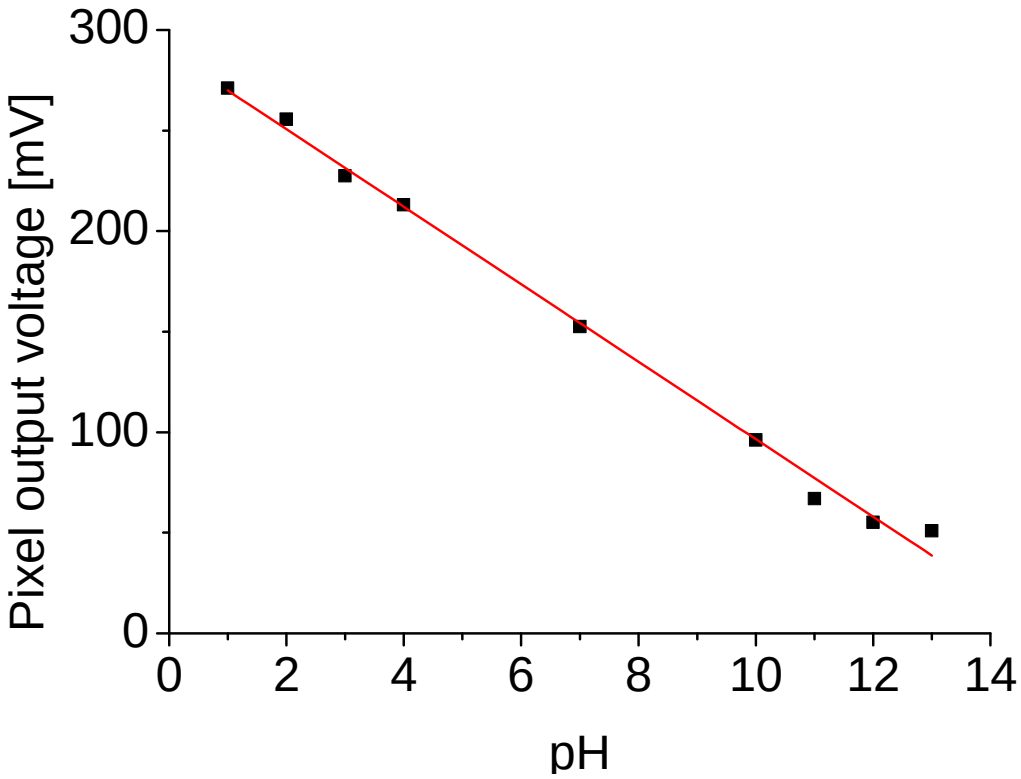

Fig. S4: Voltage output correlation extracted from Fig S3 (slope: 19.2 ± 0.5 mV/pH)