Electronic Supplementary Material (ESI) for Chemical Communications

Electronic Supplementary Information

Mode tunable p-type Si nanowire transistor based zero drive load logic inverter

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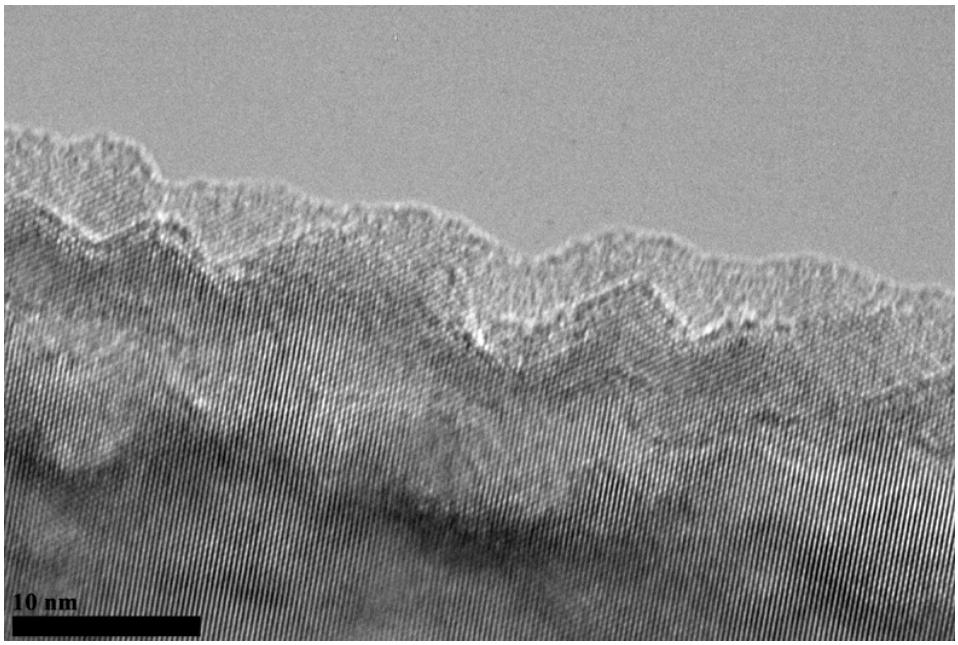

Figure S1. High-resolution TEM images of *p*-type Si NWs fabricated by the electroless etching method. The lengths of arbitrary straigth lines along the length of a NW and the length of the surface profile curves were 52.3 nm and 69.1 nm, respectively. This result implys that Si NWs have a rough surface and can absorb more OH^- ions.

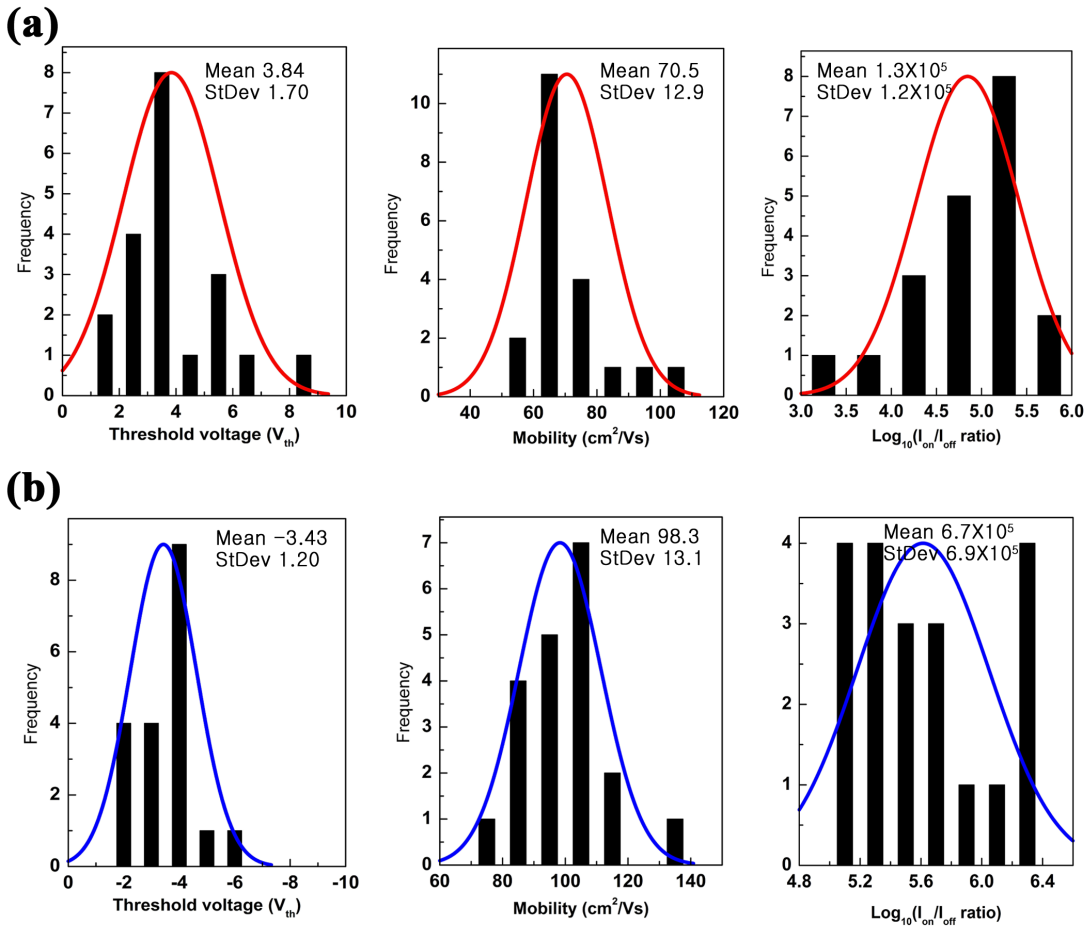

Figure S2. The statistical analysis of threshold voltages, field-effect mobilities, and I_{on}/I_{off} ratio of FETs fabricated from (a) the non-implanted Si NWs and (b) the implanted Si NWs on PVP layers.