Unsorted Single Walled Carbon Nanotube Enabled High Performance Organic Thin Film Transistors with Low Cost Metal Electrodes

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Supplementary Information

Experimental

Preparation of Diketopyrrolopyrrole-Quaterthiophene Copolymer (DPP-QT) solution:

DPP-QT was synthesized following the procedure reported by Choi et al [J. S. Ha, K. H. Kim, and D. H. Choi, *JACS*, 2011, **133**, 10364–10367]. The DPP-QT polymer (0.02 g) was dissolved in 1,1,2,2-tetrachlorethane (3.98 g) for 2 hours at 80^{o}C in the absence of light to form a 0.5 wt% solution.

Preparation of DPP-QT / SWCNT dispersion:

A dispersion of 5 wt% SWCNT respective to the total weight of the DPP-QT and SWCNT was first prepared by adding 1.5 mg of Sigma Aldrich (704148) (6,5) chirality, carbon >90 %, 77% (carbon as SWCNT), 0.7 – 0.9 nm diameter, 0.5 – 2 µm length, to 5.6985 g of 0.5 wt% DPP-QT solution. The mixture was immersed in an ice bath and probe sonicated on a Branson Digital Sonifier-450 (400 W) at 35% amplitude for 2 min. Originally, the resultant dark green dispersion was centrifuged at 25,000 g force for 30 min and the supernate was collected. After the centrifuge, no precipitate was observed at the bottom of the container. The SWCNTs were well dispersed and remained in the polymer solution. Therefore, the centrifuge step was deemed unnecessary and no longer performed. This DPP-QT/SWCNT dispersion was further diluted using the 0.5 wt% DPP-QT solution, yielding a dispersion of 2 wt% SWCNT respective to the total weight of the DPP-QT and SWCNT, for OTFT device fabrication. The concentration of SWCNTs in the dispersion is around 0.01 wt%.

OTFT Fabrication and Evaluation:

All fabrication and characterization of organic thin-film transistor devices (OTFTs) was done under ambient conditions taking precautions to isolate the material and device from light, but no precautions were taken to isolate the material or device from exposure to air or moisture. After fabrication, devices were stored under vacuum in the dark, and measured in air within 2 hours of being removed from vacuum. Bottom-gate TFT devices were built on n-doped silicon wafer as the gate electrode with a 200-nm thermal silicon oxide (SiO_2) as the dielectric layer. The SiO_2 surface was plasma cleaned for 2 minutes. The wafer was subsequently rinsed with H_2O then isopropanol and dried with an air stream. The SiO_2 surface was modified with octyltrichlorosilane (OTS-8) by immersing the cleaned silicon wafer substrate in 0.1 M OTS-8 in toluene at 60 ^{o}C for 20 min. The wafer was subsequently rinsed with toluene and isopropanol and dried with an air stream. The DPP-QT solution or DPP-QT/SWCNT dispersion was dispensed onto the OTS-8-modified SiO_2 layer allowed to sit for 2 min, then spun with a 2 s ramp time, at 2000 rpm for 120 s, yielding ~ 30 nm semiconductor layer. The semiconductor films were vacuum dried at 70 ^{o}C for 30 min and annealed at 140 ^{o}C for 40 min, and allowed to cool to room temperature under vacuum. The same semiconductor thin films were used for OTFT devices as well as SEM and AFM characterization. To complete OTFT devices, the Au, Cu and Al source and drain electrodes were deposited by vacuum evaporation through a shadow mask on top of the semiconductor layer with channel lengths of 40, 90, 190 and 370 µm and a width of 1 mm. To generate channel lengths below 40

μm, a 20 μm microwire was taped (at the sample edge) onto a wafer. The appropriate metal was deposited and the wire was removed, revealing a 20 μm channel. Using an electrode tip, the edges were scratched to generate a channel width of approximately 1mm. The actual channel lengths and widths were measured using an optical microscope.

From I_D-V_G measurements, the mobility was extracted from the saturated regime using the following equation ($V_D > V_G$): $I_D = C_i\mu(W/2L)(V_G - V_T)^2$. Where I_D is the drain current, C_i is the capacitance per unit area of the gate dielectric layer, V_G and V_T are respectively the gate voltage and threshold voltage. V_T of the device was determined from the relationship between the square root of I_D at the saturated regime and V_G of the device by extrapolating the measured data to I_D=0.

Instrumentation

SEM Imaging

Samples were imaged in their native condition (no conductive coating applied) using a Hitachi SU-8000 field emission scanning electron microscope (SEM) operating in deceleration mode with a landing voltage of 700 V.

Atomic Force Microscopy

Samples were collected on a Park Systems XE-100 AFM operated in dynamic force mode. Each image had 2-3 samples imaged with the most representative sample displayed in this report.

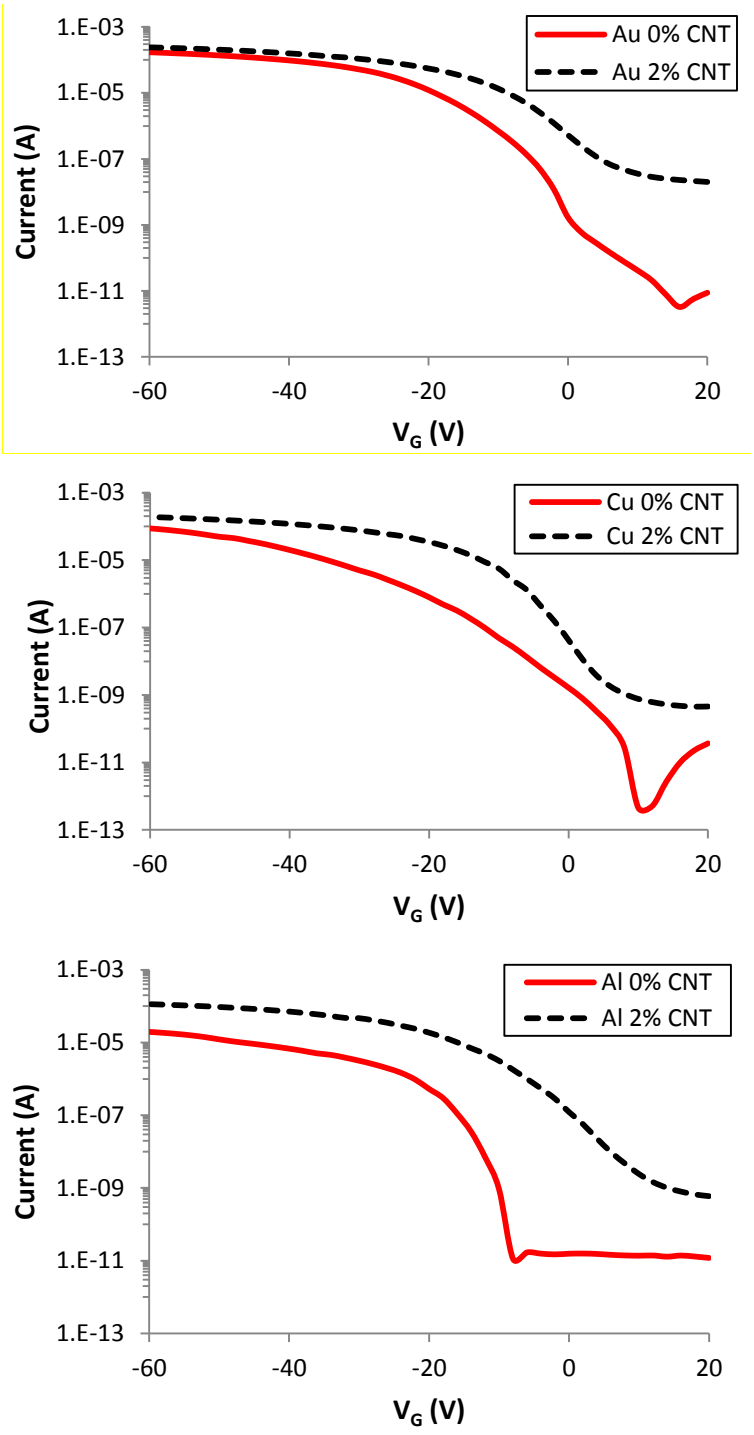

Figure 1S. Transfer curves for OTFTs having Au, Cu and Al electrodes with and without 2wt% CNT in the DPP-QT film. The transistors have a channel length of 40 µm and a channel width of 1000 µm.

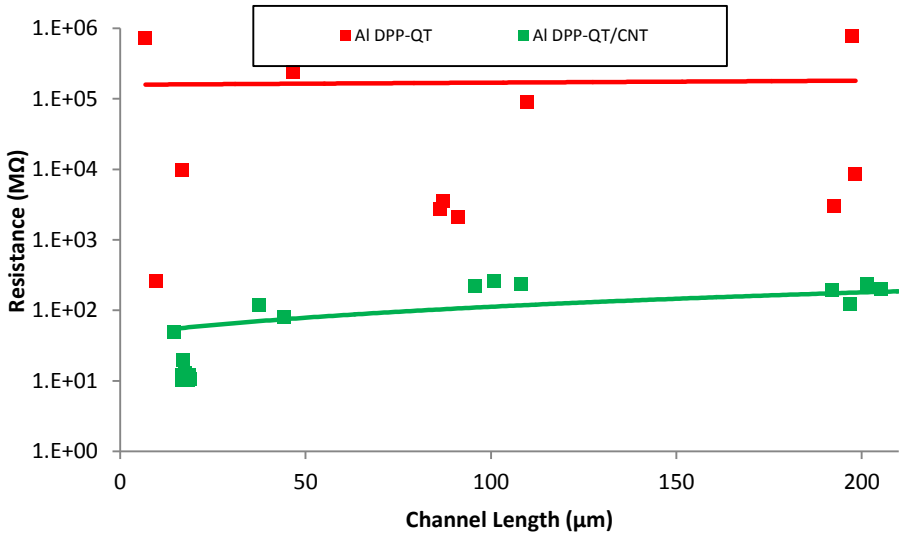

Figure 2S. Resistance vs channel length using Al electrodes for a V_{GS} = -25 V. The y intercept represents the summation of the contact resistance into and out of the channel.