Electronic Supplementary Information

Sodium Ion Assisted Memory Behaviour of Silicon Nanowire Partial Composite Field Effect Transistor

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Experimental Section

The rough Si NWs were prepared from a boron-doped p-type Si (100) substrates with a resistivity of 1–10 Ω·cm by an electoless etching method. The details of the synthesis mechanisms of the rough NWs *via* the electroless etching method have been explained in many previous reports.[1,2] To form the well-shaped rough surface, the synthesis process was performed in an etching solution of 5 M HF and 0.3 M H_2O_2 for 2 h at 50 °C.[3] The length of the silicon nanowires was about 50 ~100 μm and the diameter was 10 ~500 nm.

Poly(vinyl alcohol) (PVA, Mowiol® 40–88, Sigma–Aldrich) with an average molecular weight of 130,000 was used as organic gate dielectrics. The PVA solution was categorized into three major types: a blend of 5 wt% PVA and sodium acetate (NaAc, 99.995%, Sigma–Aldrich) (Sample I. 1:0, Sample II. 1:0.05, and Sample III. 1:0.1 wt. ratios) in H_2O. The organic gate dielectric films were spun at 1500 rpm on the cleaned commercial degenerately doped Si substrate with a 200 nm-thick SiO_2 layer. In order to make higher interface-interaction between the rough Si NW semiconductor and PVA gate dielectric, the thin-film partial composite structure by transfer implantation was introduced in our previous work.[4] After embedding of the NWs in the PVA, the films were dried in an argon atmosphere for 12 h at 60 °C to remove the solvent from the organic dielectric films.

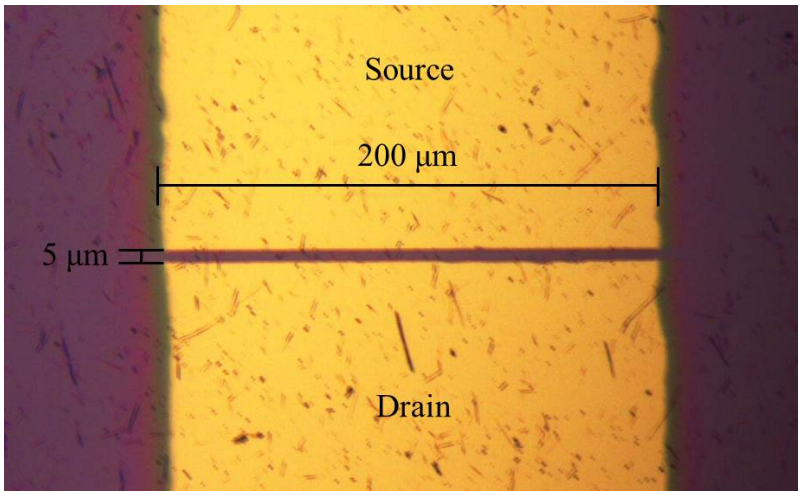

Fig. E1. A top image of the Si NW based field effect transistor

Finally, the transistor was completed by defining Au electrode as shown Fig. E1. The distance between source and drain was 5 μm the width of each electrode was 200 μm

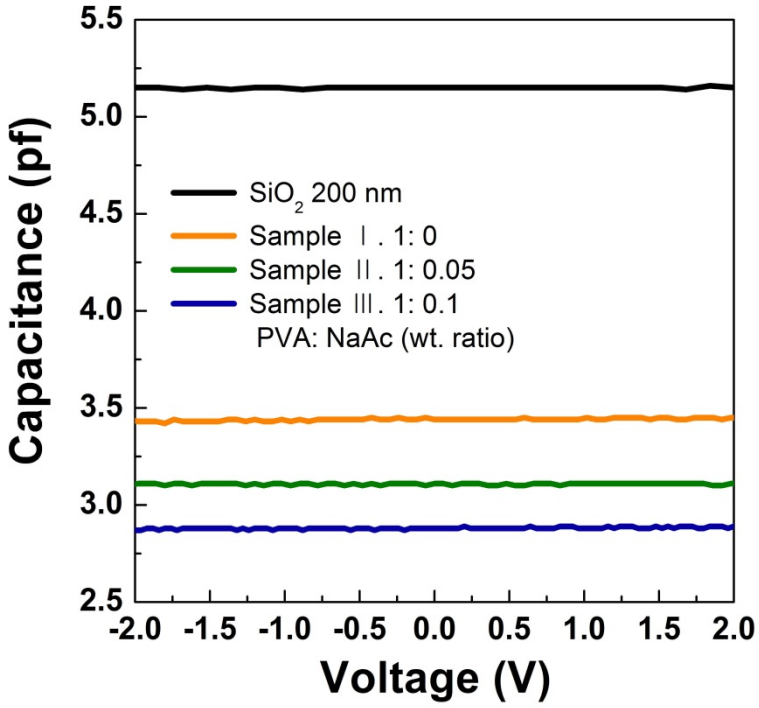

Figure S1. (a) The *C–V* characteristics of SiO_2 (thickness of 200 nm) and PVA gate dielectric for different concentration of NaAc in metal/insulator/metal (MIM) structures. The gate capacitances per unit of area (C_i) of SiO_2, Sample I, Sample II, and Sample III are 16.4, 11.0, 9.90, and 9.17 nF/cm^2, respectively. Dielectric constants (k) of Sample I (thickness: 330nm), Sample II (thickness: 410nm), and Sample III (thickness: 460nm) are calculated to be 4.09, 4.59, and 4.77, respectively.

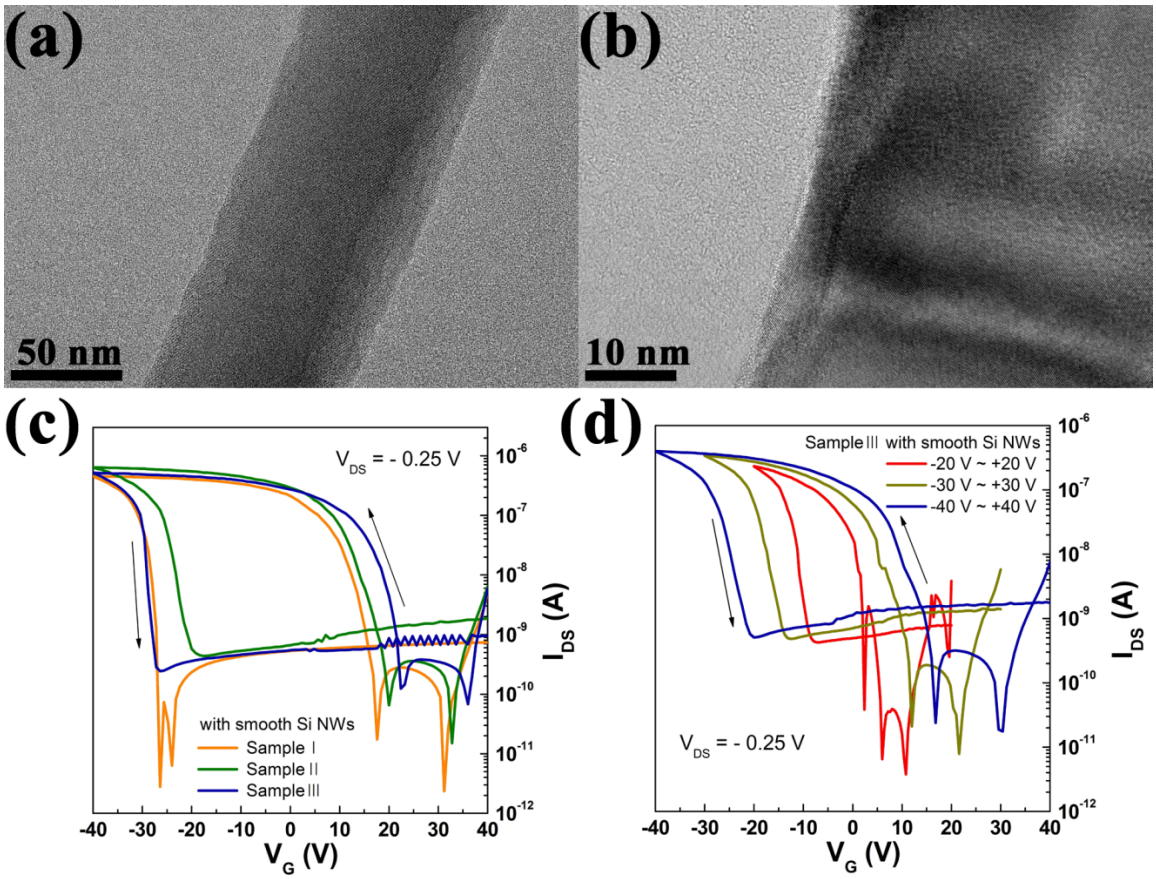

Figure S2. (a) TEM contrast image and (b) HR TEM image show a representative smooth surface of the Si NW. Boron-doped p-type Si (100) wafer with a resistivity of 1–10 Ω·cm was used as a starting wafer for fabrication of Si NWs. The synthesis process was performed in an etching solution of 5 M HF and 0.2 M H_2O_2 for 2 h at 50 °C. For smooth surface of NWs, post-annealing was carried out at 900 °C in O_2 ambient for 20 min. Subsequently, oxidized surface of Si NWs was etched in dilute HF and then rinsed in DI water. The details of the surface modulation process of the smooth NWs *via* the dry oxidation method have been explained in our previous reports.[5] (c) The transfer curves with smooth Si NWs at different concentration of NaAc in PVA dielectric. Transfer curves of forward sweep and backward sweep are shown for hysteresis measurement. The directions of the forward and backward sweeps are indicated. The hysteresis size of the smooth Si NWs has not changed appreciably as concentration of the mobile ions in PVA dielectric. (d) The transfer curves in Sample III with smooth Si NWs at different ranges of V_G sweep from ±20 V to ±40 V.

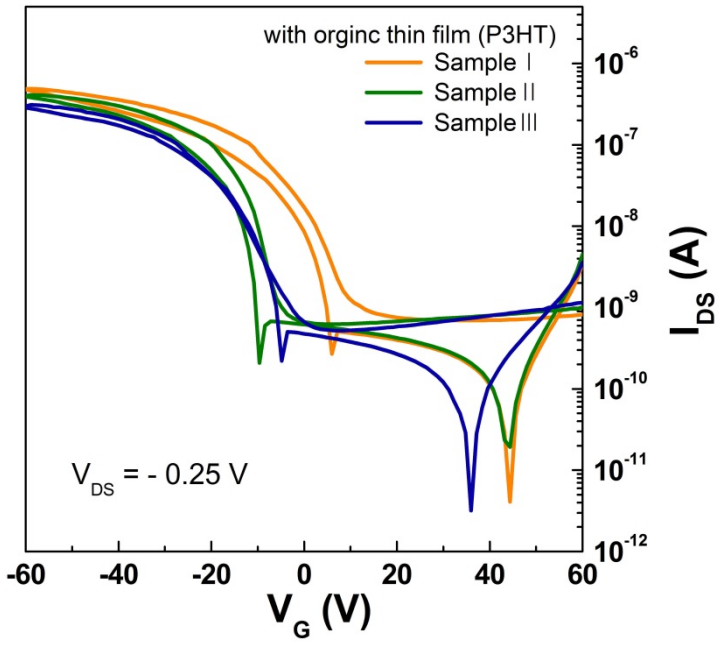

Figure S3. The transfer curves with organic thin-film semiconductor at different concentration of NaAc in PVA dielectric. The Poly(3-hexylthiophene-2,5-diyl) (P3HT) films were prepared by a 0.25 wt % P3HT in xylene and spun at 2000 rpm. The P3HT films were annealed in the vacuum for 3 h at 100 °C. Transfer curves of forward sweep and backward sweep are shown for hysteresis measurement. There are no big changes of hysteresis size and electrical properties as concentration of the mobile ions.

	Sample I	Sample II	Sample III
Gate capacitance per unit area (C_i, nF/cm^2)	6.58	6.17	5.88
Rough Si NW FETs			
Mobility (μ_{eff}, cm^2/V·s)	20–40	25–50	70–90
$I_{on/off}$ ratio	8000	1000	3000
Threshold voltage ($V_{th,forward}$)	23	3.9	–3.4
ΔV_{th}	50	24	4.8
Smooth Si NW FETs			
Mobility (μ_{eff}, cm^2/V·s)	100–250	150–250	100–300
$I_{on/off}$ ratio	25000	10000	5000
Threshold voltage ($V_{th,forward}$)	11	13	18
ΔV_{th}	40	40	45
P3HT thin-film transistor			
Mobility (μ_{eff}, cm^2/V·s)	0.01	0.03	0.01
$I_{on/off}$ ratio	2000	2000	1500
Threshold voltage ($V_{th,forward}$)	–7	–16	–15
ΔV_{th}	8	6	4

Table. S4. The electrical properties in each semiconductor were represented by numerical table.

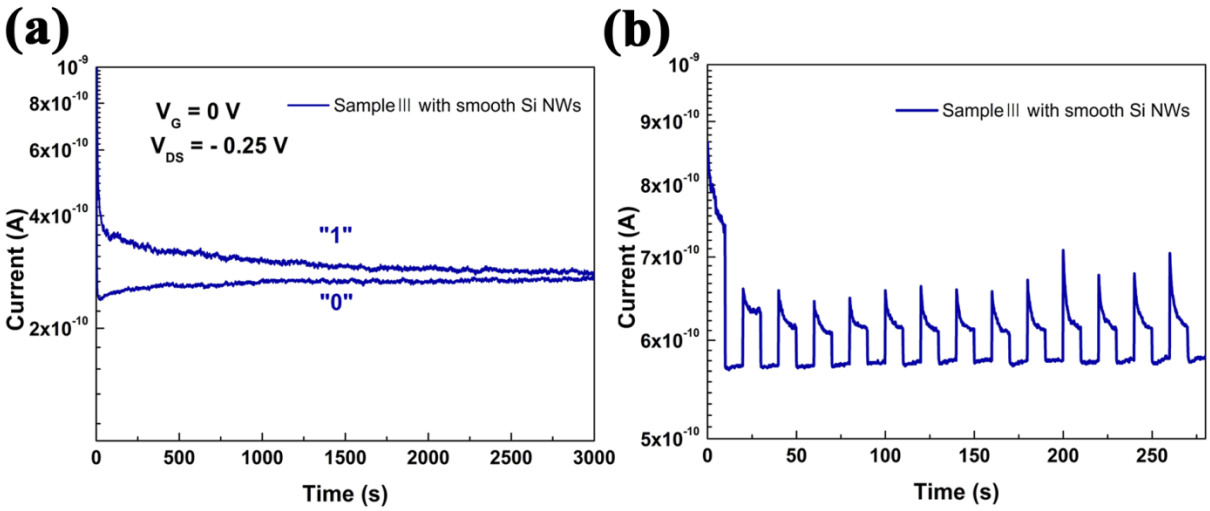

Figure S5. (a) Time dependent stability of conductance in the two states at Sample III with smooth Si NWs. The on-state "1" with a V_G of 40 V and off-state "0" was obtained with a V_G of –40 V for 1 s. (b) Memory operation, where writing and erasing were performed with 1 s gate pulsing of 40 V and –40 V, respectively. The currents of on and off states were read with V_{DS} = –0.25 V at V_G = 0 V during 10 s.

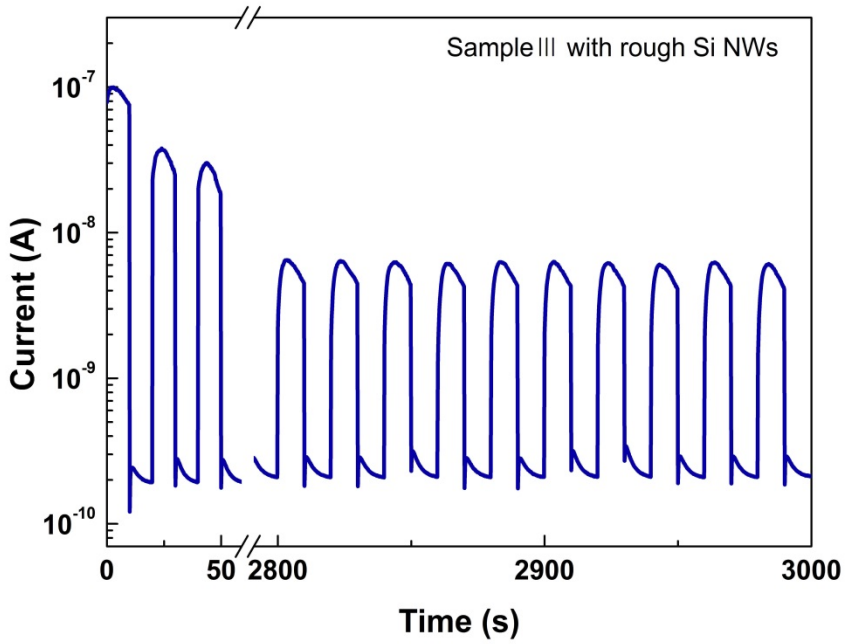

Figure S6. The duration of the on/off switching for 3000 times

References

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