Electronic Supplementary Information

Solution-grown single-crystalline microwires of a molecular semiconduc tor with improved charge transport properties

Akshaya K. Palai,[†]a Jihee Lee,[†]a Tae Joo Shin,^b Amit Kumar, ^a Seung-Un Park,^a Seungmoon Pyo^{*}a

^aDepartment of Chemistry, Konkuk University, 120 Neungdong-ro, Gwangjin-gu, Seoul 143-701, Republic of Korea

^bPohang Accelerator Laboratory, Pohang, 790-784, Republic of Korea.

*To whom correspondence should be addressed: S. M. Pyo (pyosm@konkuk.ac.kr), Tel: +82-2-450-3397, Fax:

+82-2-34365382

[†]These authors have contributed equally to this work

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Materials and Instruments: The compound 2,5-dihexadecyl-3,6-bis(5-(3-hexylthiophen-2-yl)pyrrolo[3,4-c]pyrrole-1,4(2H,5H)-dione, **DPP(3HT)**₂, was synthesized based on the procedure we reported earlier¹. All other reagents and chemicals used in this study were either purchased from Aldrich or from other local chemical companies as received.

Device performance characterization was performed in air conditions using an HP 4145B, function generator (RIGOR DG4062) and Oscilloscope (RIGOR DS2102). A surface profiler (AMBIOS XP-100) was used for the thin-film thickness measurement. Two-dimensional grazing incidence X-ray diffraction (2D-GIXD) experiments were conducted at PLS-II 9A U-SAXS beamline of Pohang Accelerator Laboratory in Korea. The incoming X-rays were monochromated (wavelength, $\lambda = 1.103$ Å) and the focused beam size at sample position was ~450 (H) x 60 (V) µm² (FWHM). The incidence angle of X-ray beam was set to a value in the range of 0.12° ~ 0.13°, which is close to the critical angle of **DPP(3HT)**₂. GIXD patterns were recorded using a 2D CCD detector (SX165, Rayonix L.L.C., USA). Diffraction angles were calibrated by a reference sucrose (Monoclinic, P21, *a* = 10.8631 Å, *b* = 8.7044 Å, *c* = 7.7624 Å, *b* = 102.938°)² and the sample-to-detector distance was about 230.9 mm.

OFET Fabrication and Characterization: Solution-processed OFETs on indium tin oxide (ITO)coated glass substrate and Si/SiO₂ were fabricated by using the procedure we reported earlier.³ The ITO substrate was patterned by photolithography and cleaned sequentially in an ultrasonic bath for 15 min with detergent, deionized water, acetone, and isopropyl alcohol, then dried at 60 °C in a drying oven and cleaned further with UV-ozone cleaner prior to use. The dielectric precursor solution was spun-cast over the ITO gate electrode and soft-baked at 90 °C for 10 min on a hot plate in air, and then hard-baked further at 175 °C in a vacuum oven (10^{-3} Torr) for 60 min to obtain a thin film. Microwires of **DPP(3HT)**₂ were grown by directly drop-casting its filtered (0.2 micron) *o*dichlorobenzene solution (0.1 wt%) using a glass capillary tube located in the substrated, followed by heating of the whole substrate at 90 °C for 1 h (Figure 1). The field effect mobility in the saturation regime was determined using the following equation:

$$I_{DS} = (W/2L)C_{i}\mu(V_{GS} - V_{th})^{2}....(1)$$

where C_i is the capacitance per unit area of the dielectric layer, and V_{th} is the threshold voltage. *L* and *W* are the channel length and effective channel width (depends on the width of the crystals) of the device, respectively.

Construction of the complementary inverter and characterization: Both **DPP(3HT)**₂ (as the *p*-channel) and PTCDI-C₈⁴ (as the *n*-channel) crystals were prepared using the abovementioned solution process and placed the crystals next to each layer on top of the ITO/CL-PVP substrate for the construction of complementary inverter. The organic inverter was completed by thermally evaporating 50 nm gold electrodes above the active layer using a shadow mask (L x W = 50 µm x 2000 µm and L x W = 50 µm x 1000 µm for the p- and n-channel OFET, respectively) forming the source and drain electrodes. The actual length and width (*W*) is calculated as the sum of the width of micro-crystals lying in the channel region and found to be L = 56 µm, W = 1165.9 µm for n-type crystals and L = 55 µm, W = 432.7 µm for p-type crystals. The **DPP(3HT)**₂ crystal-OFET was connected to the supply voltage (*V*_{DD}), while the PTCDI-C₈ crystal-OFET was connected to the ground, with the two transistors sharing an input (*V*_{IN}) and an output (*V*_{OUT}) terminal.

Gate	$DPP(3HT)_2$	Channel	Mobility	Ion/Ioff	V _{th}	SS	No. of	
Dielectric	(Wire or Film)	(L/W)(µm)	(cm ² /V.s)	ratio	(V)	(V/dec)	Devices	
Si/SiO ₂	Wire (2)	20/1.7	0.40	2.37×10^3	0.72	17.40	-	Best
		-	0.12	2.03×10^{3}	7.00	10.60	13	Average
	Wire (1)	20/0.5	0.15	9.25×10^{1}	7.70	5.50	-	Best
		-	0.11	3.07×10^2	7.80	7.00	03	Average
	Film ¹	50/1000	0.002	3.16×10^2	-40.20	10.00	10	Average
CL-PVP	Wire (4)	20/11	0.14	2.03×10^2	4.30	8.50	-	Best
		-	0.05	2.41×10^2	-9.80	21.20	23	Average
	Wire (1)	20/10.7	0.08	1.52×10^2	-15.20	20.50	-	Best
		-	0.04	$1.19 imes 10^2$	-12.90	26.30	04	Average
	Film ¹	50/1000	0.002	3.15 × 10 ²	-13.50	12.80	10	Average

Table S1 FET performance of devices based on wires and films¹ of **DPP(3HT)**₂ on various gate dielec trics. Numbers of the wires are shown in parentheses.



Fig. S1 The OM and AFM images of the DPP (3HT)₂ wires grown on Si/SiO₂ (a, b, and c, two crystal wires) and CL-PVP/ITO (d and e, 4 crystal wires) substrate.



Fig. S2 The (a and c) output ($I_{DS} - V_{DS}$) and (b and d) transfer ($I_{DS} - V_{GS}$) curves of the Si/SiO₂ gate die lectric OFETs with two wires (channel L/W = 20/1.7)(µm), and a single **DPP(3HT)**₂ wire (channel L/W = 20/0.5)(µm), respectively.



Fig. S3 (a) Output and (b) transfer characteristics of crystal-OFET based on four DPP(3HT)₂ microwires (channel L/W = 20/11)(µm) on CL-PVP gate dielectric.



Fig. S4 (a) Output and (b) transfer curves of the device kept in air for 65 days (based on four DPP(3HT)₂ microwires (channel L/W = 20/11)(µm) on CL-PVP gate dielectric).



Fig. S5 Enlarged schematic model of the molecule in Fig. 3b.



Fig. S6 The experimental *vs* simulated 2D-GIXD images of the **DPP(3HT)**₂ microwire showing good agreement and the best fit obtained with triclinic unit cell attributes: a = 30.06 Å, b = 10.89 Å, c = 5.06 Å, $\alpha = 79.3^{\circ}$, $\beta = 88.3^{\circ}$, and $\gamma = 88.7^{\circ}$



Fig. S7 Schematic diagram of the complementary inverter constructed by combining p-(22 **DPP(3HT)**₂ wires) and *n*-channel (74 PTCDI-C₈ wires) OFETs with CL-PVP gate dielectric (a). The OM image (b) and corresponding output (c) and transfer (d) characteristics of the *n*-channel OFET.

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