Electronic Supplementary Material (ESI) for Chemical Communications.
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Supplementary Information

Lateral growth of ZnO nanorods arrays in polyhedral structures for high on-current field-effect transistors

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METHODS

Lateral growth of ZnO nanorods arrays and fabrication of polyhedral-type FETs. Figure S1 represents the typical fabrication processes of a circle-type FET with lateral growth of ZnO NRs. The fabrication processes consist of four steps that we developed for the fabrication of laterally grown ZnO NRs FETs:[1] 1) photoresist (PR) patterning of polyhedral shapes on ZnO seed layer on p-Si/SiO_2(300 nm) using conventional lithography and etching (a-d), 2) selective lateral growth of ZnO NRs in solution followed by removing of PR (e and f), 3) PR patterning on the laterally-grown ZnO NRs for source-drain metal deposition (g), and 4) metallization and lift-off, deposition of back-gate metal and passivation with (poly)methylmetahacrylate (PMMA) (h-i). The PMMA passivation layer was made by spin-casting at 4,000 rpm, followed by soft-baking in oven at 90 ℃ for 5 min. The ZnO seed layer having a thickness of 50 nm was deposited on the p-Si/SiO_2 by radio-frequency sputtering using a ZnO target (99.99 % purity). For the standard lithography patterning, a positive photoresist (AZ5214) with a thickness of 1.2 μm was spun on the p-Si/SiO_2/ZnO substrate. The patterning of the ZnO seed layer was then carried out with inductively coupled plasma (ICP) discharges of H_2 at 5 mTorr, 600 W ICP source power and 30 W rf chuck power for 90 s. Next, the lateral growth of ZnO NRs on the pre-patterned p-Si/SiO_2/ZnO was performed in solution by using zinc nitrate hexahydrate (ZNH; $Zn(NO_3)_2{\cdot}xH_2O$), hexamethylenetetramine (HMTA; $C_6H_{12}N_4$) and polyethyleneimine (PEI; $(C_2H_5N)_n$). All the regents used in this synthesis were of analytical grade and used as-received without further purification. In a typical reaction process, an equimolar ratio (0.01 M) of ZNH and HMTA solution was prepared in 100 mL of deionized water (Milli Q 18.2 MΩ cm) and then ~$1x10^{-3}$ mM PEI was added in the same solution under stirring, and the synthesis was carried out at 85 ^oC. Details of the lateral growth of ZnO NRs are available elsewhere.[2-5] It was reported that the threshold voltage of ZnO NRs FET is affected by the NR diameter without any significant changes of subthreshold swing, carrier concentration and on/off ratio.[6] In this work, we optimized the diameter of ZnO NR to ~200 nm. After the lateral growth of ZnO NRs, PR was removed by a lift-off process with acetone. For the deposition of source and drain electrodes, a negative PR (thickness ~1.2 μm) was spun selectively on the top of the laterally-grown ZnO NRs, followed by the deposition of Ti(30nm)/Au(120nm) by using an electron-beam evaporator (KVE-C25096). After the metal deposition, source and drain electrodes were formed by removing the PR with a lift-off process in acetone. It is worthwhile to note that the source and drain electrodes were deposited on ZnO nanorods after they were laterally grown between source and drain (see FiguresS1, e-h). Further to ensure an ohmic contact, as shown in FESEM images of polyhedral type FETs in Figures 1-3 (i.e., dotted lines),

about 3 μm of ZnO nanorod in source side was coated with Ti/Au. Finally, the back-gate of Ti(30nm)/Au(120nm) was deposited under a p-Si substrate by the electron-beam evaporator. All the FETs were annealed at 350℃ under H_2 flow, followed by passivation with PMMA.

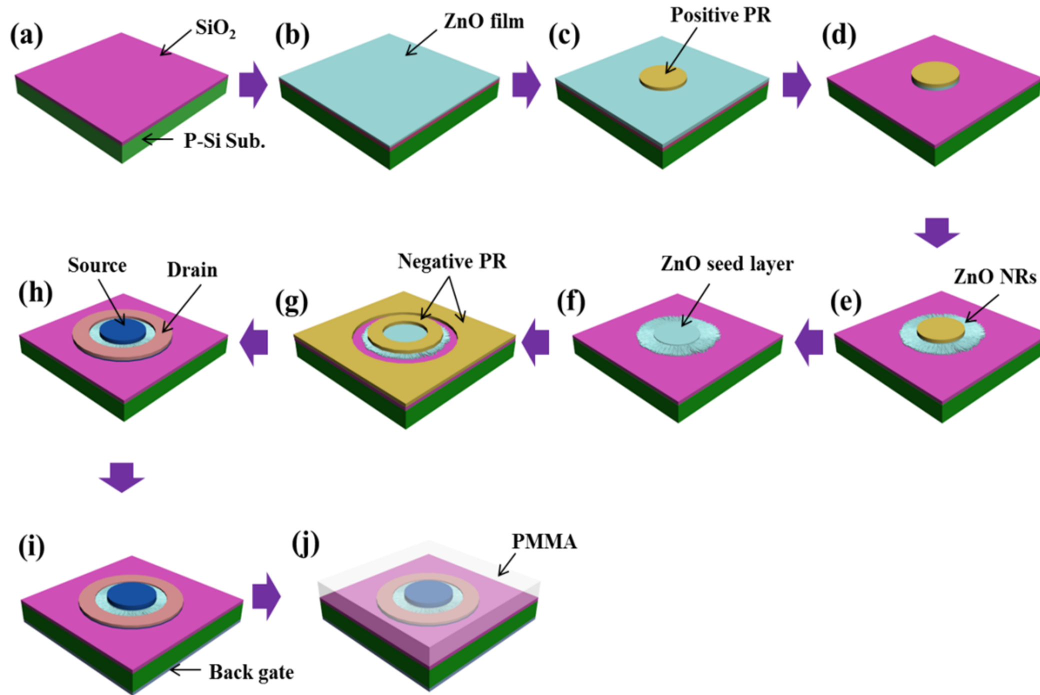

Figure S1. Schematic illustration of fabrication processes of circle-type FETs based on laterally-grown ZnO NR.

Characterization. Structural characterizations of the as-grown ZnO NRs and PH-FETs were performed using field-effect scanning electron microscopy (FESEM), transmission electron microscopy (TEM) and selected-area electron diffraction (SAED) system. The device performances of the PH-FETs were examined by measuring the source-drain current versus source-drain voltage (I_{DS}-V_{DS}) and source-drain current versus source-gate voltage (I_{DS}-V_{GS}). The electrical measurements were performed using a four probe station (HP 4156C semiconductor parameter analyzer) in the range from 20 fA to 100 mA at room temperature. To extract the threshold voltage from the I_{DS}-V_{GS} measurements, the constant-current method was used.

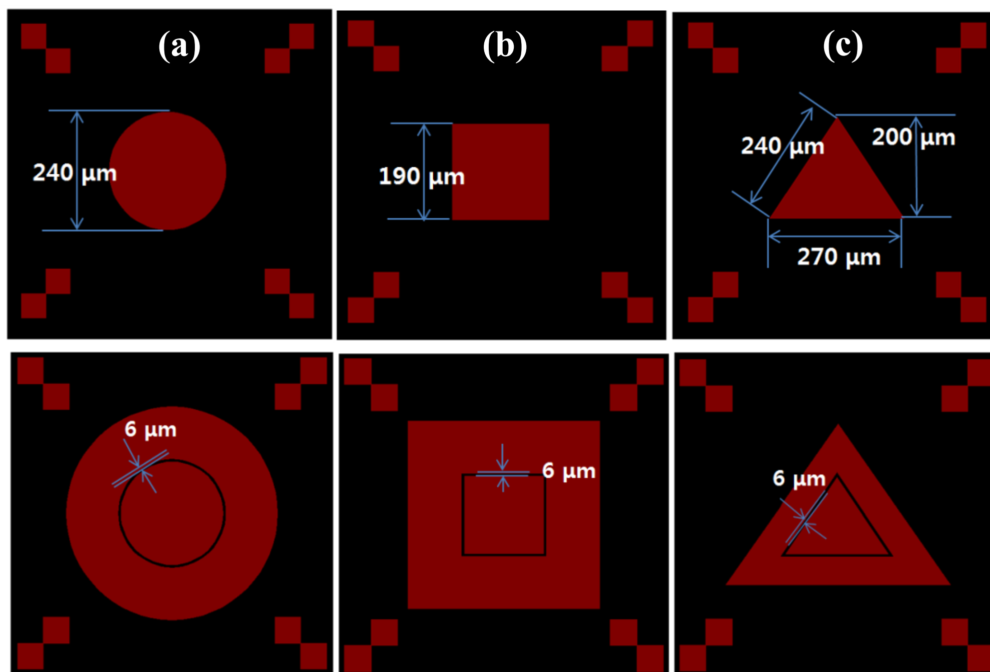

Figure S2. Low (top) and high magnification dimension of (a) circle-, (b) square- and (c) triangle-type FETs.

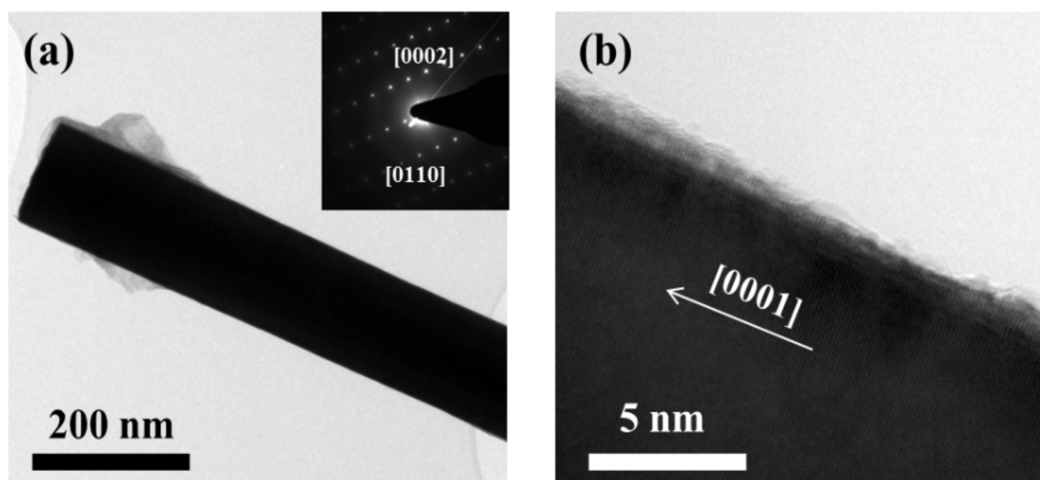

Figure S3. (a) TEM image with SAED pattern and (b) HRTEM of single ZnO nanorod.

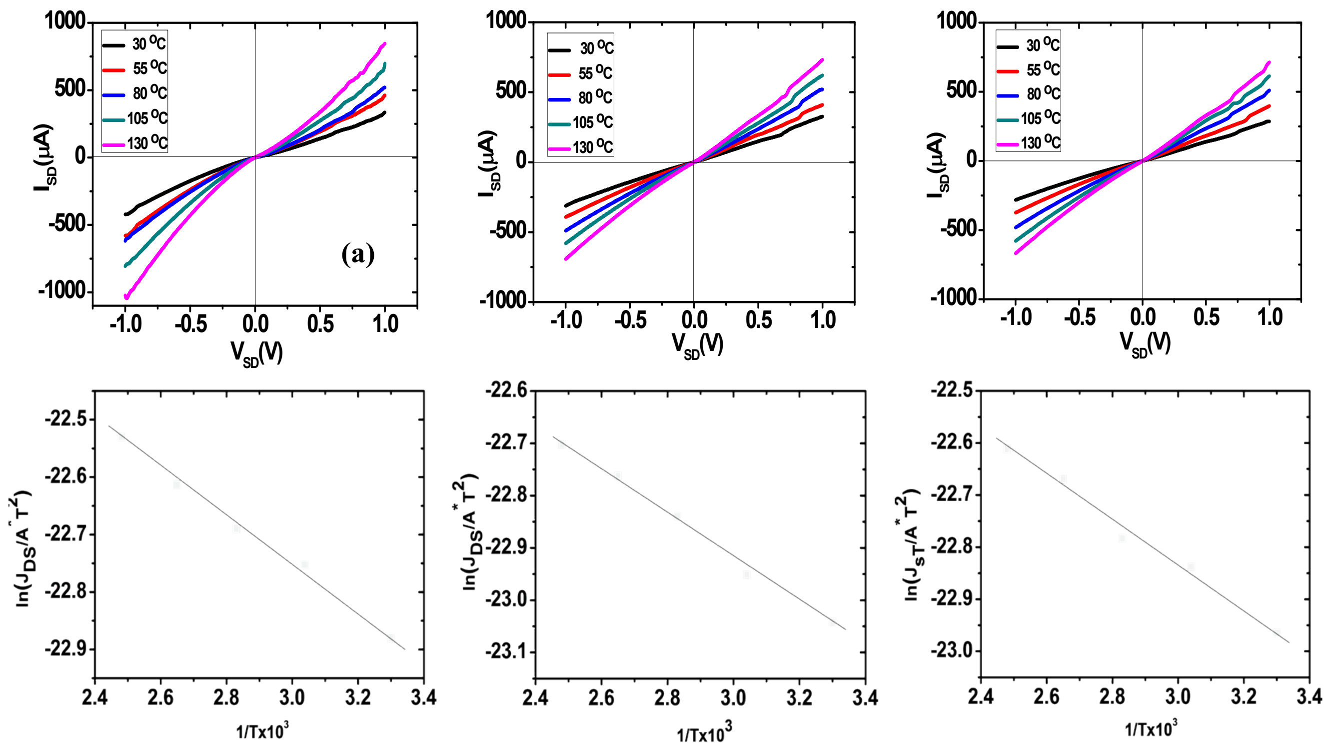

Figure S4. Temperature dependency of I_{DS}-V_{DS} and plots of ln (J_{DS}/A^*T^2) *vs*. $1/T$: (a, b) circle-, (c, d) square-, and (e, f) triangle-type ZnO NRs FETs.

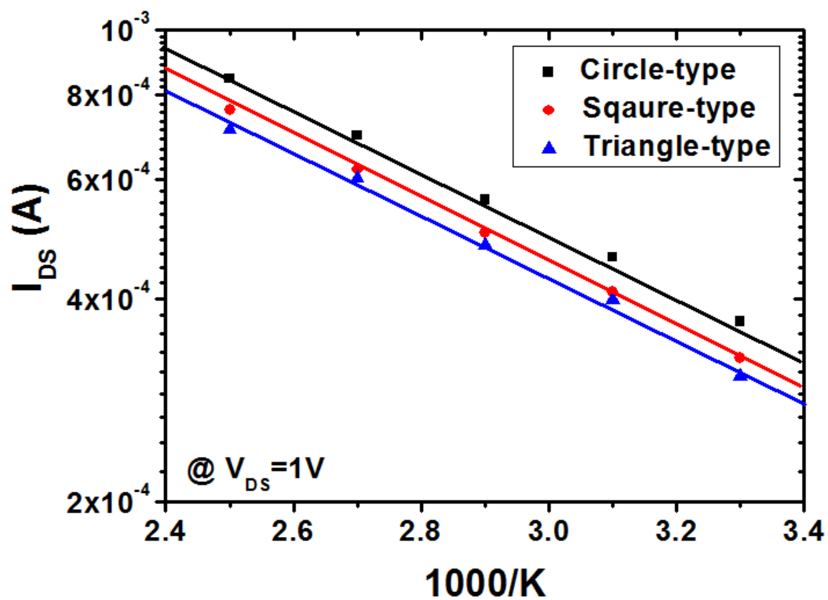

Figure S5. Arrhenius plots of ln I_{DS} *vs*. $1/T$.

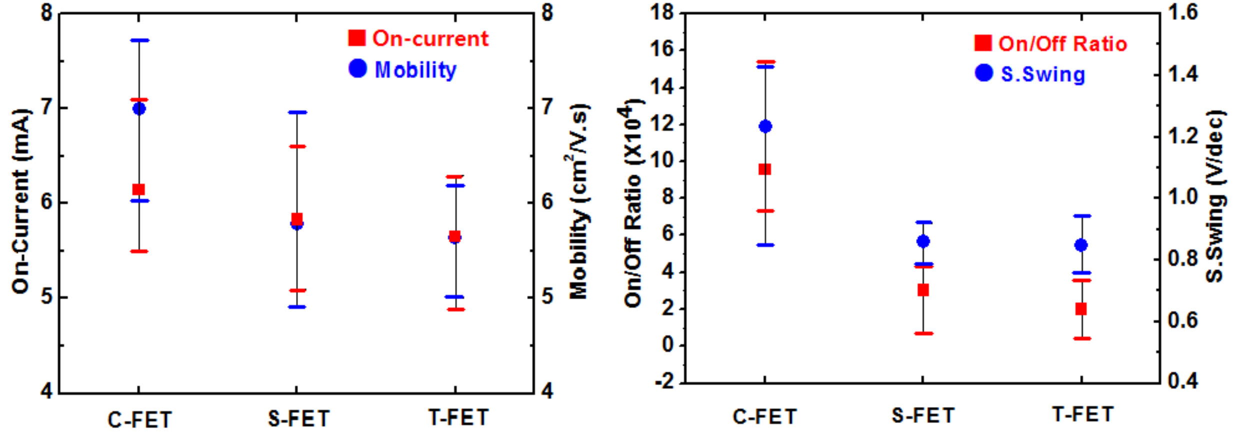

Figure S6. Statistic plots of on-current and effective mobility (left) and on/off ratio and sub-threshold swing (right) measured from nine devices respectively for circle-, square- and triangle-type FETs.

Table S1. Device parameters of polyhedral type FETs based on laterally-grown ZnO nanorods.

FET type	Channel length/width* (μm/μm)	Mobility (cm^2/Vs) at V_{DS}=3V	Trans-conductance g_m (μS)	Carrier conc. (cm^{-3})	On/off ratio	Threshold voltage (V)
Circle	6/754	7.82	32.0	8.2 x 10^{17}	1.6 x 10^5	+8
Square	6/760	5.72	25.0	7.1 x 10^{17}	1.8 x 10^4	+5
Triangle	6/750	5.63	20.0	6.5 x 10^{17}	4.5 x 10^3	+6

* Width is defined as the perimeter of a polyhedral structure.

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