

COMMUNICATION

Electronic Supplementary information (ESI)

Crystallization of rubrene on nanopillar-templated surface by melt-process and its application in field effect transistor

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Experimental section

Fabrication of nanopillar array:

The nanopillars array is defined by nanosphere lithography and metal assisted chemical etching. The 2D colloidal crystal served as mask was obtained from the assembly of polystyrene (PS) colloids at air/water interface according to literature procedure.¹ The 2D colloidal crystal was transfer onto a heavily-doped p-typed silicon wafer, followed by oxygen plasma (50 walt, 50 mtorr of O₂, and flow rate of 20sccm, Plasma Lab) etching to reduce the dimension of the PS colloids. A 40-nm-thick gold was deposited on the PS colloids array using E-gun evaporation to serve as catalytic layer for etching of underlying silicon substrate. The nanopillar array was formed by immersing the wafer to a mixture solution (H₂O: H₂O₂ 35%: HF 48%=50: 1: 9 by volume) for 8min. The redundant gold layer and PS sphere were removed by aqua regia and piranha solution. Excess ions and chemicals were further removed by deionized water (18.2 MΩ-cm, Millipore) rinsing for several times. The wafer patterned by nanopillars array was sliced to 7mm x 7mm squares. The oxide layer on nanopillar array was grown by a typical thermal process at around 1000°C in quartz tube furnace under a dried atmosphere.

Fabrication of SiO_x layer and source electrodes:

To prevent gold cluster from adhering to the sidewalls of nanopillars, which may produce undesired conductivity or electron traps, a SiO_x hat was decorated on the top of each nanopillar. The wafer with nanopillars was mounted on a tilted (θ~15°) and rotating stage (60 rpm). The scheme and cross-sectional images are presented in Fig S1(1). The source electrodes composed of Cr/Au (3/60nm) were evaporated through a shadow mask with a width of 800 or 100 μm, as illustrated in FigS1(2).

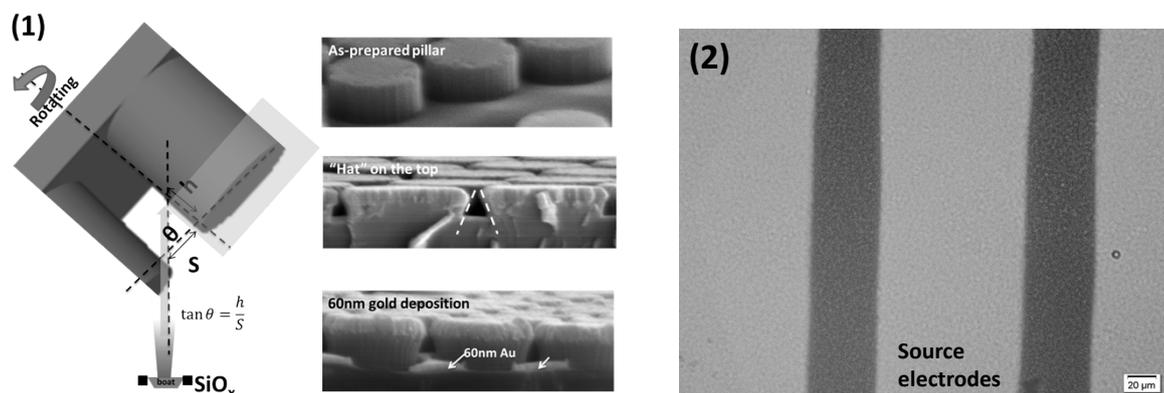


Figure S1. (1) Scheme and SEM images for depositon of SiO_x layer on the top of nanopsgere (2) Source electrodes at the bottom of nanopillar array.

Fabrication of rubrene/nanopillars hybrids and drain electrodes:

Rubrene (99.99%) purchased from Sigma Alderich was dissolved in toluene (J.T. Baker) to saturation. The rubrene solution (50 μ l-150 μ l) was carefully dropped onto nanopillar sample, originally kept at 90 °C, using a micropipette. After the removal of toluene, the morphologies of dried rubrene on planar and nanostructured surface are compared in Fig S2(1) and S2(2). The rubrene solidified on nanopillar surface were seen to give dendritic branches and more uniformly distributed than that on planar surface. The samples were quickly heated to 310~320°C to reach melting. The melted rubrene quickly spread over the sample surface. Cooling at a rate of 35°C/min resulted in crystallization. Aluminum layer serving as drain electrodes were evaporated on rubrene crystal/nanopillar hybrids through a shadow mask (slit width=800 or 100 μ m) that was orthogonal to source electrodes, as illustrated in Fig S2(3).

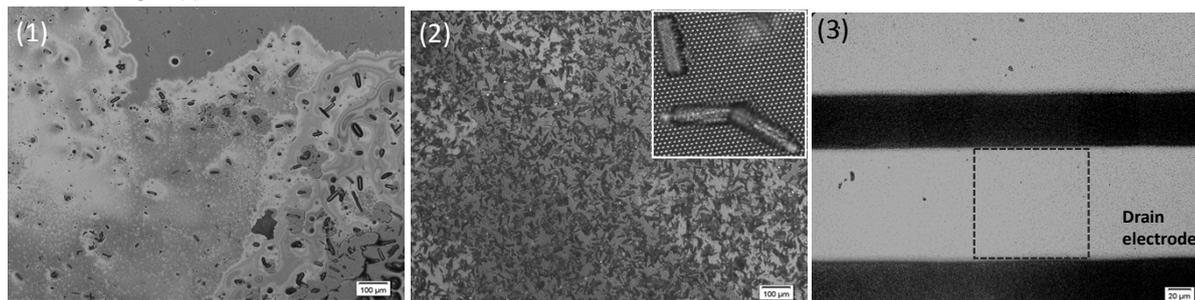


Figure S2. Rubrene dried on (1) planar wafer surface and (2) nanopillar-templated surface before melting. Inset is the magnified image. (3) Al drain electrode. The intersection, marked by dotted line, is the active area.

Fabrication of conventional FET with nanopillar-templated rubrene films

The conventional OFET was fabricated on ODTS-modified nanopillar substrate with thick rubrene film. The device was prepared by depositing source/drain electrodes (Cr/Au = 3/80nm), $L/W = 80/1800\mu\text{m}$, followed by chemical vapor deposition of parylene (~800nm) and then Al gate of (~200nm), shown in Fig S3(1). The mobility of conventional OFET can be extracted from I_D-V_G measurements.

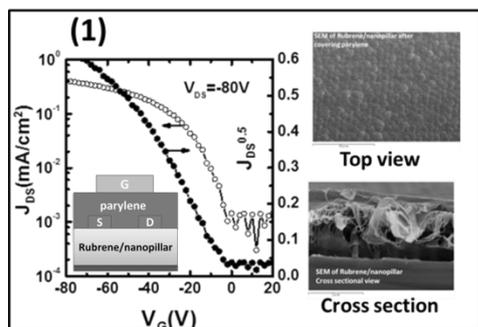


Figure S3 (1) Layout and performance of conventional on nanopillar-templated rubrene film

1. Wu, K.-Y.; Tao, Y.-T.; Ho, C.-C.; Lee, W.-L.; Perng, T.-P., *Applied Physics Letters* 2011, **99**, -.