Electronic Supplementary Material (ESI) for Physical Chemistry Chemical Physics.

Supplementary Information for:

Solution-processed N-type Fullerene Field-Effect Transistors Prepared Using CVD-grown Graphene Electrodes: Improving Performance with Thermal Annealing

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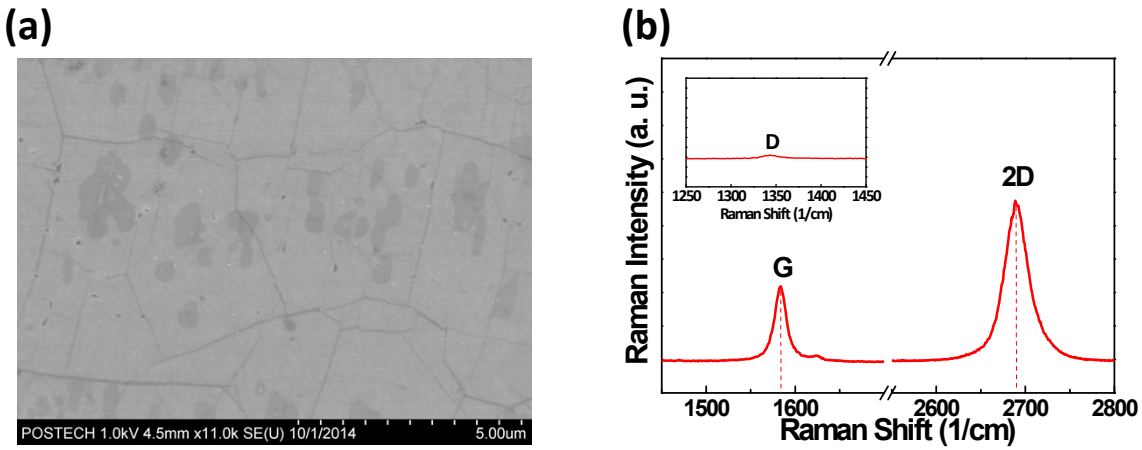


Figure S1. (a) Scanning electron microscopy image and (b) Raman spectra of graphene electrodes for OFETs, respectively.

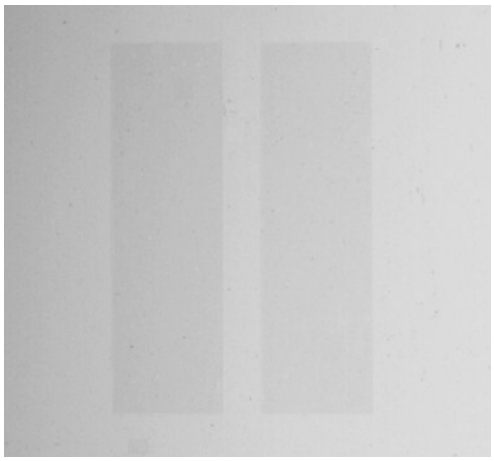


Figure S2. Optical microscopy image of patterned graphene electrodes for OFETs (without contact pad).

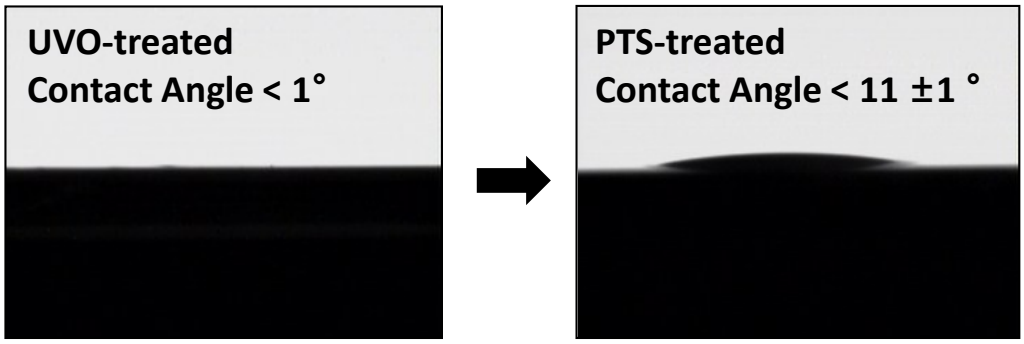


Figure S3. Optical images of the seeding dichlorobenzene droplet on the UVO- and PTS-treated SiO_2/Si substrates.

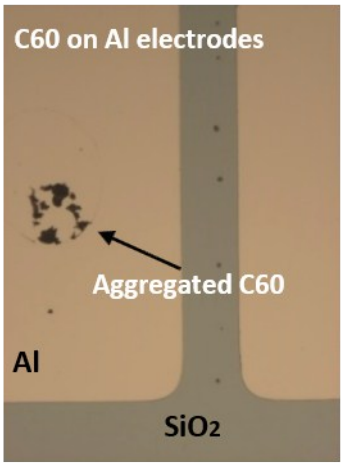


Figure S4. Optical microscopy images of the aggregated C_{60} on aluminum electrodes.

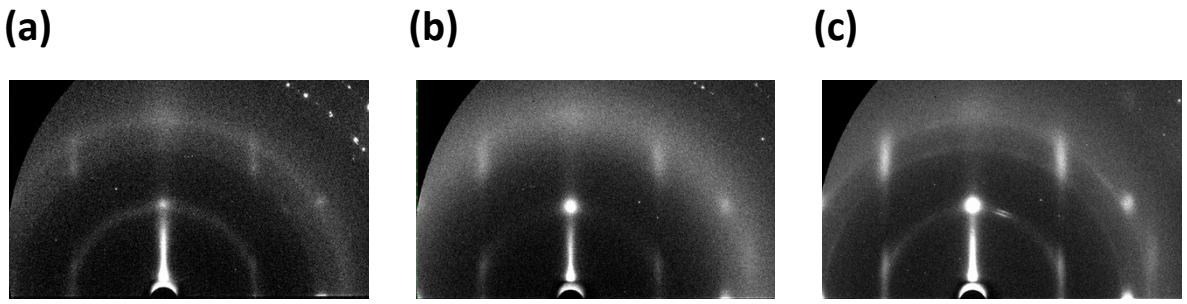
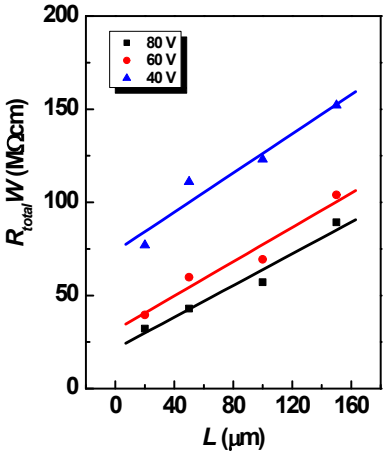
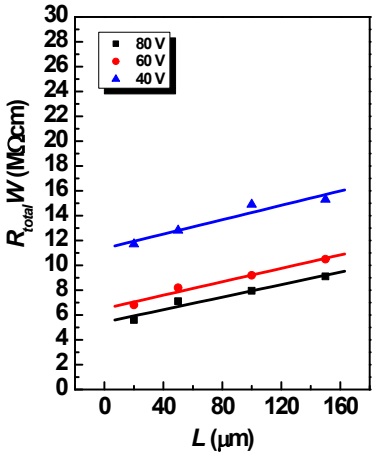


Figure S5. 2D-GIXD patterns of the thermally annealed C_{60} films on graphene at (a) 50 °C, (b) 90 °C, and (c) 130 °C

1) 50 ℃-annealed C_{60} FET



2) 90 ℃-annealed C_{60} FET



3) 130 ℃-annealed C_{60} FET

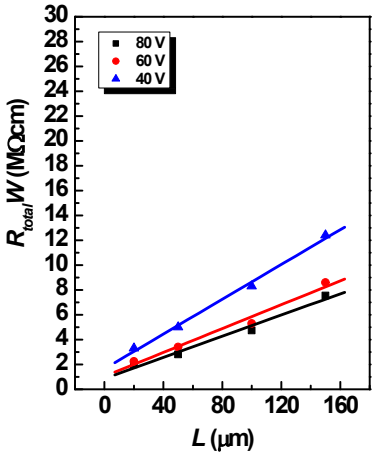


Figure S6. Width-normalized total resistance ($R_{total}W$) for the C_{60} FETs annealed at three different T_A (50, 90 and 130 °C) as a function of the gate voltages.