Electronic Supplementary Material (ESI) for Physical Chemistry Chemical Physics.

Supporting Information

Understanding Molecular Surface Doping of Large Bandgap Organic Semiconductors and Overcoming the Contact/Access Resistance in Organic Filed-Effect Transistors

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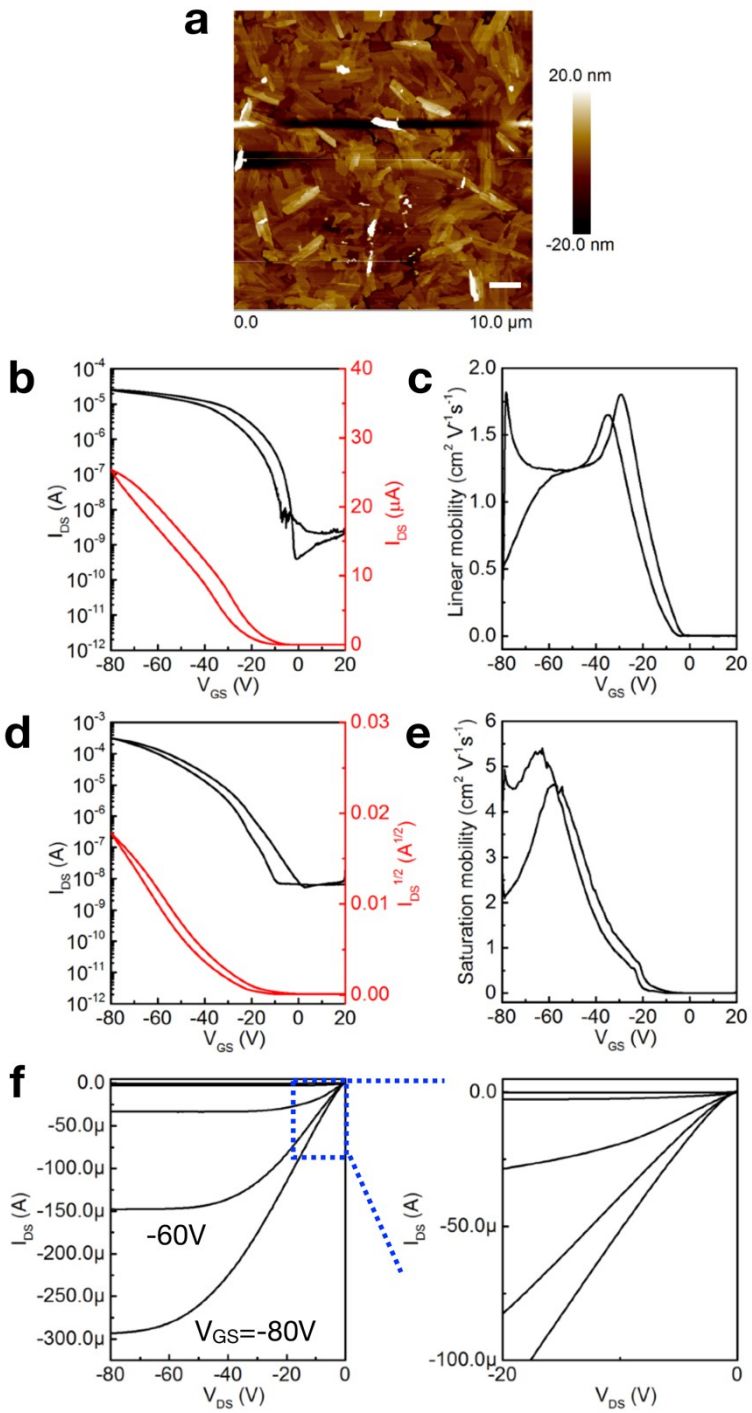

Fig. S1. The 10 nm F_4-TCNQ surface doped C_8-BTBT transistor. (a) AFM morphology of the doped thin film. (b) Transfer curve in the linear region and (c) corresponding gate dependence on the linear mobility, V_{DS} = –5 V. (d) Transfer curve in the saturation regime and (e) corresponding gate dependence on the saturation mobility, V_{DS} = –80 V. (f) Output curve, right side is the zoom-in curves at small V_{DS} region.

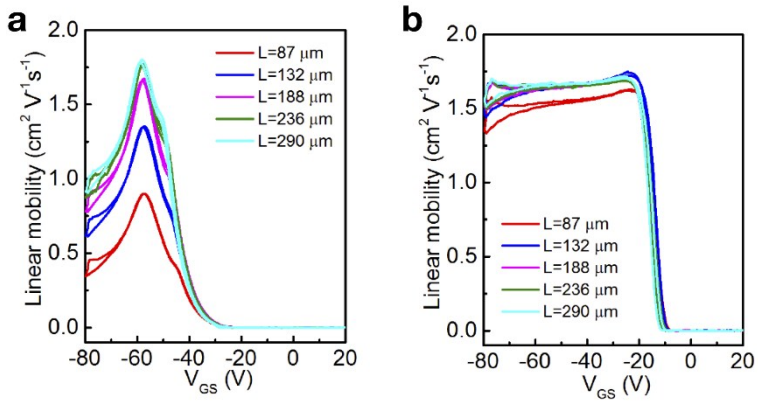

Fig. S2. (a) Gate dependence on the linear mobility of pristine C_8-BTBT transistors at various channel lengths. (b) Gate dependence on the linear mobility of surface doped C_8-BTBT transistors at various channel lengths.

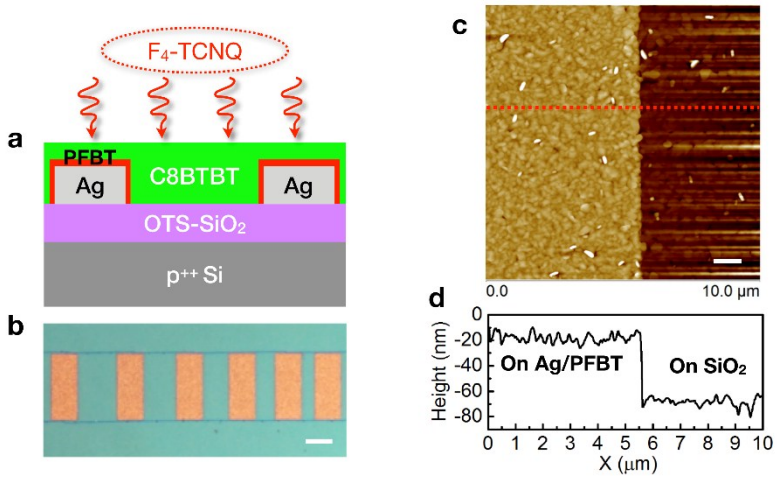

Fig. S3. (a) Schematic drawing of a BGBC C_8-BTBT transistor with F_4-TCNQ surface doping. (b) Optical image of a set of surface doped transistors with various channel lengths in TLM measurement, the scale bar is 200 μm. (c) AFM image of surface doped C_8-BTBT film grown on the PFBT-treated Ag and OTS-treated SiO_2 surface, the scale bar is 1 μm. (d) Corresponding height profile of the C_8-BTBT film along the red dash line in (c). The scale bar is 200 μm.

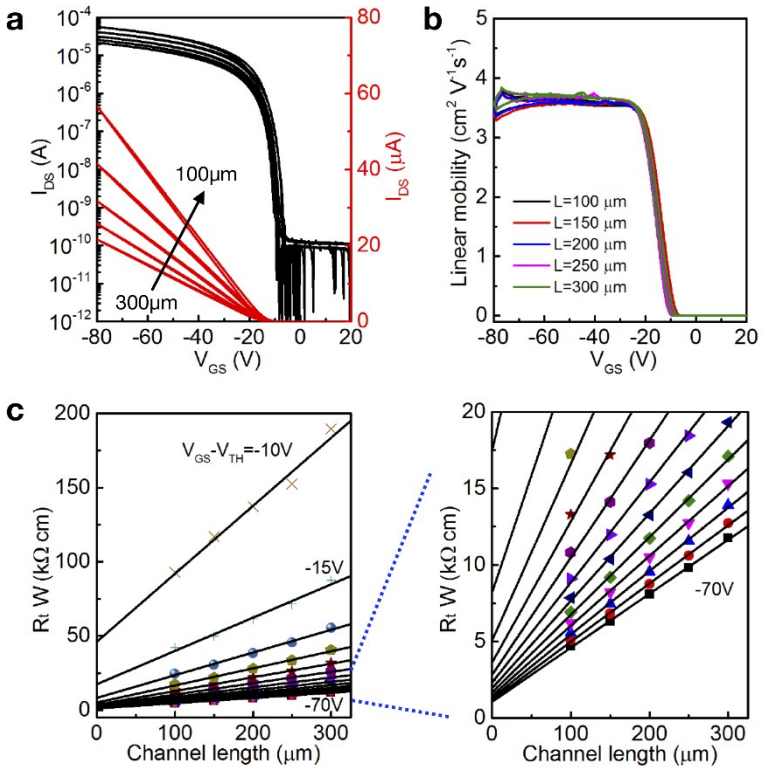

Fig. S4. (a) The linear transfer curves of the co-planar devices with various channel lengths in the TLM measurement, V_{DS} = –5 V. (b) Linear carrier mobility versus gate bias. (c) Device total resistance versus channel length at various gate bias levels. Right hand side is the zoom-in plot at the intercept to show the contact resistance of 1.1 kΩ cm.

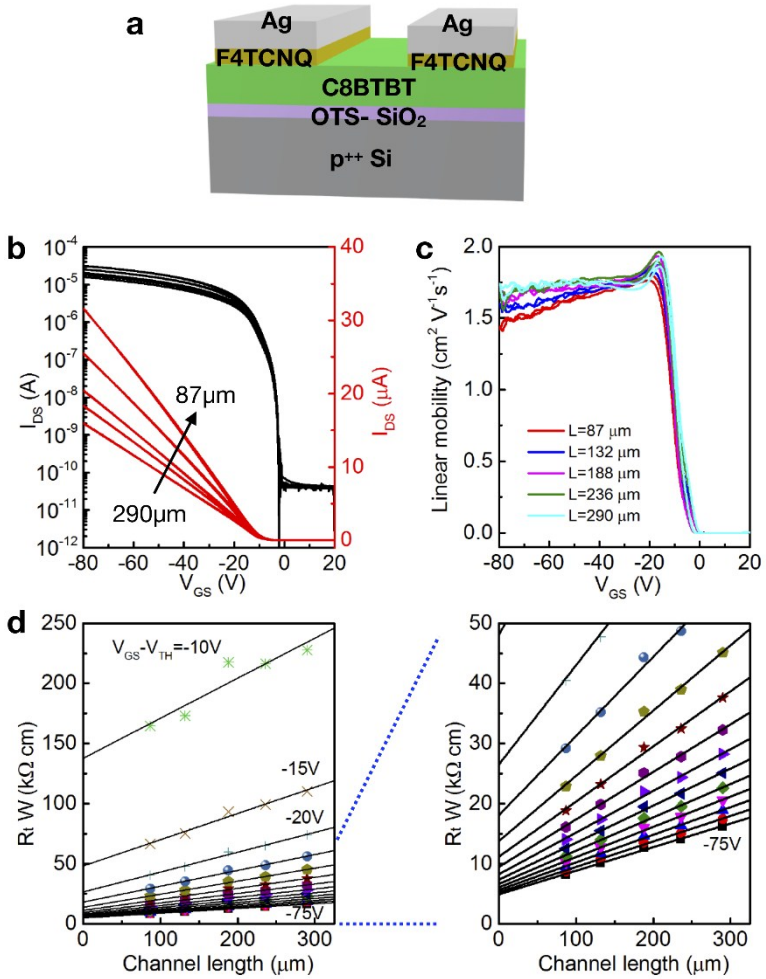

Fig. S5. (a) Schematic drawing of a F_4-TCNQ contact doped C_8-BTBT transistor. (b) The linear transfer curves in the TLM measurement, $V_{DS} = -5$ V. (c) Linear mobility versus gate voltage. (d) Total resistance versus channel length at various gate bias levels, right side is the zoom-in plot at the intercept to show the contact resistance of 4.9 kΩ cm.

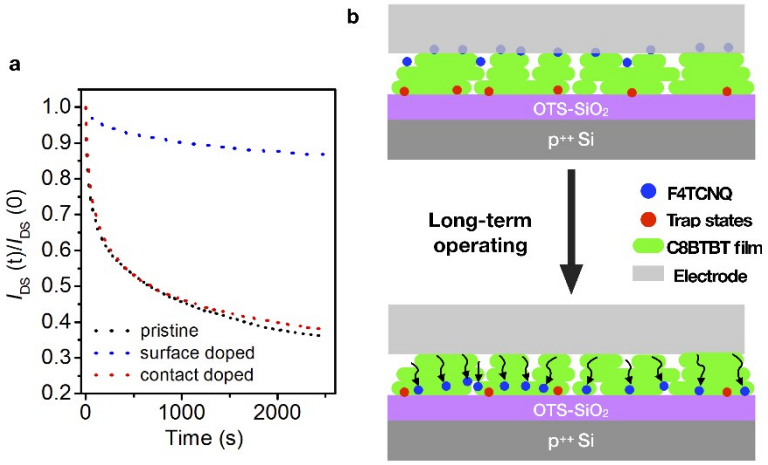

Fig. S6. (a) Bias stress performance of the pristine and doped C_8-BTBT transistor, $V_{GS} = V_{DS} =$ –80 V. (b) Illustration of the proposed decay mechanism of the contact doped transistor under bias.

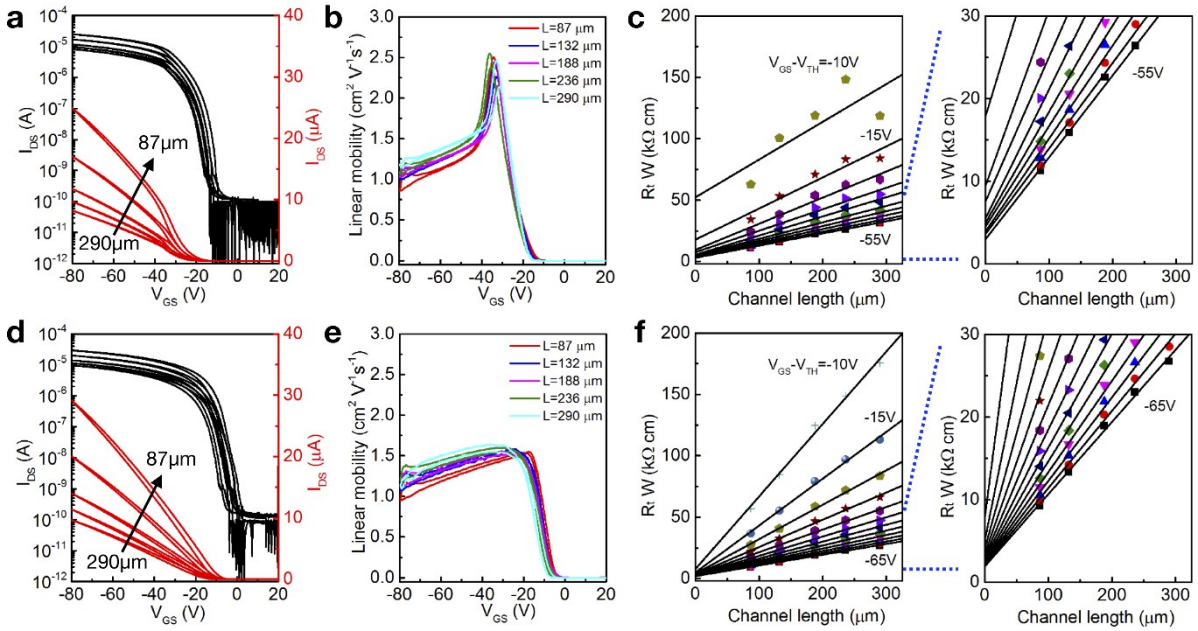

Fig. S7. The pristine DNTT device performance. (a) The linear transfer curves in the TLM measurement, V_{DS} = –5 V. (b) Linear mobility versus gate bias. (c) Total resistance versus channel length at various gate bias levels. The corresponding curves of surface doped DNTT device are shown in (d), (e) and (f). The zoom-in plots at the intercept show the contact resistance of 3.0 kΩ cm and 1.9 kΩ cm in the pristine and surface doped DNTT device, respectively. Moreover, the mobility of the surface doped device shows very small gate dependence, while the mobility of the pristine device decreases sharply near the V_{TH} region, which may result in a mobility overestimation due to gated Schottky contacts.

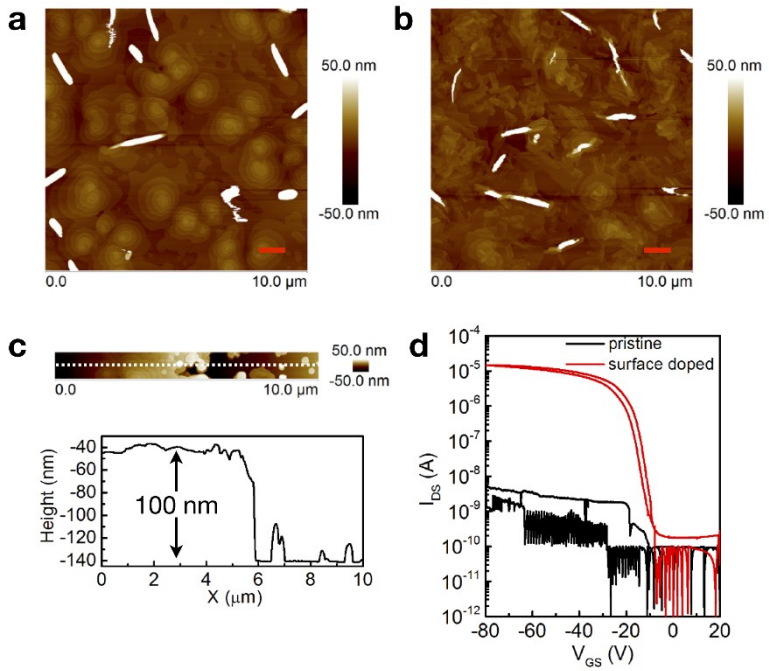

Fig. S8. Surface doping effect on thicker C_8-BTBT thin film based devices with large access resistance. AFM images of 100 nm thick (a) pristine C_8-BTBT thin film and (b) surface doped C_8-BTBT thin film. (c) Height profile of the scratched C_8-BTBT film which confirms the film thickness of 100 nm. (d) The transfer curves in the linear region, $V_{DS} = -5$ V. The scale bars are 1 μm.

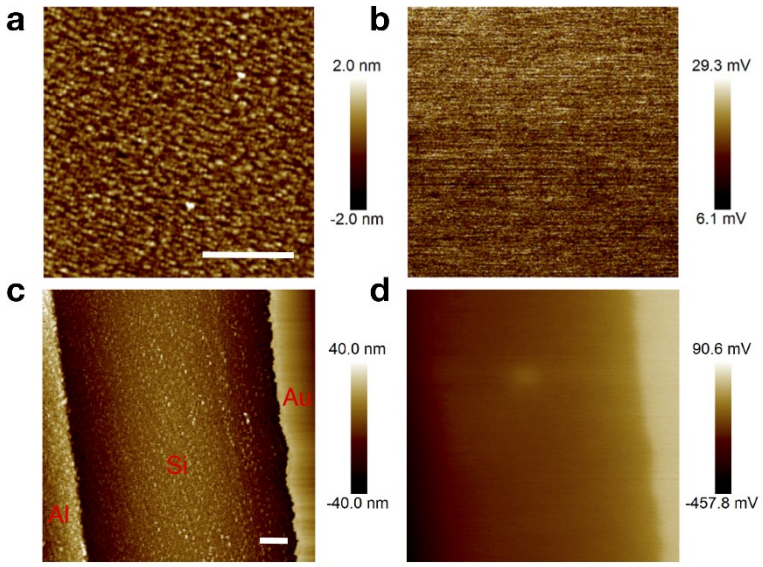

Fig. S9. KPFM calibration of the WF_{tip} on standard Al/Si/Au sample surface provides by Bruker. (a) Morphology image and (b) corresponding KPFM image of standard Au thin film surface; (c) Morphology image and (d) corresponding KPFM image of patterned Al and Au thin films on Si surface. All scale bars are 1 μm.

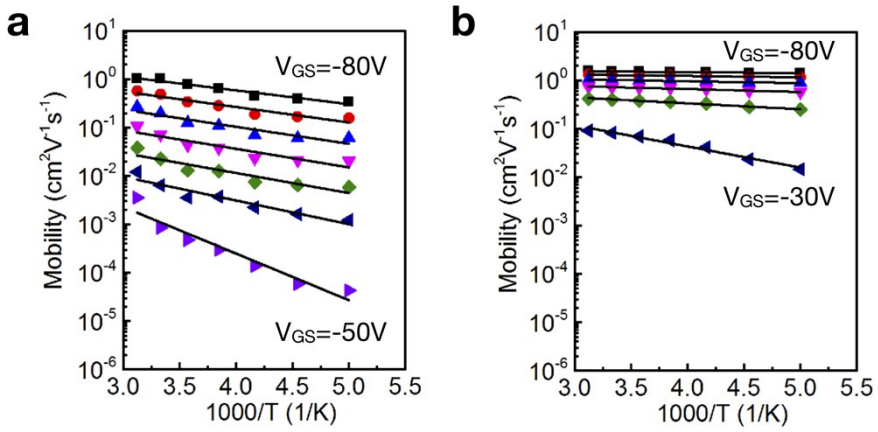

Fig. S10. (a) and (b) linear mobility versus 1000/*T* for pristine and surface doped device, respectively.

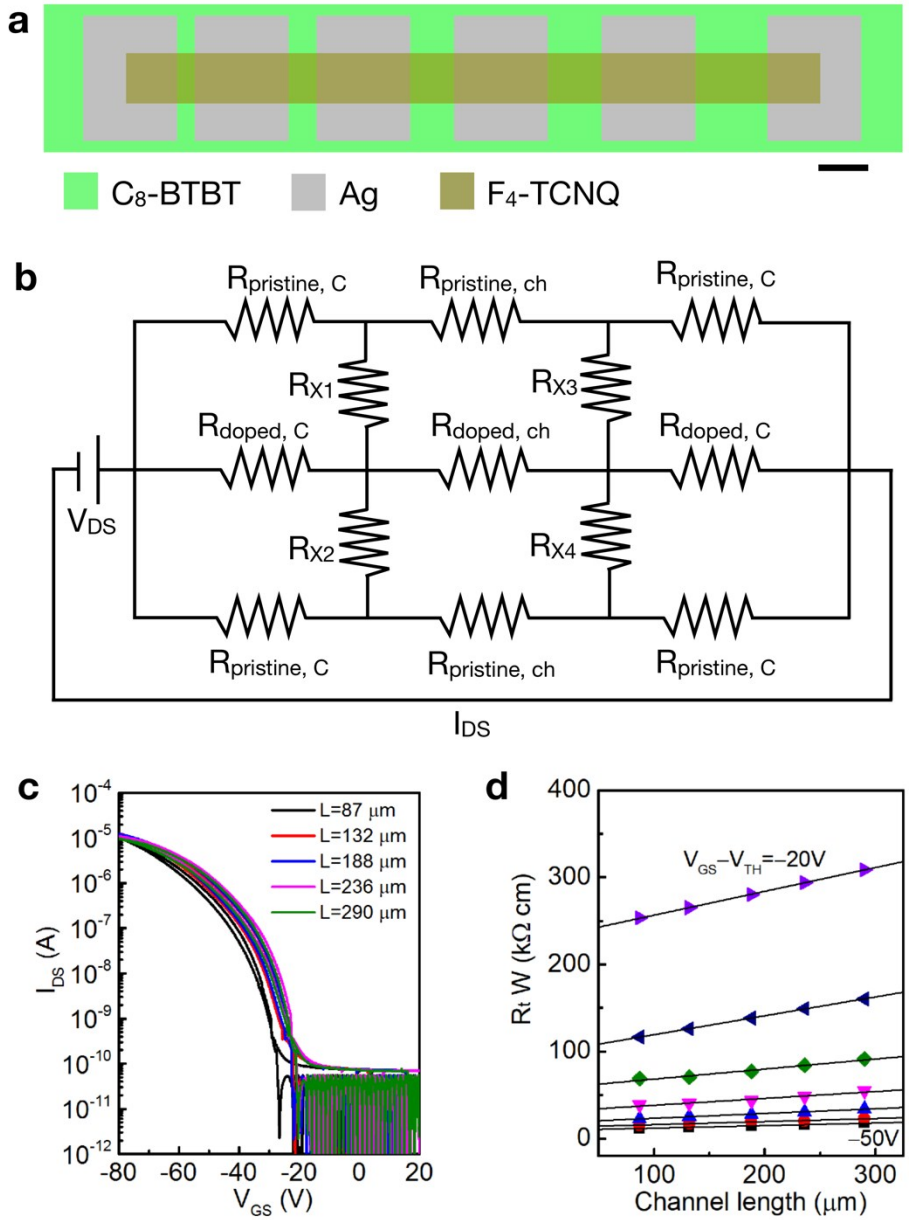

Fig. S11 Partial doping of the C_8-BTBT device. (a) The schematic illustration of partially surface doped transistors for TLM measurement on Si/SiO_2 substrate. The scale bar is 200 μm. (b) The equivalent circuit diagram of the partially doped device. (c) Linear transfer curves of partially surface doped devices in TLM measurement, $V_{DS} = -5$ V. (d) Total resistance of partially surface doped device as a function of channel length at various gate bias levels.

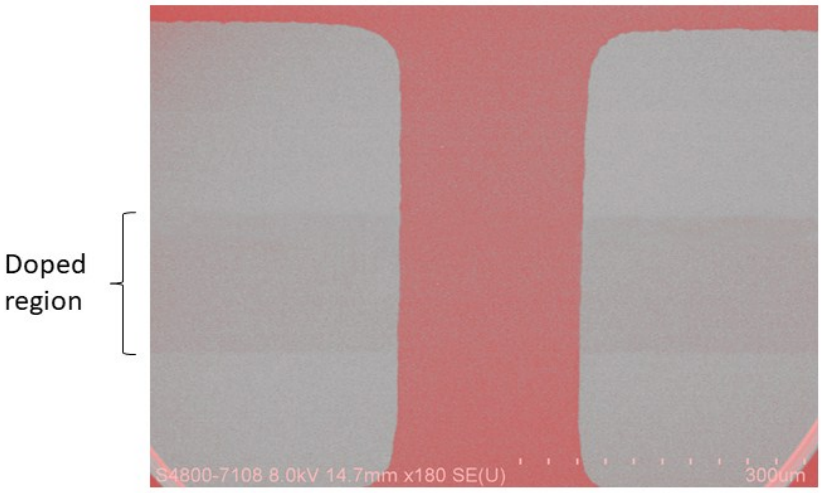

Fig. S12. The false colored SEM image of partially surface doped device. The surface doped region was marked by the left brace.