Supporting information

Saturation profile based conformality analysis for atomic layer deposition: aluminum oxide in lateral high-aspect-ratio channels

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1. Supporting information to Experimental details

Figure S1 shows the PillarHall-3 chip layout design with rectangular channels on a silicon substrate. A top polysilicon membrane was supported by silicon pillars (Figure S1 b and c). The main test area consists of nine different LHAR channels (and six of VHAR type). The LHAR channels in the main test area are mirrored [Figure S1a (2)], while the largest LHAR channel with the lateral length L of 5000 µm is one-sided [Figure S1a (3)]. On the edges of the chip, additional eight LHAR channels are arranged, which open up in different directions.

Each LHAR channel has a different opening width W (Table S1) before the channel entry (i) to recognize the individual channel e.g. in cross sectional scanning electron microscopy

and (ii) to use opening widths as a length scale indicator in top-view analysis. The opening is sufficiently wide ($W >> H$) to not limit the film growth.

The PillarHall-3 conformality test chips contain LHAR channels with four different pillar arrays: layouts v1a, v1b, v2a, and v2b, as presented in Figure S3. Pillars are located in hexagonal symmetry with different pillar inter-distance a, pillar diameter d, and distance between rows of pillars l depending on the layout (Table S2). Layout v1b is the standard design, with a = 49 µm, d = 4 µm, and l = 42.4 µm. The lateral distance l is calculated as $\frac{\sqrt{3}}{2}a$.The pillars at the channel entry are elongated in all designs.

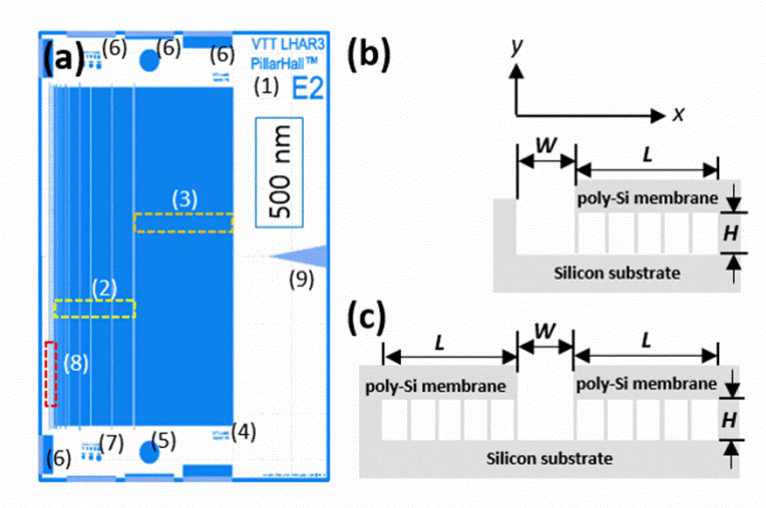

Figure S1 (a) Top view layout of PillarHall-3 having microscopic LHAR channels: (1) chip number, (2) LHAR channels in the main test area, (3) the largest LHAR test feature, (4) pillar layout indicator, (5) channel height indicator (silicon oxide between silicon and polysilicon), (6) additional LHAR channels (located symmetrically on top and bottom of the chip), (7) polysilicon tensile stress test circles, (8) VHAR channels, and (9) cleaving notch. Panels (b)-(c) are schematic side views of rectangular LHAR channels with x and y directions, not in drawn scale.

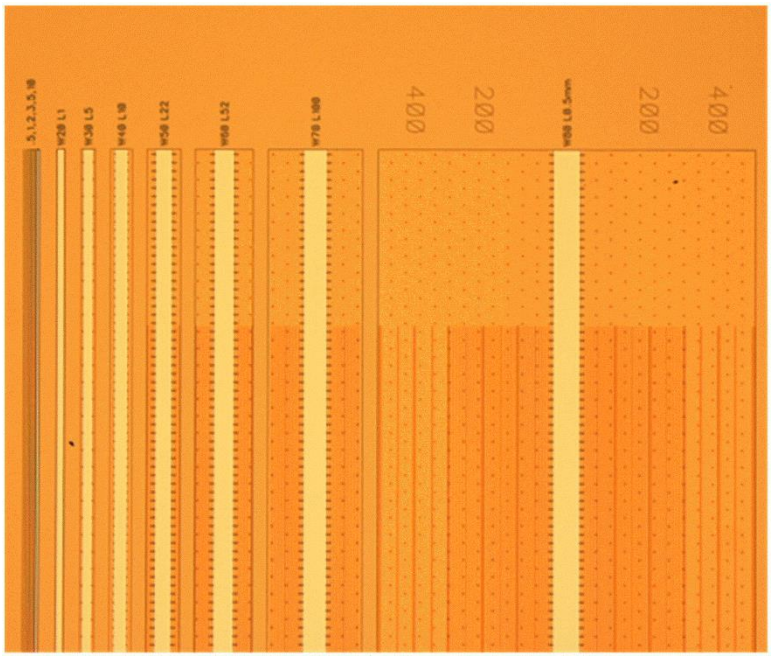

Figure S2. Optical microscopic image of PillarHall-3 conformality test chip with its top membrane on (sample 13, Table 1). A distance indicator scale is marked on top of the membrane for optical analysis.

Table S1. Description of the PillarHall™-3 chips containing microscopic LHAR channels in the main test structure area, from top to bottom, most demanding to least demanding aspect ratio

Opening width W (µm)	Lateral length L (µm)	Code on chip	Opening type	Maximum AR (channel height 100 nm)	Maximum AR (channel height 500 nm)	Maximum AR (channel height 2000 nm)
100	5000	W100 L5mm	One-sided	50000 : 1	10000 : 1	2500 : 1
90	1000	W90 L1mm	Mirrored	10000 : 1	2000 : 1	500 : 1
80	500	W80 L0.5mm	Mirrored	5000 : 1	1000 : 1	250 : 1
70	100	W70 L100	Mirrored	1000 : 1	200 : 1	50 : 1
60	52	W60 L52	Mirrored	520 : 1	104 : 1	26 : 1
50	22	W50 L22	Mirrored	220 : 1	44 : 1	11 : 1
40	10	W40 L10	Mirrored	100 : 1	20 : 1	5 : 1
30	5	W30 L5	Mirrored	50 : 1	10 : 1	2.5 : 1
20	1	W20 L1	Mirrored	10 : 1	2 : 1	0.5 : 1

Table S2. Different support pillar arrays in PillarHall-3 conformality test prototypes

Pillar layout	Pillar inter-distance *a* (µm) [a]	Distance between rows of pillars *l* (µm)	Pillar diameter *d* (µm)
v1a	28	24.2	4
v1b	49	42.4	4
v2a	98	84.9	4
v2b	49	42.4	2

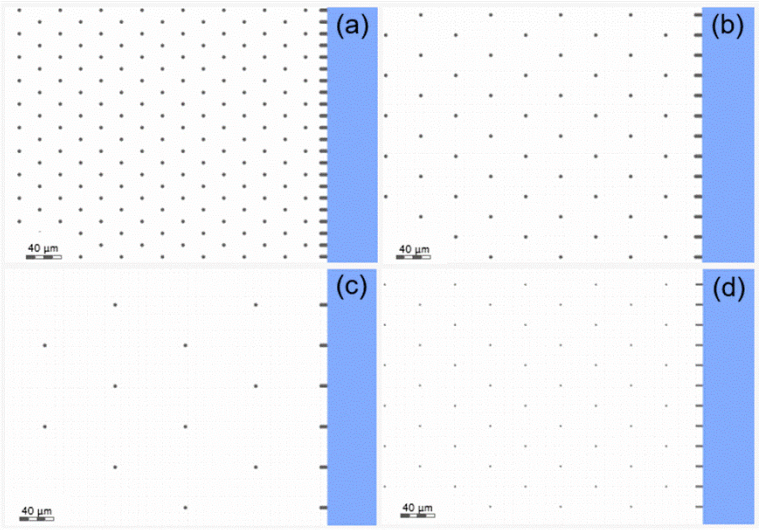

Figure S3. Illustration of the top view of PillarHall-3 with Different pillar array layouts fabrication: (a) Layout v1a, (b) Layout v1b, (c) Layout v2a, (d) Layout v2b. Layout details in Table S2.

Table S3. List of prepared samples with their unique sample code used during the analysis (and thus traceable) and TMA-water ALD sequences on PillarHall-3 at 300 °C (varied variables bolded)

Series	Sample code	Unique sample code	Wafer code-location of the chip-pillar layout-channel height	TMA pulse-purge-water pulse-purge (s)
A	1	V0068	M10-C03-1A-500	0.1-4.0-0.1-4.0
	2	V0069	M10-F03-1B-500	0.1-4.0-0.1-4.0
	3	V0070	M10-D04-2A-500	0.1-4.0-0.1-4.0
B	4	V0004	W15-F02-1B-500	0.1-4.0-0.1-4.0
	5	V0004	W15-F02-1B-500	0.1-4.0-0.1-4.0
	6	V0004	W15-F02-1B-500	0.1-4.0-0.1-4.0
C	7	V0012	M05-H02-1B-**100**	0.1-4.0-0.1-4.0
	8	V0001	M08-F05-1B-**500**	0.1-4.0-0.1-4.0
	9	V0008	M15-G03-1B-**2000**	0.1-4.0-0.1-4.0

	10	V0057	M12-G01-1B-500	0.1-4.0-0.1-4.0
D	8	V0001	M08-F05-1B-500	0.1-4.0-0.1-4.0
	11	V0031	M08-F06-1B-500	0.1-4.0-0.1-4.0
	12	V0041	M08-C04-1B-500	**0.1**-4.0-0.1-4.0
E	13	V0050	M12-H02-1B-500	**0.2**-4.0-0.1-4.0
	14	V0053	MXX-B06-2A-500	**0.4**-4.0-0.1-4.0
	15	V0047	M12-F01-1B-500	0.1-**1.0**-0.1-**1.0**
F	12	V0041	M08-C04-1B-500	0.1-**4.0**-0.1-**4.0**
	16	V0044	M08-G02-1B-500	0.1-**10**-0.1-**10**

Table S4. List of samples prepared by TMA-water ALD sequences on PillarHall-3 at 300 °C and analyzed by AFM

Unique sample code	Wafer code-location of the chip-pillar layout-channel height	TMA pulse-purge-water pulse-purge (s)	Note
-	M10-H03-1B-500	-	AFM measurement across the chip with its membrane on (Figure S13)
-	M06-G03-1B-100	-	AFM measurement across the chip with its membrane on (Figure S13)
V0038	M10-D06-2A-500	0.1-4.0-0.1-4.0	AFM measurement across the chip (Figure S6)
V0043	M06-D05-2A-100	0.1-10.0-0.1-10.0	AFM measurement across the chip (Figure S6)

2. Supporting information to Results

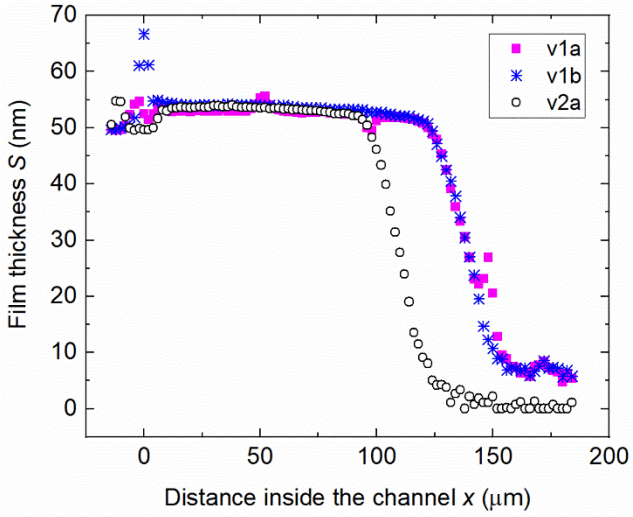

Figure S4. The as-measured saturation profile of samples 1 to 3 with different pillar layout designs were measured with reflectometry after removing the membrane (Table 1 Series A).

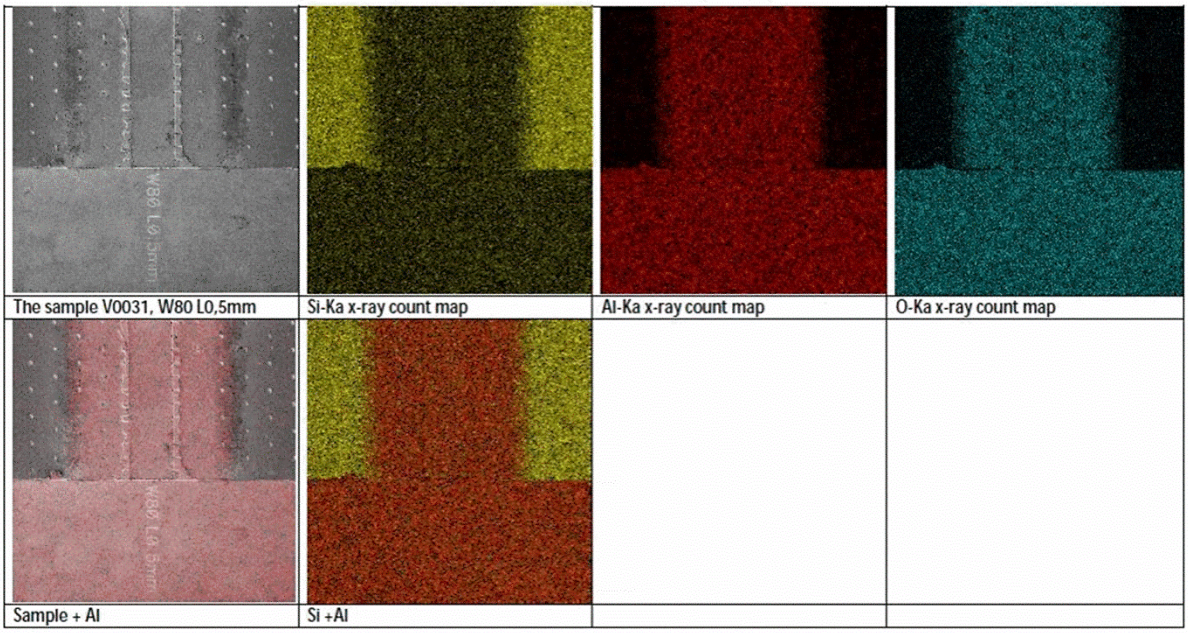

Figure S5. Elemental maps for Si, Al, and O of PillarHall-3 chip top view (sample 11 in Table 1) measured by SEM-EDS. ALD Al_2O_3 was coated on the chip using the 1000 cycles with the ALD process sequences of TMA pulse-purge-water pulse-purge of (0.1-4.0-0.1-4.0) s, and the top membrane was removed by adhesive tape before the measurement.

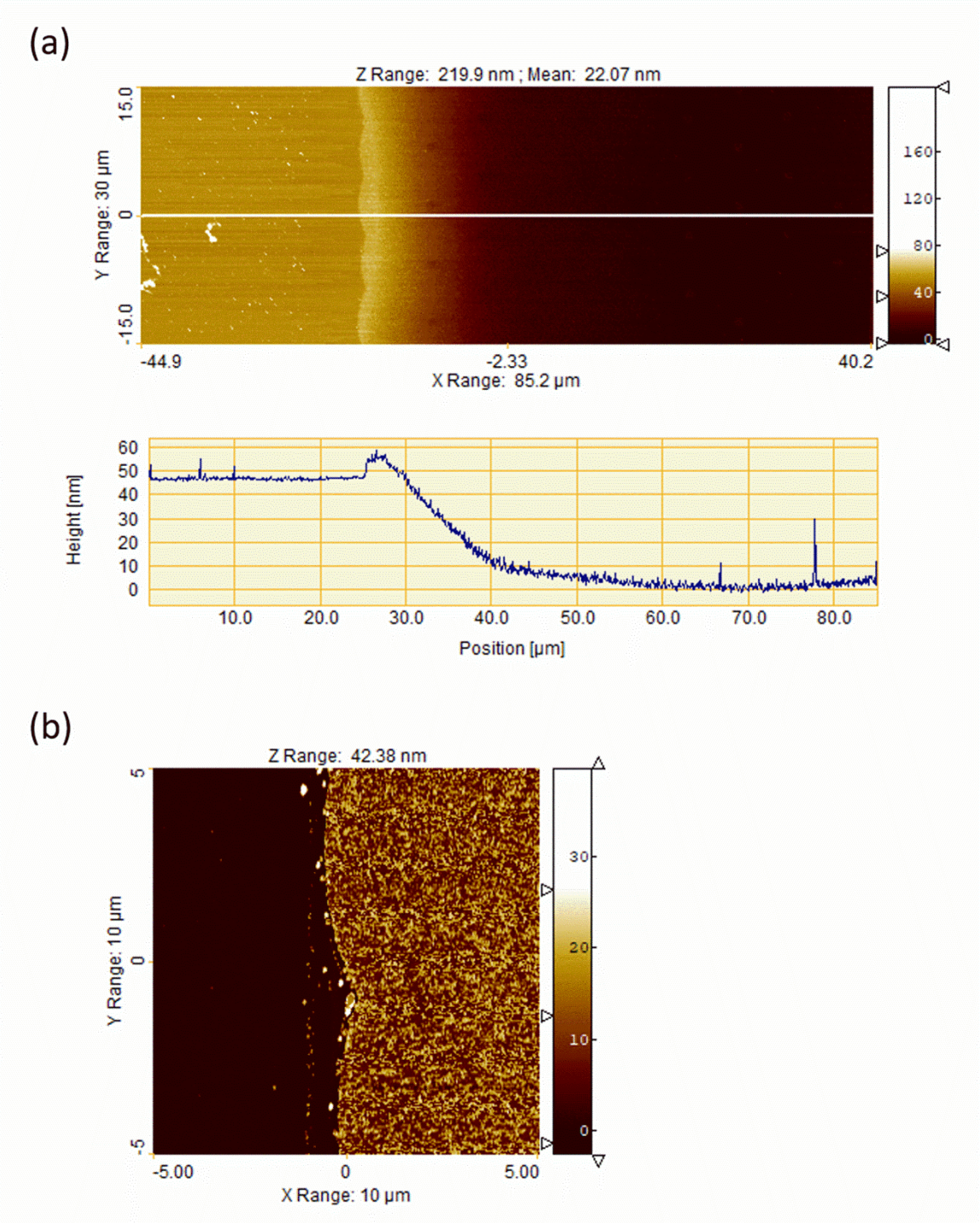

Figure S6. (a) AFM image (top) and line scan (bottom) across the PillarHall-3 prototype (design channel height of 100 nm) coated by Al_2O_3 film made in 500 cycles at 300 °C. Unique sample code: V0043. (b) AFM image of before (Region I) and after (Region II) the LHAR channel entry with its design channel height of 500 nm. Unique sample code: V0038. These samples are not listed in Table 1.

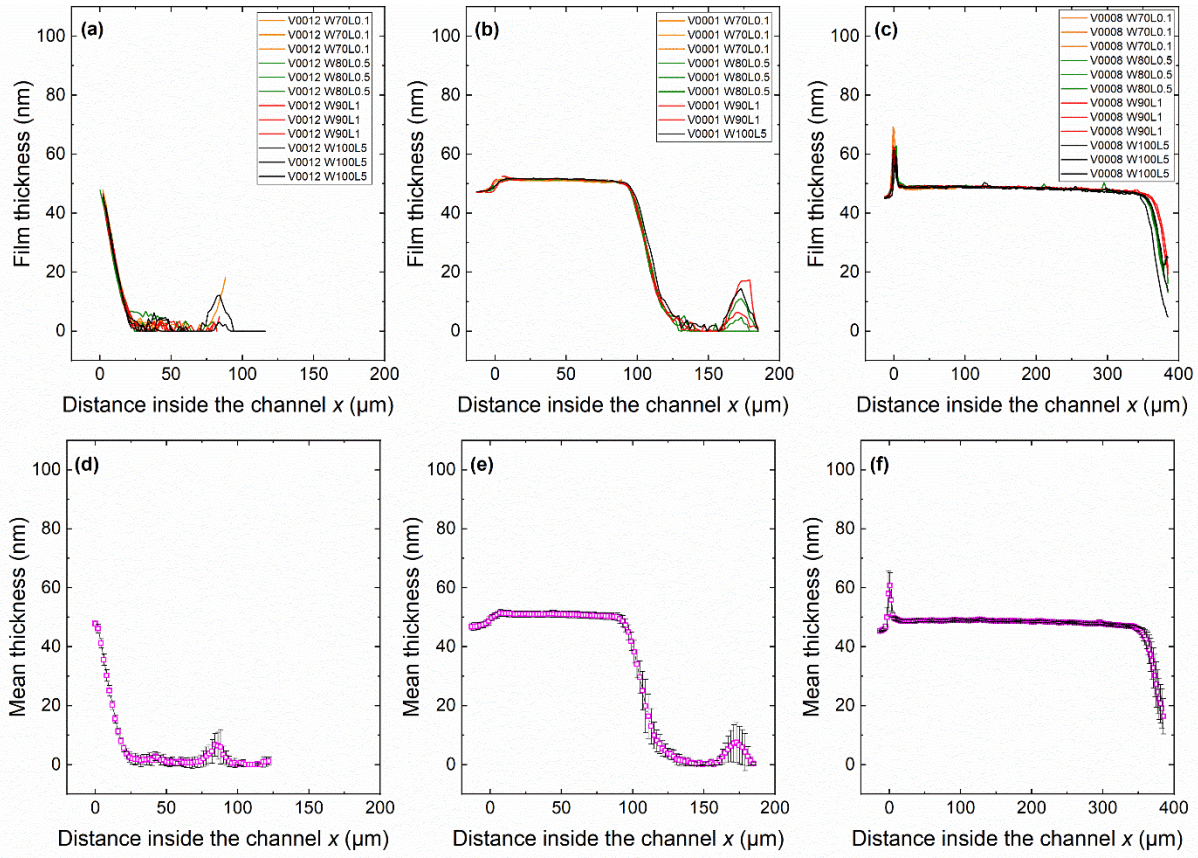

Figure S7. Reflectometer line scans for ALD Al_2O_3 film made in 500 cycles at 300 °C in PillarHall-3 LHAR channels. Different design channel heights were used [100, 500, and 2000 nm for panels (a), (b), and (c), respectively]. Samples 7, 8, and 9 (Table 1 Series C). Panels (a), (b), and (c): For each channel, having various opening width *W* (mm) and lateral length *L* (mm), the thickness measurement was repeated several times. Each time, 100 data points were obtained from 100 and 500 nm channels and 200 points from 2000 nm channel. Panels (d), (e), and (f): The mean film thicknesses were determined from the average of each location. The square symbol presents the mean thickness value, and the error bar represents one standard deviation.

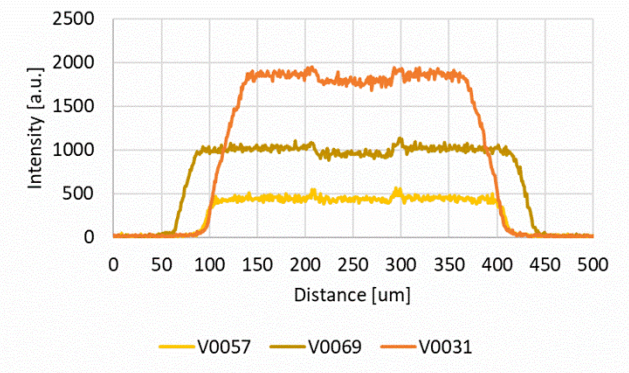

Figure S8. SEM-EDS line scans of Al in the samples made in different numbers of ALD cycles (250, 500, and 1000 cycles used, Sample details in Table 1, Series D within PillarHall-3 LHAR channel with design channel height of 500 nm).

2.1 ALD film thickness vs. cycles

The relationship between the Al_2O_3 ALD film thickness and number of ALD cycles was analyzed. In Figure S9, linear film growth against the number of cycles was observed from the films made in 250, 500, and 1000 cycles over the design channel height of 500 nm. The GPC in the channel decreased slightly with increasing number of ALD cycles (Figure S9 b). The higher GPC in the beginning could have been caused by the rough surface of the etched channel. The intercepts of *y*-axis in the film growth plot (Figure S9 a) indicate the existence of native silicon oxide layer and the surface roughness in the channel (Region IIb). To exclude the effect of native oxide layer and rough surface, thickness values were corrected by subtracting those intercept values (Figure S9 c), and GPC was recalculated using the corrected thickness (Figure S9 d).

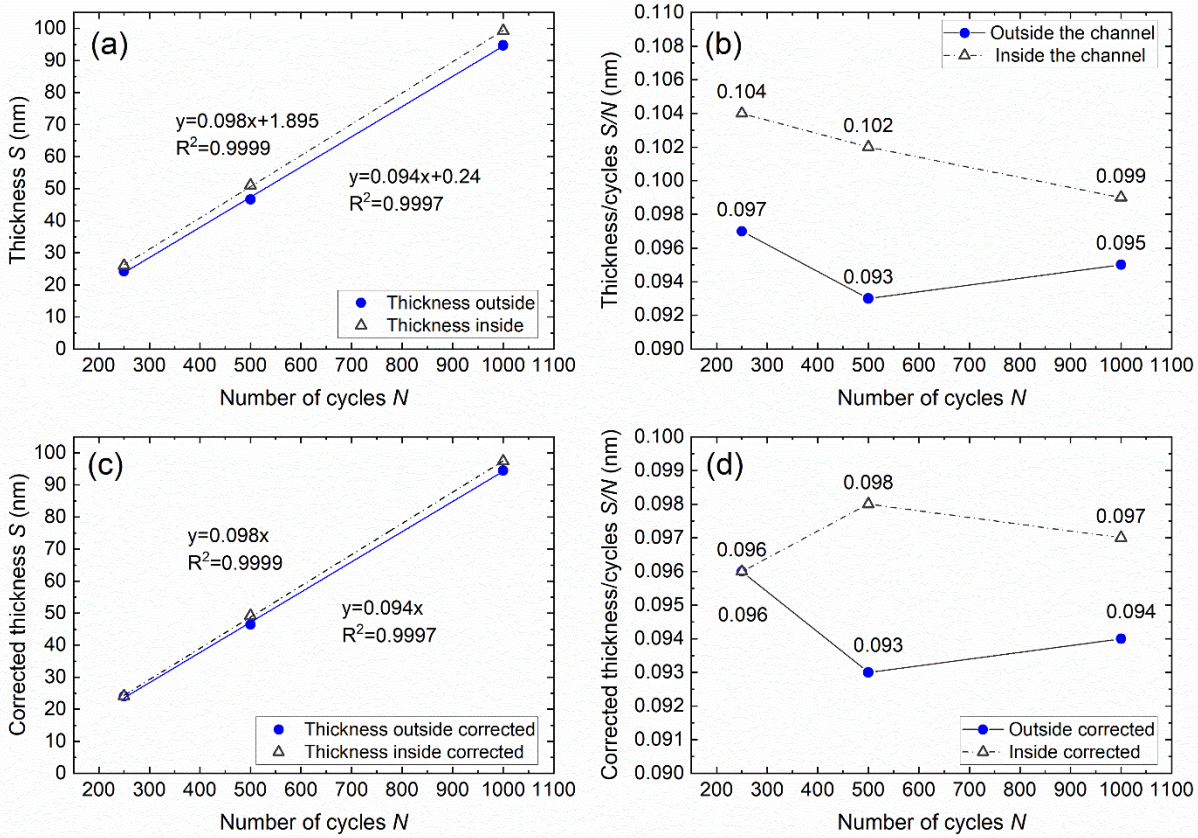

Figure S9. Film thickness with respect to the number of ALD cycles for TMA-water process at 300 °C in a LHAR channel, having a design channel height of 500 nm (Table 1 Series D). The mean film thickness of 100 points obtained by reflectometer line scan after the removal of the top membrane. (a) The film thicknesses as a function of the number of growth cycles. (b) Thickness data of (a), divided with the number of ALD cycles. (c) The film thickness inside and outside the channel were corrected by subtracting the intercept values in panel (a). (d) Thickness data of (c), divided with the number of ALD cycles.

3. Supporting information to Discussion

3.1 Fabrication issues related to LHAR channels in different heights

The LHAR channel fabrication targeted channels with the heights of 100, 500, and 2000 nm. For each wafer, some fabrication-related parameter was varied, and on a wafer, up to four layouts were experimented with. Our work has concentrated on reporting on the channels with a targeted 500 nm channel height, where the fabrication worked out best. The channels with 2000 nm had fabrication (dry etch) related issues, leading to that some of the features were accidentally rounded and some channels were lost or narrowed. The channels with targeted 100 nm channel height, in turn, suffered from large relative error in the channel height because of membrane hanging between pillars and already small channel. On the basis of the analysis presented, the LHAR channel with Layout v1b will give the most reliable and comparable results.

Table S5. Measured silicon dioxide thickness during the fabrication of PillarHall-3 chip. Each wafer was measured five times in different locations

Wafer no.	1st (nm)	2nd (nm)	3rd (nm)	4th (nm)	5th (nm)	Mean (nm)	Standard deviation (nm)
M5	108.6	108.7	107.5	109.1	109.1	108.6	0.8
M6	108.1	107.9	106.8	107.9	107.9	107.7	0.5
M8	519.1	520.5	519.6	517.3	519.0	519.1	1.2
M9	520.5	519.0	519.4	519.4	517.3	519.1	1.1
M15	2036.3	2034.9	2034.8	2034.4	2033.3	2034.7	1.1
M16	2033.9	2032.8	2033.6	2031.9	2032.5	2033.0	0.8

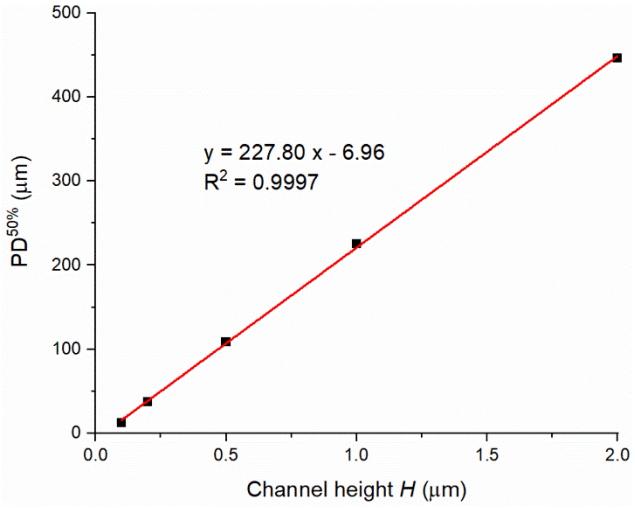

Figure S10. MATLAB simulation for the effect of channel height H on $PD^{50\%}$. Parameters used: H = 500 nm, N = 500, T = 300 °C, t_{pulse} = 0.1 s, M_A = 0.075 kg/mol, p_{A0} = 100 Pa, d_A =

591 pm, M_B = 0.028 kg/mol, p_B = 300 Pa, d_B = 374 pm, GPC = 0.098 nm, q = 3.6 nm^{-2}, K = 1000 Pa^{-1}, ρ = 3100 kg/m^3, c = 0.012, and P_d = 0.043 s^{-1}.

3.2 The effect of pillars on saturation profile

The pillars in PillarHall-3 conformality test chips keep the top membrane from touching the bottom of the structure. They also act as distance indicators in top-view microscopy. Yet, the pillars alter the surface area to be coated and increase diffusion resistance. Here, we mathematically assess the effect of the pillars on diffusion.

F (mol/m^{2}s) is the flux of material in direction x, and it is calculated as

$$F = HwD\,(dc/dx), \quad (1)$$

where H (m) is height of a rectangular channel, W is width of the channel, D is diffusion constant of molecule (m^2/s), and c is concentration. If the change in concentration in distance L (m) is C the gradient is

$$dc/dx = C/L. \quad (2)$$

The diffusion resistance is defined as

$$R = C/F. \quad (3)$$

Therefore, the diffusion resistance R (s/m^3) of a rectangular channel is

$$R = \frac{H}{WLD}. \quad (4)$$

If the diameter of the pillar is d (m) and the distance between them is a (m), the diffusion resistance of one row of pillars with the number of n is

$$R_{\mathrm{row}} = \frac{d}{H(a-d)Dn}. \quad (5)$$

The diffusion resistance of the space between pillar rows is

$$R_0 = \frac{a-d}{HaDn}. \quad (6)$$

If there would be no pillars the total diffusion resistance would be

$$R_{\mathrm{open}} = \frac{a}{HaDn}. \quad (7)$$

The ratio of diffusion resistances with pillars to without them is

$$r_{\mathrm{R}} = \frac{R_{\mathrm{row}}+R_0}{R_{\mathrm{open}}} = \frac{\left(\frac{a}{d}\right)^2-\frac{a}{d}+1}{\left(\frac{a}{d}\right)^2-\frac{a}{d}}. \quad (8)$$

The diffusion resistance ratio is plotted in Figure S11 as a function of the dimensionless pillar distance a/d. In the most dense pillar configuration the effect on the diffusion resistance is slightly above 2% which might be noticeable in the most precise penetration depth measurement. Therefore, the pillar distance should be at least 11 times larger than the pillar diameter so that the effect on diffusion resistance is below 1%.

To estimate how the surface area to be coated changes, we assume that the pillars have a cylindrical shape having a diameter d. The surface growth area decreases by the top and bottom parts of pillars $2\pi(\frac{d}{2})^2$, whereas it increases by the surface area of the side of each pillar A_1, which is

$$A_1 = \pi dH. \quad (9)$$

The channel height H also influences the surface growth area, since the pillar area A_1 depends on the height. The surface area of the channel roof and ceiling in a triangle formed by three pillars is

$$A_0 = \sqrt{3}a^2, \qquad (10)$$

where a is distance between pillars. The total surface growth area with pillars is

$$A_{\text{growth}} = \sqrt{3}a^2 + n[\pi dH - 2\pi\left(\frac{d}{2}\right)^2], \qquad (11)$$

where n is the number of whole pillars in the triangle. Because the internal angles in an equilateral triangle are 60° each of the three pillars have 1/6 of their volume in the triangle. The total number of whole pillars thus is n= 0.5. The ratio of film growth area with pillars to no-pillars case is

$$r_{\text{A}} = \frac{A_{\text{growth}}}{A_0} = 1 + \frac{\pi dH - 2\pi\left(\frac{d}{2}\right)^2}{2\sqrt{3}a^2}. \qquad (12)$$

With pillars having the diameter of 4 µm in H = 0.5 µm channel the effect on film growth area is below 1% if the pillar inter-distance a is larger than 25 µm (Figure S12 a). Therefore, for the typical pillar layout v1b the effect on film growth area is negligible as its pillar inter-distance is large enough (49 µm).

Increase of the diffusion resistance decreases the film penetration depth, while the decrease of the film growth area increases the penetration depth. The apparent diffusion constant with pillars is $D = D_0/(r_R r_A)$ where D_0 is the diffusion coefficient without pillars. Thus the effects tend to cancel each other and the net effect on the apparent diffusion coefficient D is small (Figure S12 b).

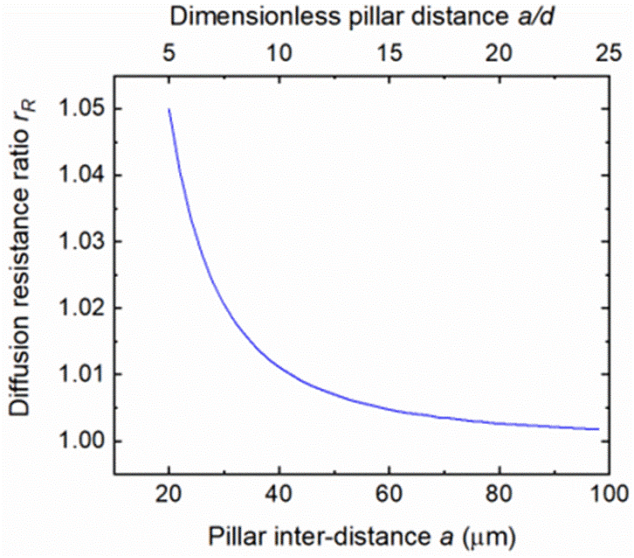

Figure S11. The relative increase of diffusion resistance when the distance between the pillars a decreases. For the default design, the pillar diameter d is 4 µm.

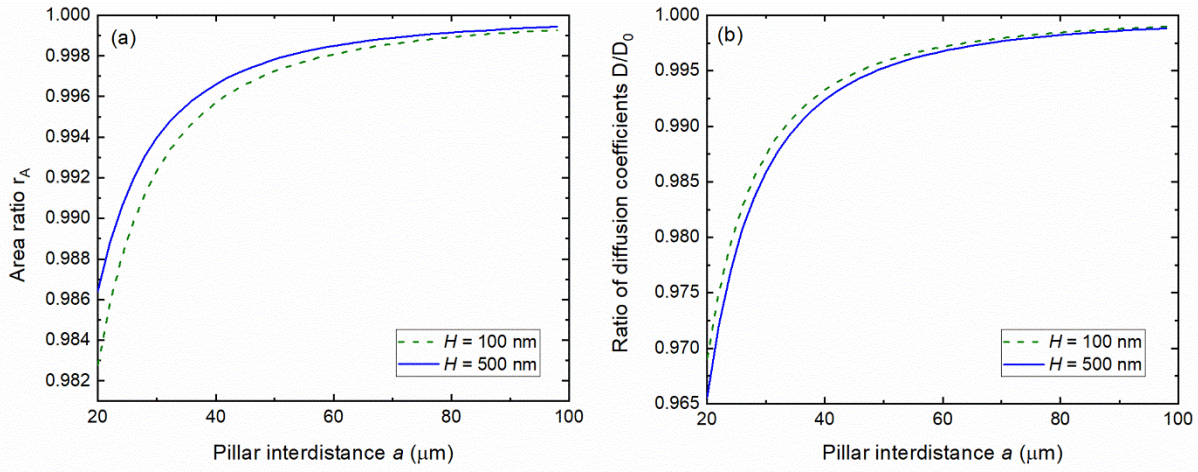

Figure S12. (a) The reduction in the growth area when the distance *a* between the pillars changes. (b) The change in the relative apparent diffusion coefficient *D* when the distance a between the pillars changes. D_0 is the diffusion coefficient without pillars.

3.3 AFM analysis on LHAR channel with its membrane

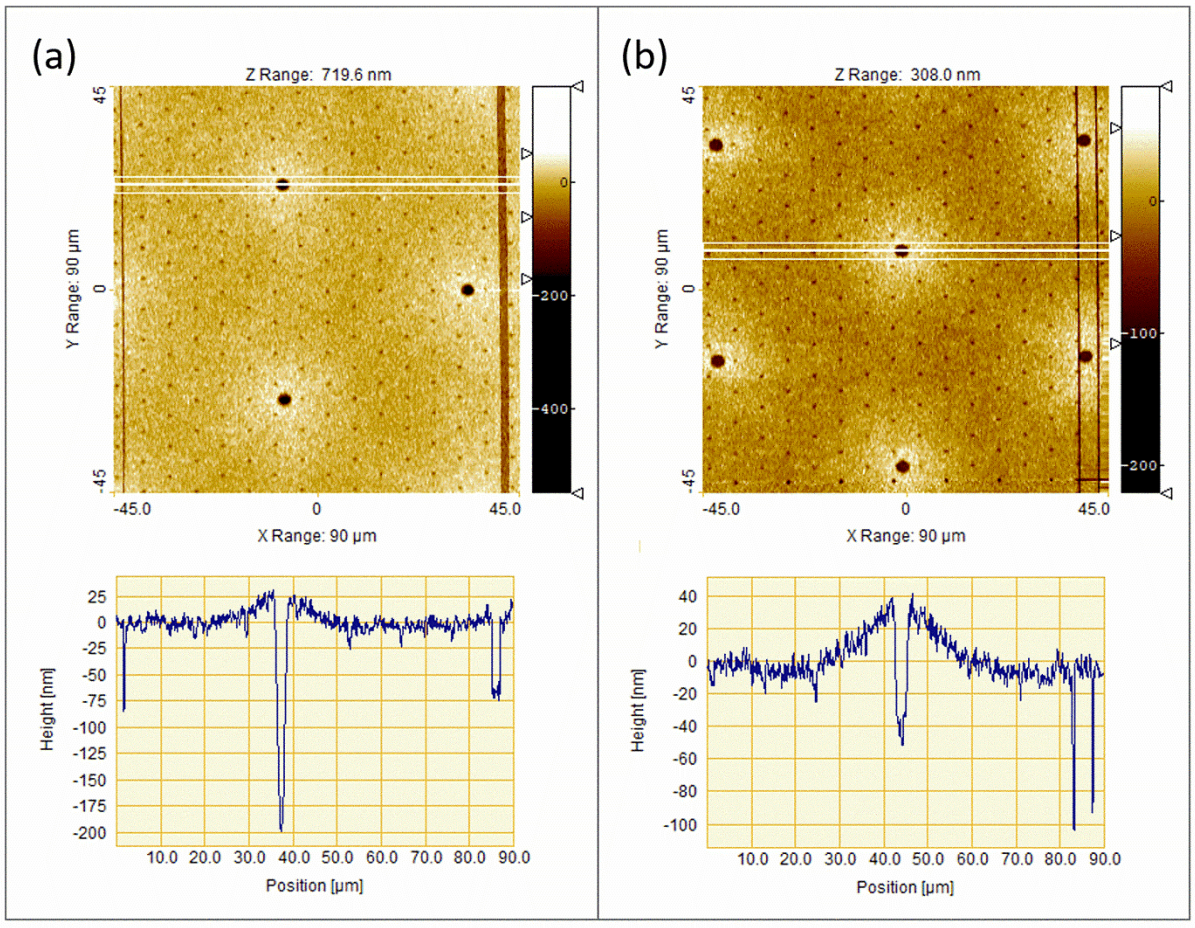

Figure S13. AFM measurement across the top membrane of LHAR microscopic PillarHall-3 prototypes with their design channel height of (a) 500 nm (Layout of v1b) and (b) 100 nm (Layout of v1b). Top row: AFM images. Bottom row: line scans.

3.4 GPC vs. pulse length and purge length

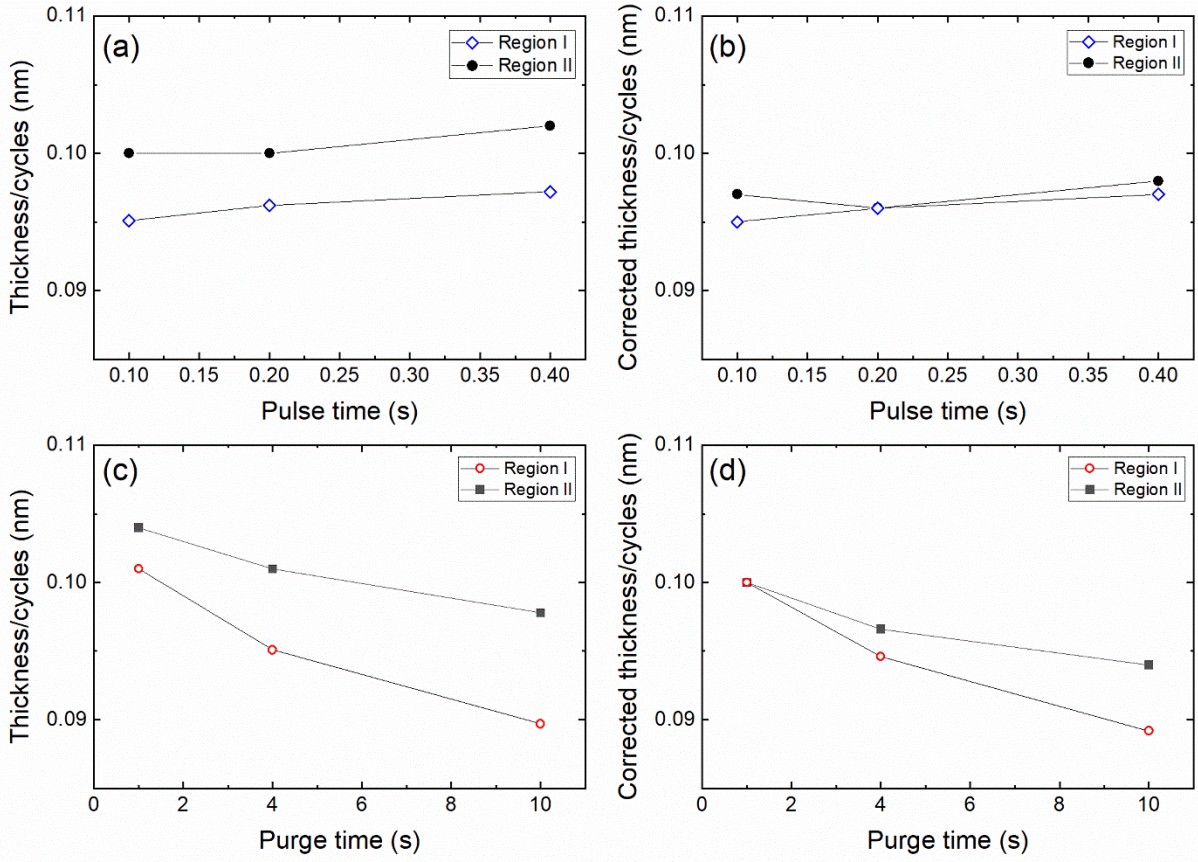

Figure S14. GPC with respect to different TMA pulse time [panels (a) and (b)] and purge time [panels (c) and (d)]. Al_2O_3 film was grown at 300 °C in the test structure with the design channel height of 500 nm. GPC was determined as saturated film thickness per growth cycles. Panel (b) and (d): film thickness and GPC correction were made by subtracting the intercept values in Figure S9 panel (a).

3.5 The comparison of PillarHall generations

The PillarHall-3 design reported in this work differs from the PillarHall-1 design, used in earlier works.[1–3] The most important differences are described in Table S6. In addition, a fundamental difference is that in PillarHall-3, the entrance to the channel was at the same level as the channel itself, whereas in PillarHall-1 contained a recess in front of the channel caused by etching of silicon. With PillarHall-3, one could thus determine the film thickness in front of the channel for reference purposes (Region I), whereas for PillarHall-1, such reference measurement could not be made.

Table S6. Difference in characteristics of PillarHall-3 compared to PillarHall-1

Chip generations	LHAR channel shape and symmetry	Pillar composition	Pillar arrangement	Pillar size	Reference

PillarHall-1	Elongated circle; 1d symmetry in the center and circular hole symmetry at the edges	Silicon dioxide	Honeycomb symmetry (a=ca. 9 μm)	Variable controlled by etch time	Gao et al.[1]
PillarHall-3	Rectangular; 1d symmetry	Polysilicon	Hexagonal symmetry (a = 49 μm for layout v1b)	Design value 4 μm; controlled by lithography	This work

We observed a nanostep near the start of the channel of PillarHall-3 (Figure S15 and Figure 3b). While the origin of the step is not fully understood, it could have been caused by the rough channel surface resulting from plug-up process.[4] This roughness should have been similar in PillarHall-3 and PillarHall-1, as the same plug-up process is used in both fabrication processes.

To qualitatively compare the results obtained from PillarHall-3 with those of PillarHall-1, scaled saturation profiles for Al_2O_3 films made with the TMA-water process with the same number of cycles at 300 °C in the two test structures are shown in Figure S15. The Al_2O_3 film penetrated slightly deeper in PillarHall-3, likely because of lower diffusion resistance due to less dense pillars. The saturation profile was smoother with less noise, most likely because the pillar remnants did not disturb the measurement in PillarHall-3 (spot size ~5 micrometer fits in the space between pillars). A small difference in slope at the saturation front is observed (-0.00099 nm and -0.00136 nm for sample 11 and Gao et al.,[1] respectively).

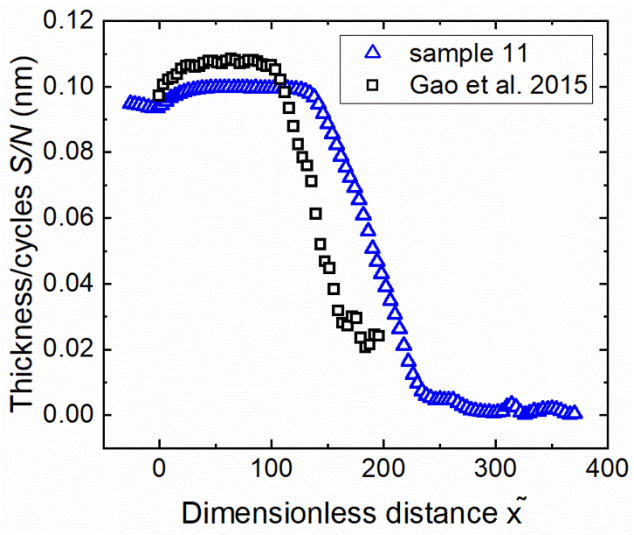

Figure S15. Scaled saturation profile of Al_2O_3 ALD thin film obtained from our experiment compared to Gao et al.[1] Our study used PillarHall-3 while the reference used PillarHall-1. Both prototypes had design channel heights of 500 nm, and the films were made in 1000 cycles.

3.6 Origin of spikes occasionally observed in saturation profile

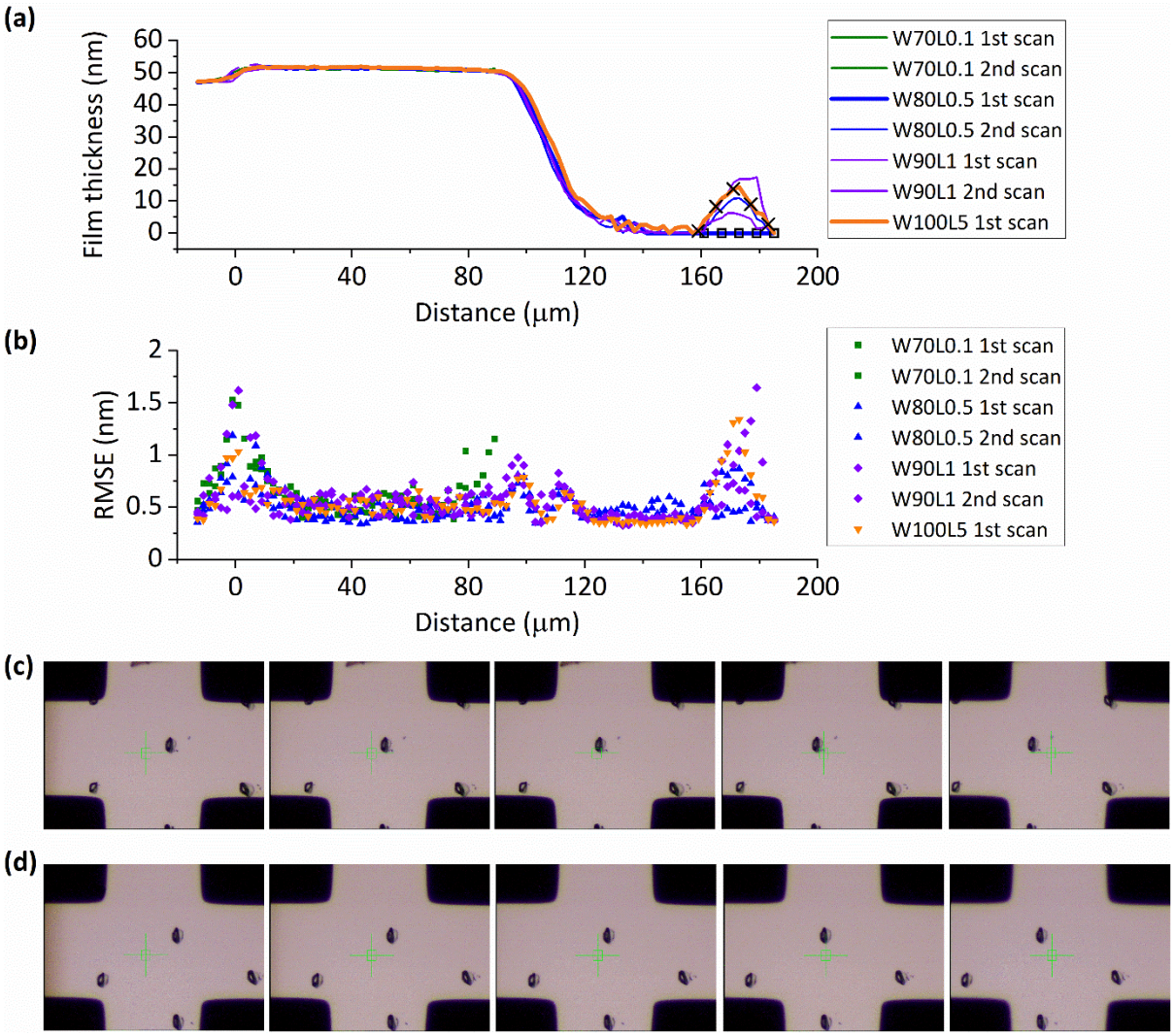

Figure S16. Repeated saturation profile measurements for Sample 8 (Table 1) after removing the top membrane: (a) line scans measured by reflectometer with an occasional spike in Region IV, (b) the corresponding root mean square error (RMSE) fitting residual of the reflectometer measurement, and (c) and (d) microscope images related to the measurement spots marked with x and ☐ in panel (a) for channel W100L5 and W80L0.5 (1st scan), respectively. LHAR design channel height 500 nm and pillar layout design v1b.

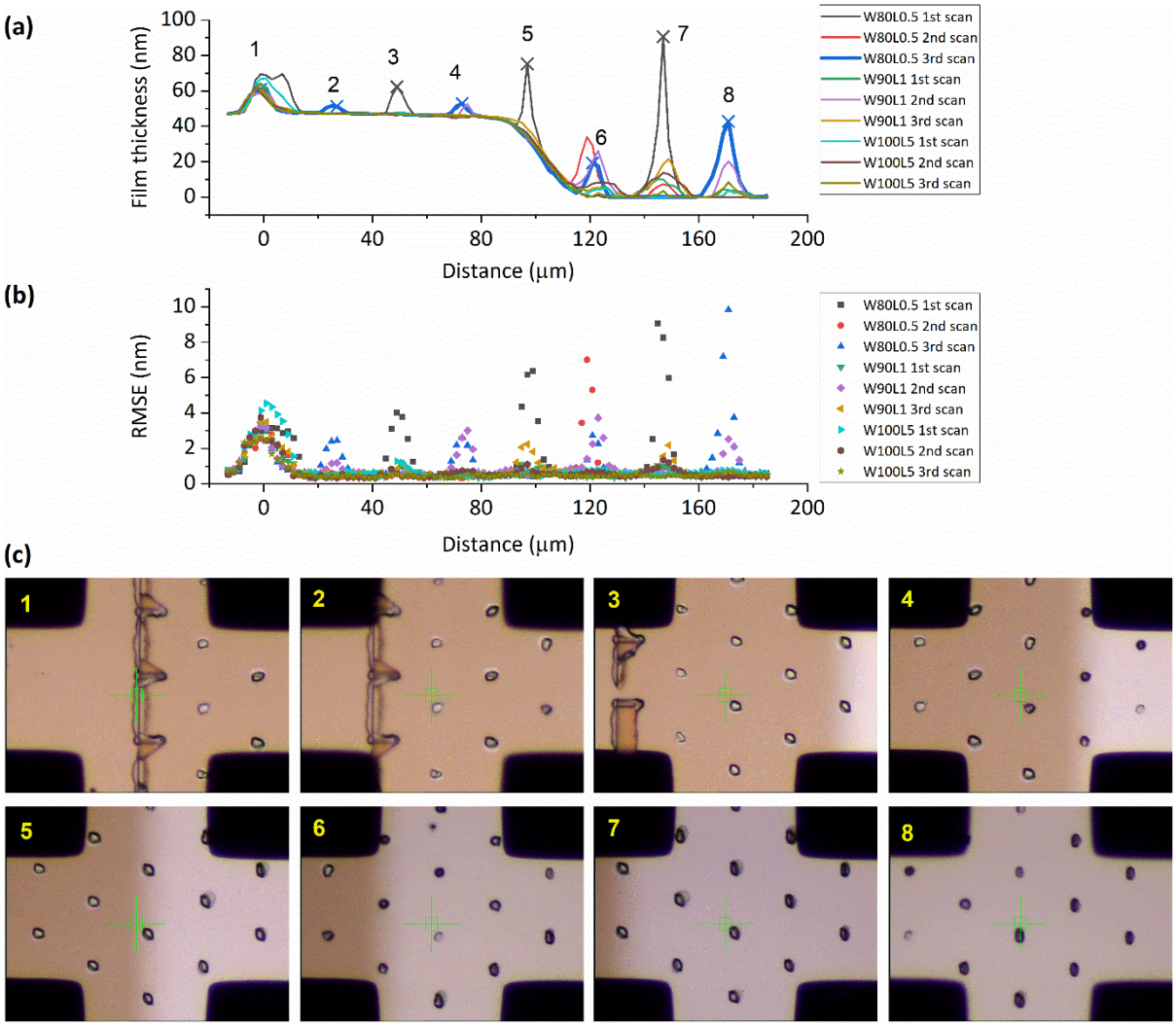

Figure S17. Repeated saturation profile measurements after removing the top membrane: (a) line scans measured by reflectometer with occasional spikes in Regions II to IV, (b) the corresponding RMSE fitting residual of the reflectometer measurement, and (c) microscope images related to the measurement spots marked with x in panel (a), channel W80L0.5 (1st and 3rd scan). For this sample (V0005, not in Table 1), as a sacrificial layer, low-pressure chemical vapor deposition process based on tetraethyl orthosilicate (LPCVD TEOS) was used instead of thermal silicon oxide layer. Al_2O_3 was coated on LHAR channels with a design channel height of 500 nm and pillar layout design of v1a by ALD sequence of TMA-water-purge-water of (0.1-4.0-0.1-4.0) s at 300 ˚C. 500 cycles were used.

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