

Supporting Information

Interface-induced transition from Schottky-to-Ohmic contact in Sc_2CO_2 -based multiferroic heterojunctions

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Table S1. Optimized lattice constant ($a = b$), equilibrium interface distance (d), and binding energy (E_b) of MnSe₂/Sc₂CO₂ with different stacking modes.

Stacking modes	$a=b$ (Å)	d (Å)	E_b (eV)	contact type
U1	3.42	3.41	1.44	Schottky
U2	3.42	3.40	1.47	Schottky
U3	3.42	3.48	1.38	Schottky
D1	3.42	2.89	1.49	Ohmic
D2	3.42	2.76	1.58	Ohmic
D3	3.42	2.79	1.53	Ohmic

Figure S1

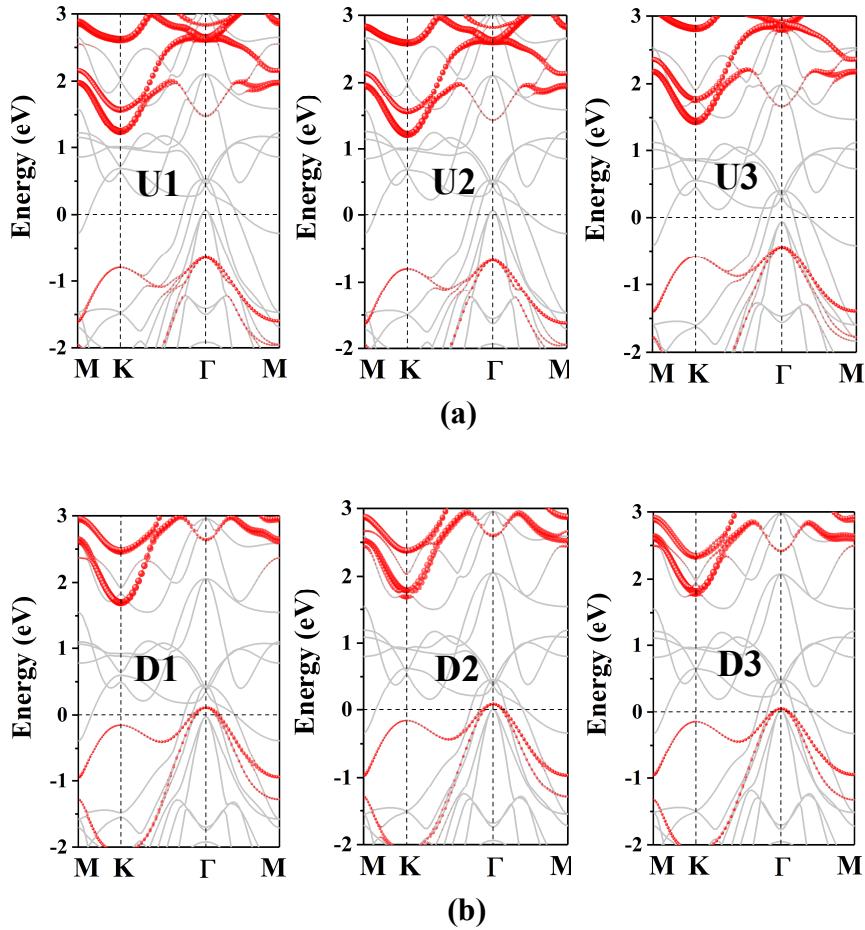


Figure S1. The electronic band structures of (a) MnSe₂/Sc-P[↑], (b) MnSe₂/Sc-P[↓] with different stacking modes.

Figure S2

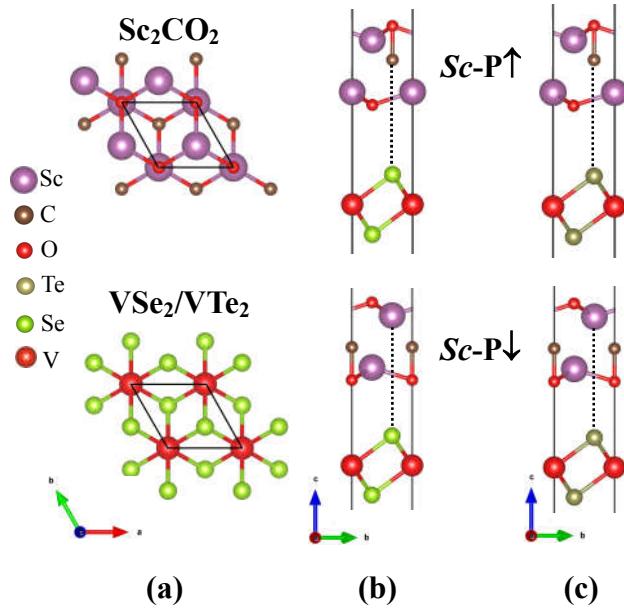


Figure S2. (a) Top views of Sc_2CO_2 , VSe_2 or VTe_2 . Side views of $\text{VSe}_2/\text{Sc}_2\text{CO}_2$ (b), and $\text{VTe}_2/\text{Sc}_2\text{CO}_2$ (c) with polarized states $\text{Sc-P}\uparrow$ and $\text{Sc-P}\downarrow$.

Figure S3

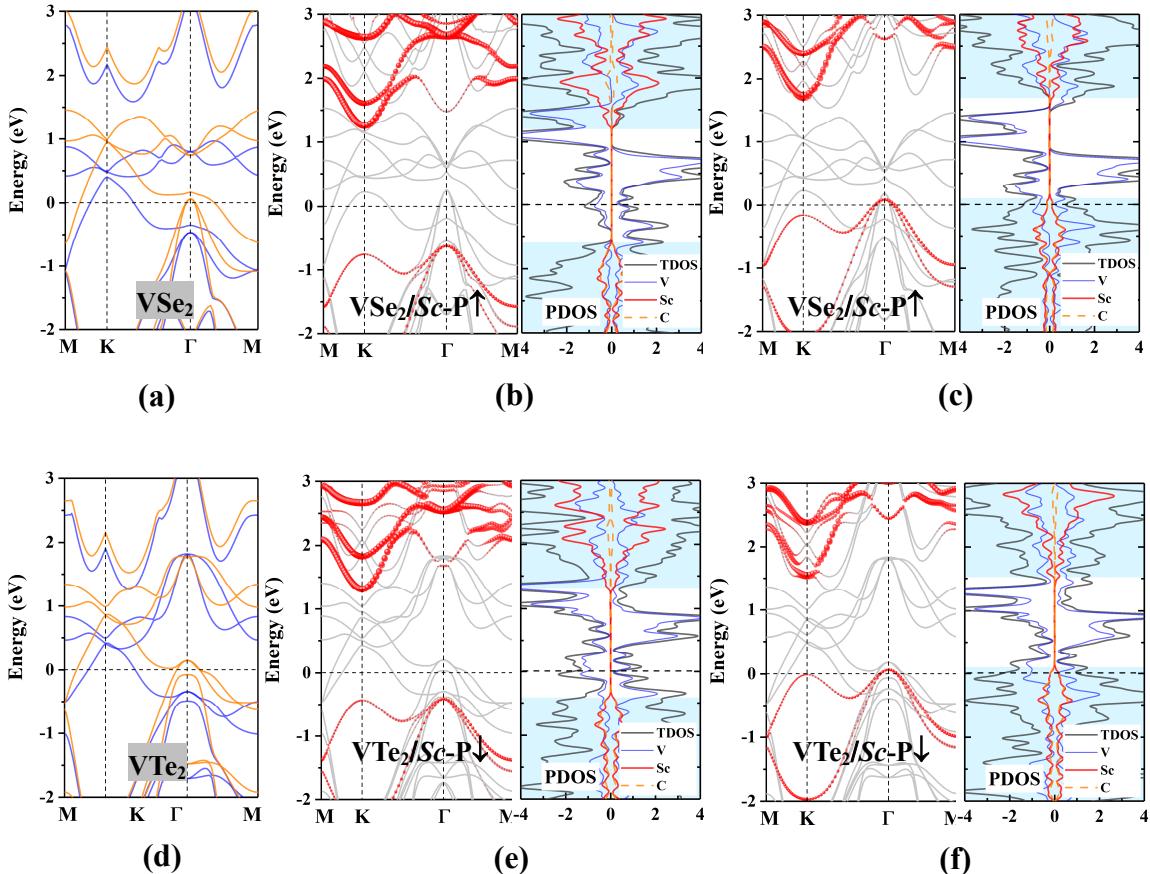


Figure S3. The electronic band structures of (a) 1T-VSe₂, (b-c) VSe₂/Sc₂CO₂, (d) 1T-VTe₂, and (e-f) VTe₂/Sc₂CO₂ with polarized states $Sc\text{-}P\uparrow$ and $Sc\text{-}P\downarrow$. On the right (b-c, e-f) is the corresponding projected density of states.

Figure S4

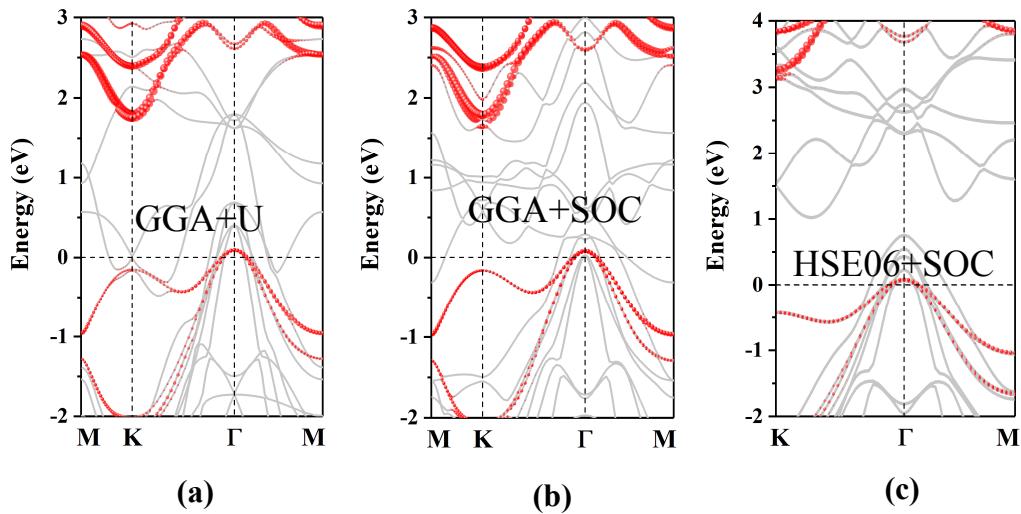


Figure S4. The electronic band structures of MnSe₂/Sc-P↓ heterostructures with (a) GGA+U_{eff} ($U_{\text{eff}}=3.9$ eV), (b) GGA+SOC, and (c) HSE06+SOC.

Figure S5

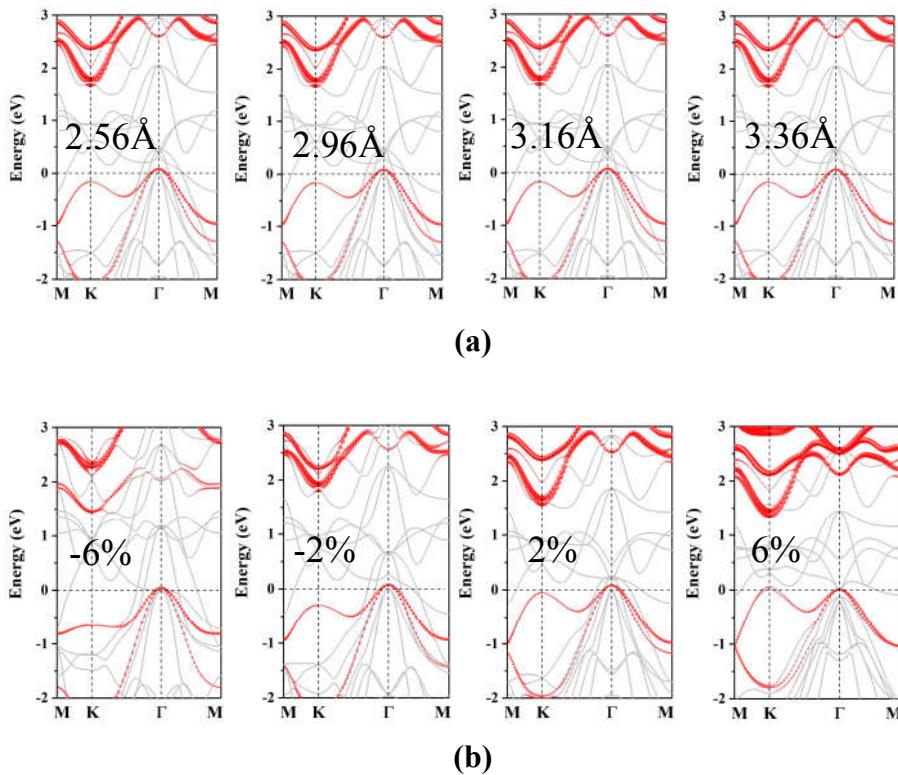


Figure S5. The electronic band structures of MnSe₂/Sc-P↓ with different interlayer distances (a) and biaxial strains (b), exhibiting an intrinsic Ohmic contact.

Figure S6

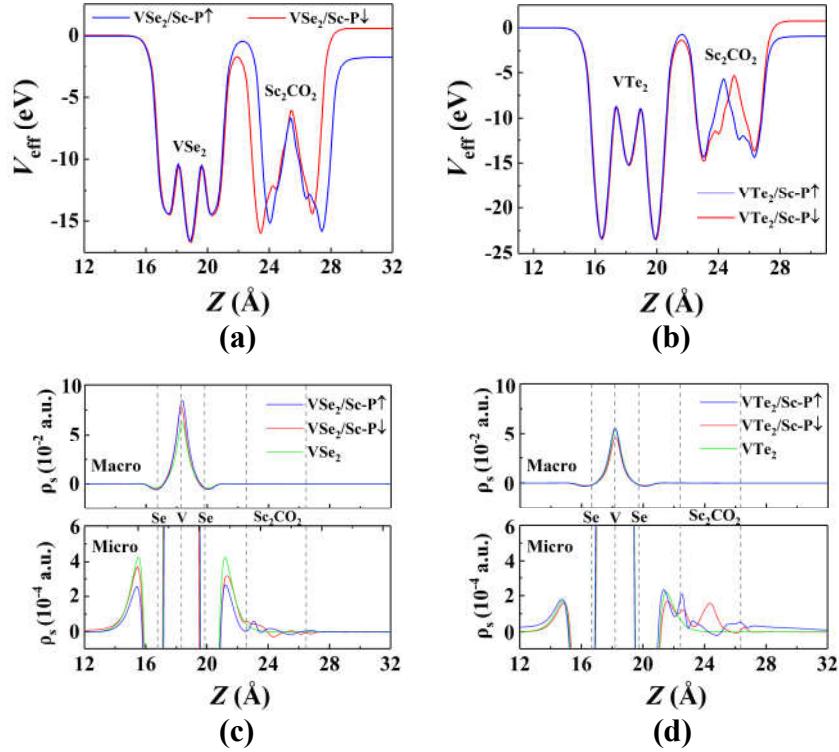


Figure S6. (a-b) The effective potentials (V_{eff}) and (c-d) the spin density (ρ_s) along the vertical z -direction of $\text{VSe}_2/\text{Sc}_2\text{CO}_2$ and $\text{VTe}_2/\text{Sc}_2\text{CO}_2$ with polarized states $\text{Sc-P}\uparrow$ and $\text{Sc-P}\downarrow$.

Figure S7

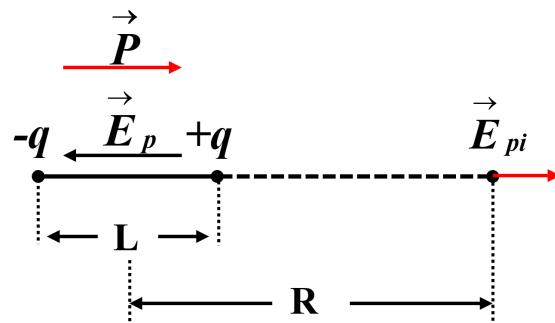


Figure S7. Electric field strength (\vec{E}_{pi}) of electric dipole (\vec{P}) at the heterojunction interface.

Figure S8

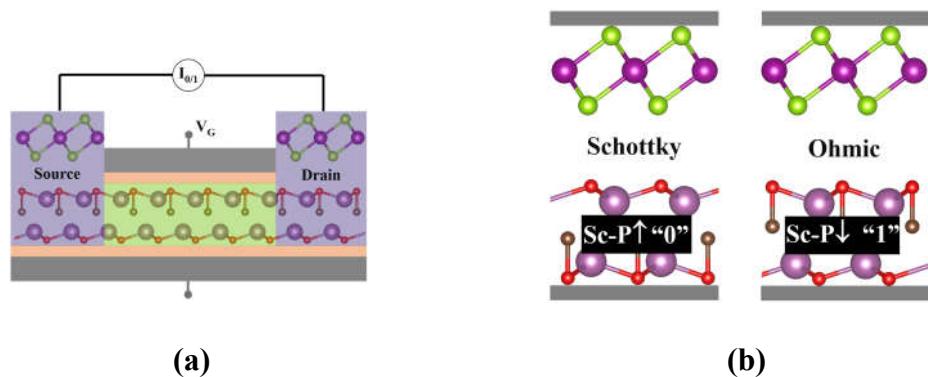


Figure S8. Device model diagrams of (a) field effect transistor and (b) memory.