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Supportting Information

Flexible Boron Nitride-based Memristor for In-situ Digital and Analogue Neuromorphic Computing Applications

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S1. TEM images and EDX elemental analysis of BN nanosheets.

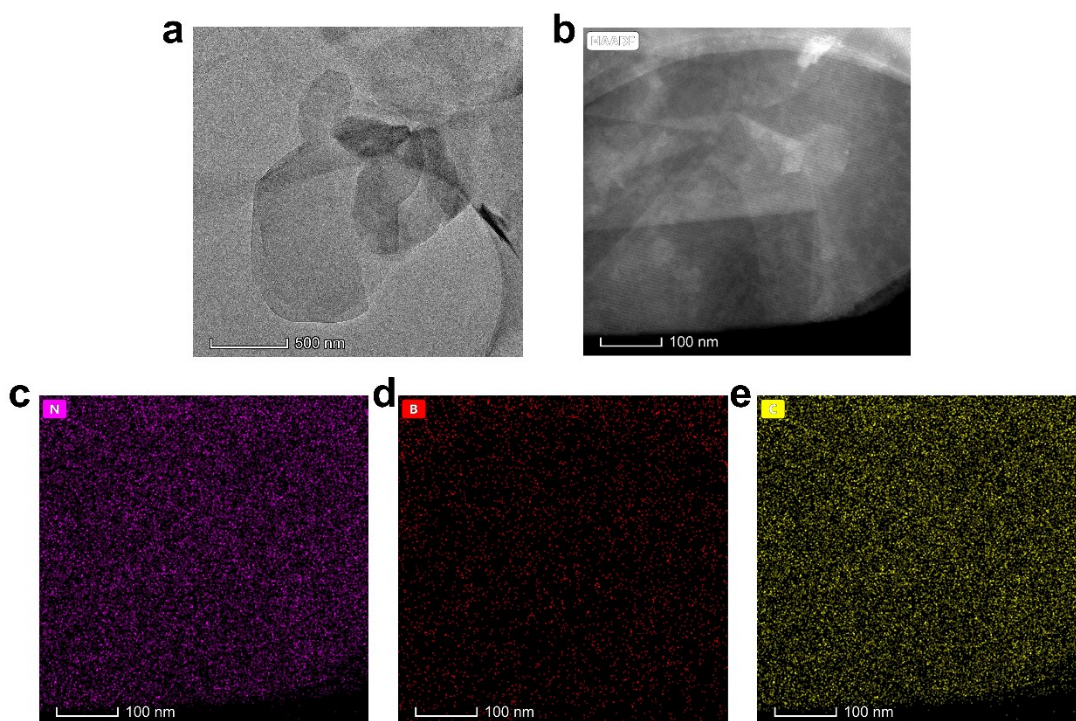


Figure S1. a) The TEM image of selected BN nanosheets (scale bar: 500 nm). b) The TEM image of an individual BN nanosheet (scale bar: 100 nm). c-e) EDX elemental analysis of the individual BN nanosheet, including element maps of c) Boron (pink), d) Nitrogen (red) and e) Carbon (yellow).

S2. The morphology of BN nanosheets by SEM.

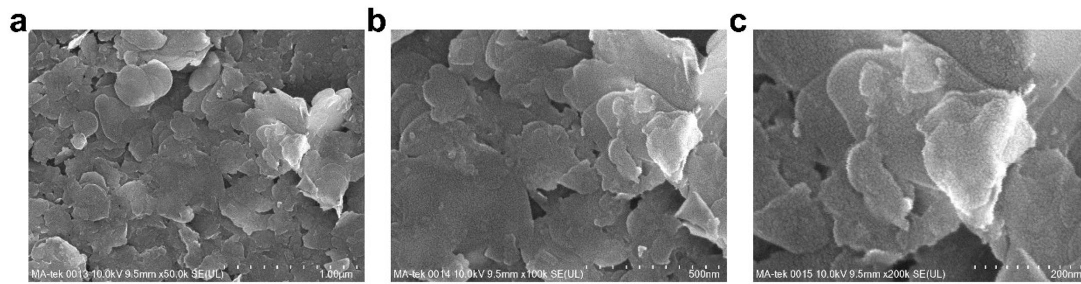


Figure S2. The SEM top-view images of BN nanosheets spin-coated on silicon with scale bar of a) 1 um, b) 500 nm and c) 200 nm.

S3. The XPS and Raman spectra of BN nanosheets.

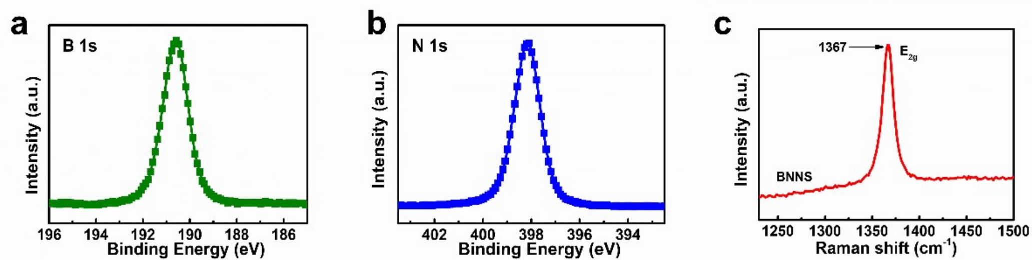


Figure S3. XPS results of the BN nanosheets including a) B 1s spectrum and b) N 1s spectrum. c) Raman spectrum of the BN nanosheets. The peak at 1367 cm^{-1} corresponds to the E_{2g} phonon mode of BN.

S4. Low power consumption of BN- based memristor.

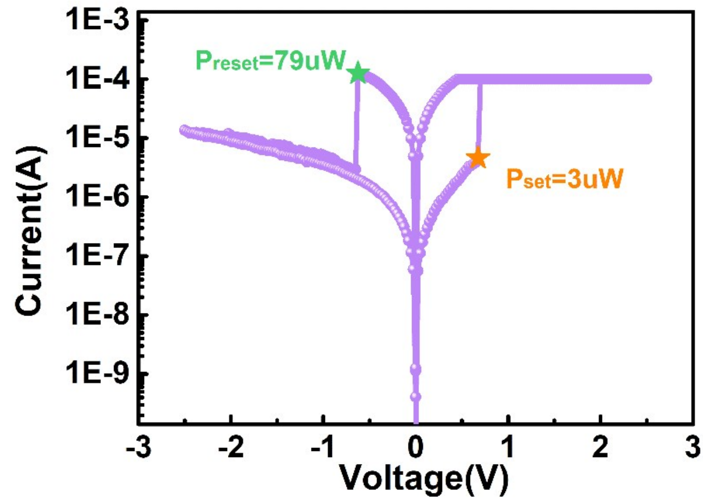
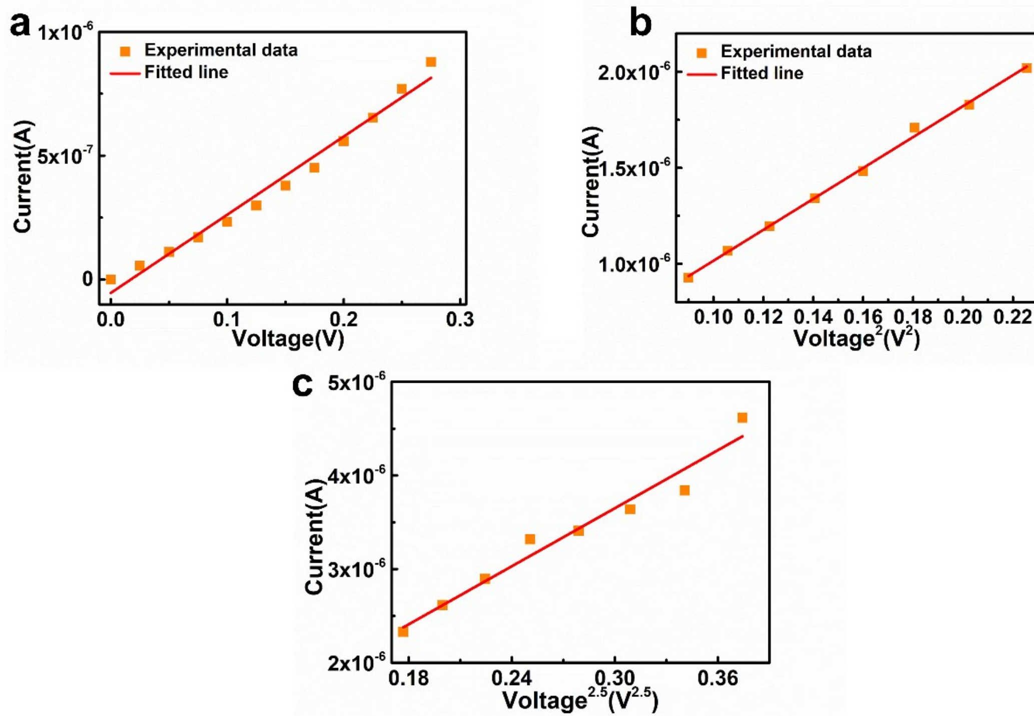


Figure S4. The resistive switching curve of BN- based memristor. The power consumption of device during set and reset processes are 3 μW and 79 μW, respectively. The switching voltage and current of set process is 0.675V and 4.62 μA, respectively. The switching voltage and current of reset process is -0.625V and 126 μA, respectively. Based on the formula of P=U×I, the switching power consumption of device could be calculated.



S5. The fitted conduction mechanisms of device.

Figure S5. Re-plotted positive part of the switching curves of device. a) The fitted I-V curve for Ohmic conduction mechanism (0- 0.275 V). b) The fitted I-V^2 curve for trap-limited SCLC conduction mechanism (0.275 V- 0.475 V). c) The fitted I-$V^{2.5}$ curve for trap-filled limit conduction mechanism (0.475 V- 0.675 V).

S6. The truth table of NAND and NOT logic gates.

Input			Output	
			Not A	NAND
A	B	C	C’	C”
0	0	0	1	1
0	1	0	1	1
1	0	0	0	1
1	1	0	0	0

Figure S6. The logic operations of NAND and NOT logic gates. The NAND logic gate was realized via modulating the logic states of A, B and C’’. The NOT logic gate was realized via modulating the logic states of A, B and C’.

S7. Gradually decreased current under negative voltage sweeping.

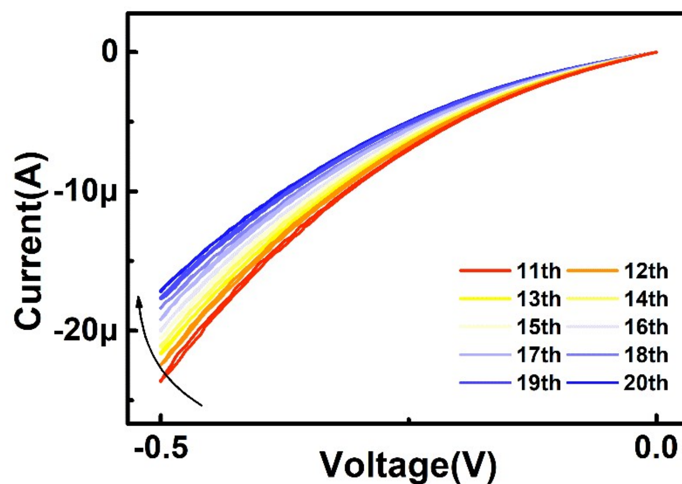
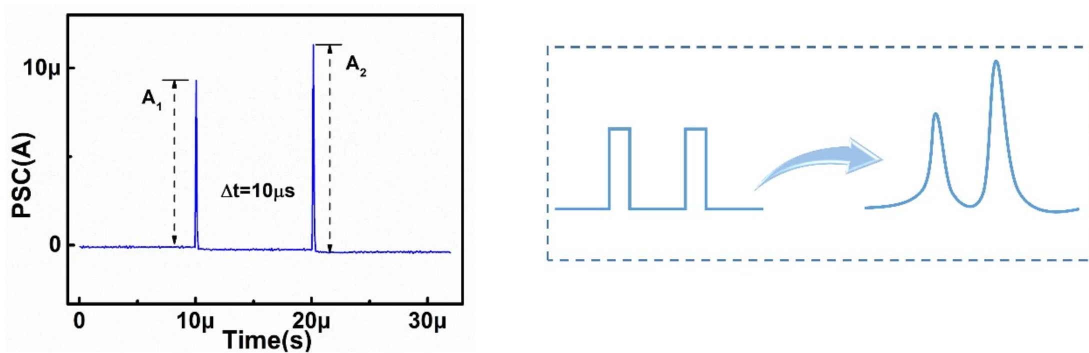


Figure S7. The post- synaptic current of device could decrease under consecutive negative voltage (-0.5V) sweeping, indicating the potential of device as artificial synapse with gradually modulated conductance.



S8. The PPF characteristic of artificial synaptic device.

Figure S8. The PPF characteristic was simulated by artificial synapse device via applying a paired of positive spikes (0.8 V, 1 μs) with interval of 10 μs. Two post-synaptic current spikes were induced and the second current spike is higher than the first one.

S9. The voltage pulses designed for LTP and LTD emulation.

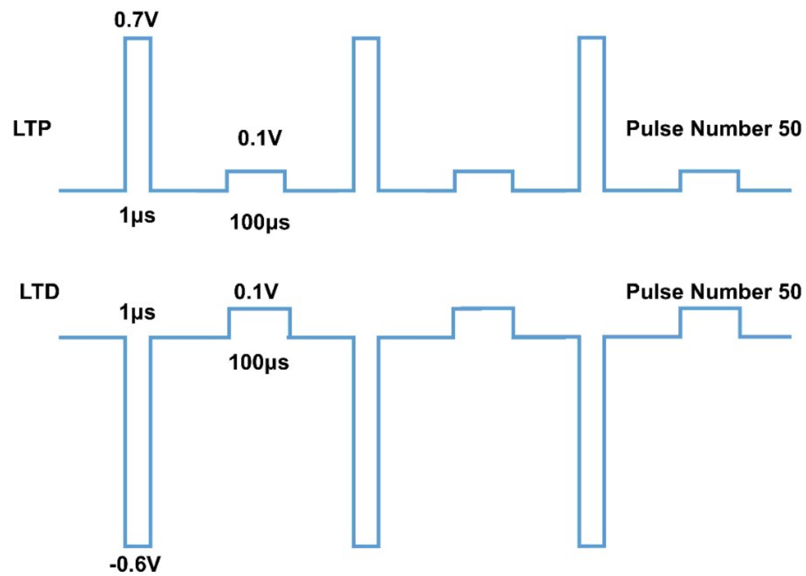


Figure S9. The long-term potentiation and depression of the device were simulated via applying 50 positive pulses (0.7 V, 1 μs) and 50 negative pulses (-0.6 V, 1 μs). The post- synaptic current was monitored via small bias pulse (0.1 V, 100 μs) after each operation pulses. Based on the formula of $\bar{W} = (V^2 \times \Delta G \times t)/N_{pulse}$, the power consumption of LTP/LTD could be calculated.

S10 The long-term retention capability of memristor.

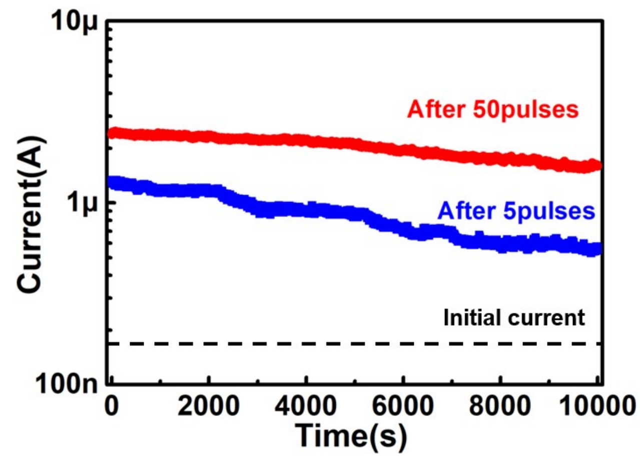


Figure S10. The long-term retention curve of memristor after applying certain pulses (5 pulses and 50 pulses), indicating the long-term retention capability of memristor. The initial current is ~150 nA.

S11 The waveforms of STDP measurement.

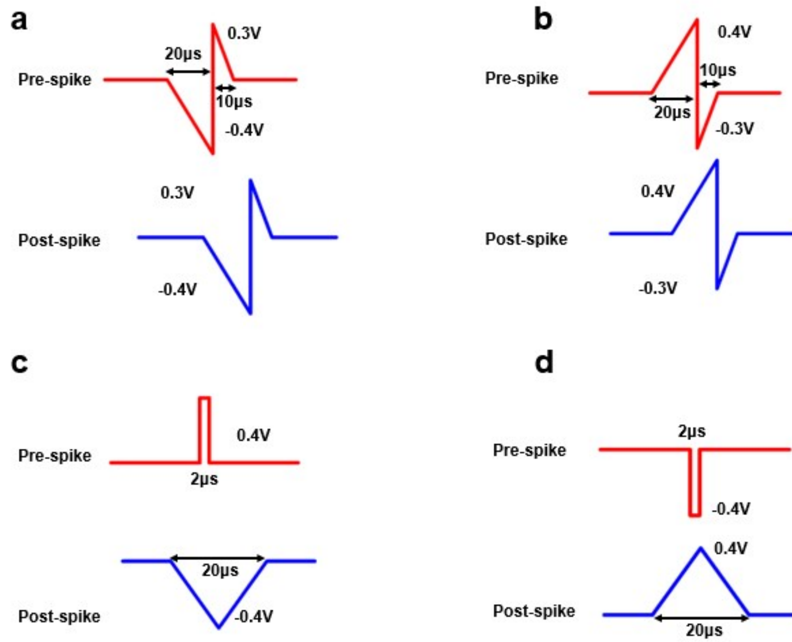


Figure S11. The designed a) asymmetric Hebbian, b) asymmetric anti-Hebbian, c) symmetric Hebbian and d) symmetric anti-Hebbian STDP waveforms.