Electronic Supplementary Information (ESI)

Negative Differential Transconductance Device with Stepped Gate Dielectric for Multi-Valued Logic Circuits

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Ambipolar carrier transport in WSe_2

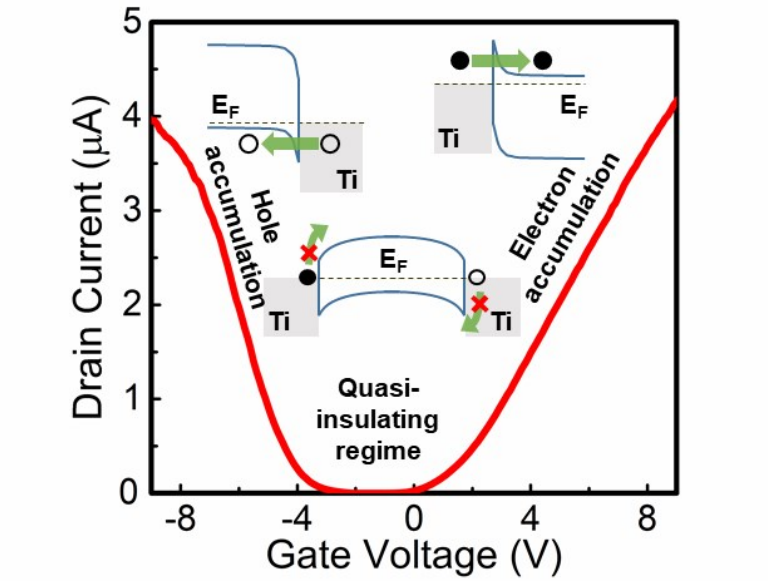

Fig. S1 Ambipolar transfer characteristic of a WSe_2 thin-film transistor with low-work-function Ti contacts. The band diagrams of the Ti/WSe_2 Schottky contact at different gate voltage ranges illustrate three distinct operational regimes: hole accumulation, quasi-insulating, and electron accumulation regimes.

Low-work-function Ti was chosen as a material for the source and drain electrodes to facilitate ambipolar carrier transport in WSe_2 as shown in Fig. S1. Three operational regimes can be distinguished. When Fermi-level of Ti is near the mid-gap of WSe_2 ($V_G \approx$ -1.5 V), both electron and hole injections are hindered by high Schottky barriers, and quasi-insulating regime with minimized drain current is observed. When V_G become more negative (positive) with respect to the quasi-insulating region, the Schottky barrier decreases (increases) for holes and increases (decreases) for electrons, therefore holes (electrons) accumulate in the channel.

Hysteresis width of WSe_2 thin-film transistors with different gate dielectric materials

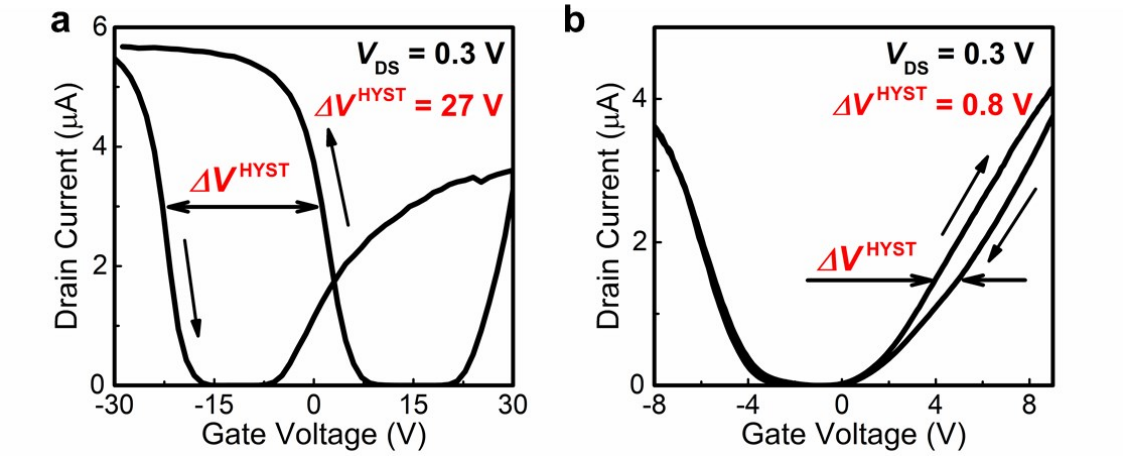

Fig. S2 a, b) Hysteresis width in the transfer characteristics of the WSe_2 thin-film transistors with SiO_2 (a) and *h*-BN (b) as gate dielectrics. Black arrows indicate gate voltage sweep directions.

A superior interface formed between layered WSe_2 and *h*-BN materials, results in a significantly narrowed hysteresis width in the WSe_2/*h*-BN TFT transfer characteristic (ΔV = 0.8 V, Fig. S2b) compared to the WSe_2/SiO_2 TFT transfer characteristic (ΔV = 27 V, Fig. S2a).

Residue-free transfer process by employing the difference in adhesion forces at different interfaces

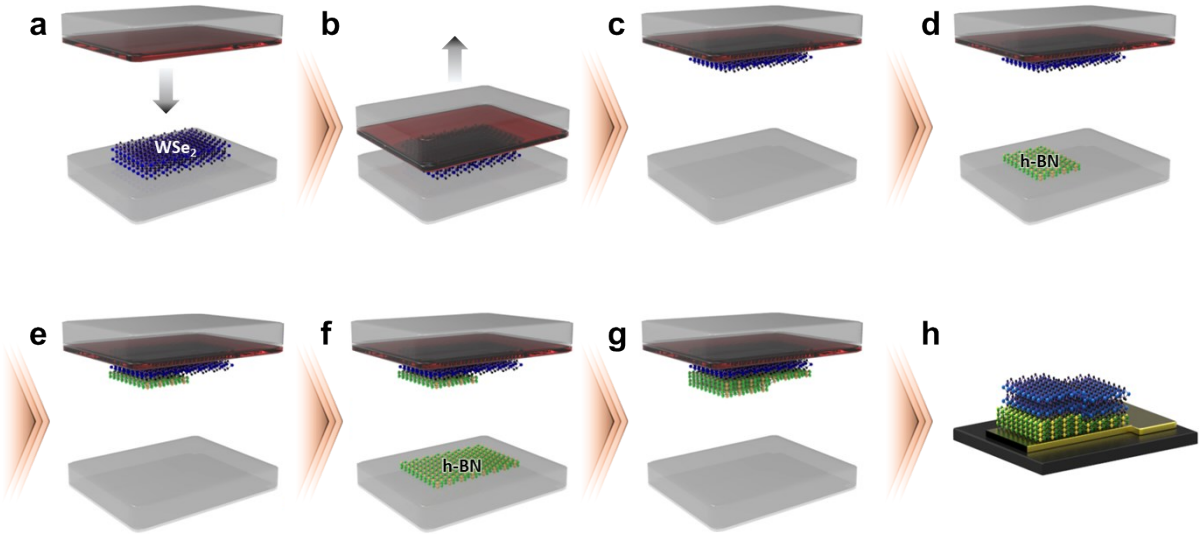

Fig. S3 Step-by-step illustration of the residue-free transfer process by employing the difference in adhesion forces at different interfaces. a) Alignment of the substrate with the polymer layer (top substrate) and the substrate with the exfoliated WSe_2 flake. b) Contacting the polymer layer with the WSe_2 flake. c) Picking the WSe_2 flake. d) Alignment of the polymer layer/WSe_2 stack with the substrate with the first exfoliated *h*-BN flake. e) Picking the first *h*-BN flake. f) Alignment of the polymer layer/WSe_2/*h*-BN stack with the substrate with the second exfoliated *h*-BN flake. g) Picking the second *h*-BN flake. h Transferring the polymer layer/WSe_2/*h*-BN/*h*-BN stack onto the bottom gate electrode and dissolving the polymer layer.

Fig. S3 illustrates the residue-free transfer method employed for single-peak NDTFET fabrication. It exploits differences in the adhesion forces at different interfaces. A flake of WSe_2 and two flakes of *h*-BN are first mechanically exfoliated from their crystals onto different (PDMS) substrates using an adhesive tape. Next, another PDMS substrate is coated with a polymer layer, aligned with the substrate having the WSe_2 flake using a micromanipulator (a), and brought into contact with the exfoliated WSe_2 flake (b). After lifting the substrate covered with the polymer layer, the WSe_2 flake attaches to the polymer layer due to a stronger adhesion force between the polymer layer and WSe_2 than between PDMS and WSe_2 (c). Then *h*-BN flakes were picked from their substrates one by one with polymer layer/WSe_2 stack due to a stronger adhesion force at the interface of WSe_2/*h*-BN than at the interface of *h*-BN/PDMS (d-g). Finally, the polymer layer/WSe2/*h*-BN/*h*-BN stack is transferred onto the substrate with the prepatterned Au back gate (h). The polymer layer is dissolved then in acetone and rinsed in isopropyl alcohol (IPA) to remove remaining polymer residuals.

Stability under multiple measurement cycles

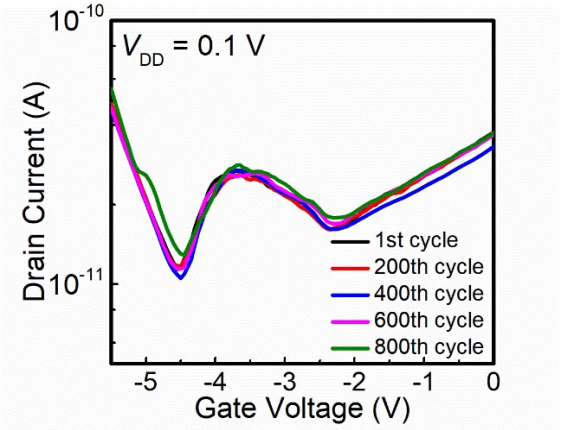

Fig. S4 Transfer characteristics of the NDTFET under multiple measurement cycles.

In Fig. S4, we show transfer characteristics of as-fabricated NDTFET which was tested in multiple cycles of measurements. The transfer characteristics are stable and do not tend to degrade, which is indicative of good overall quality of used materials and interfaces.

Parameters of the NDTFET transfer characteristic

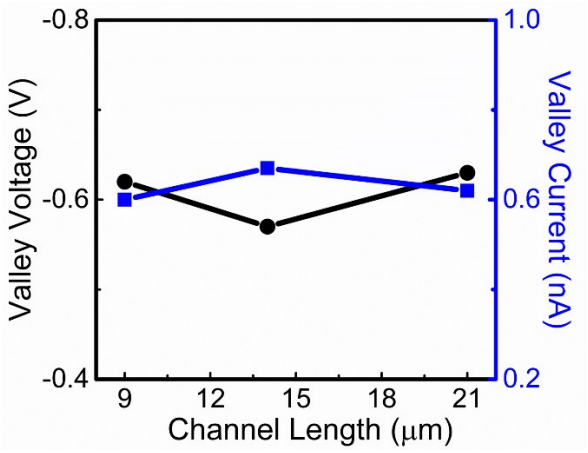

Fig. S5 Parameters of the NDTFET transfer characteristic. Valley voltage and valley current of the NDTFET transfer characteristic as function of the L_T extracted from Fig. 3f.

The valley voltage and valley current are extracted from Fig. 3f and plotted (Fig. S5) as a function of the channel length of the part with a thicker gate dialectic (L_T). Because the current is only weakly affected by L_T for $V_G > V_{PEAK}$ as it was discussed in the main text, I_{VALLEY} and V_{VALLEY} ($V_{VALLEY} > V_{PEAK}$) remain almost constant.

On operation of the quinary inverter

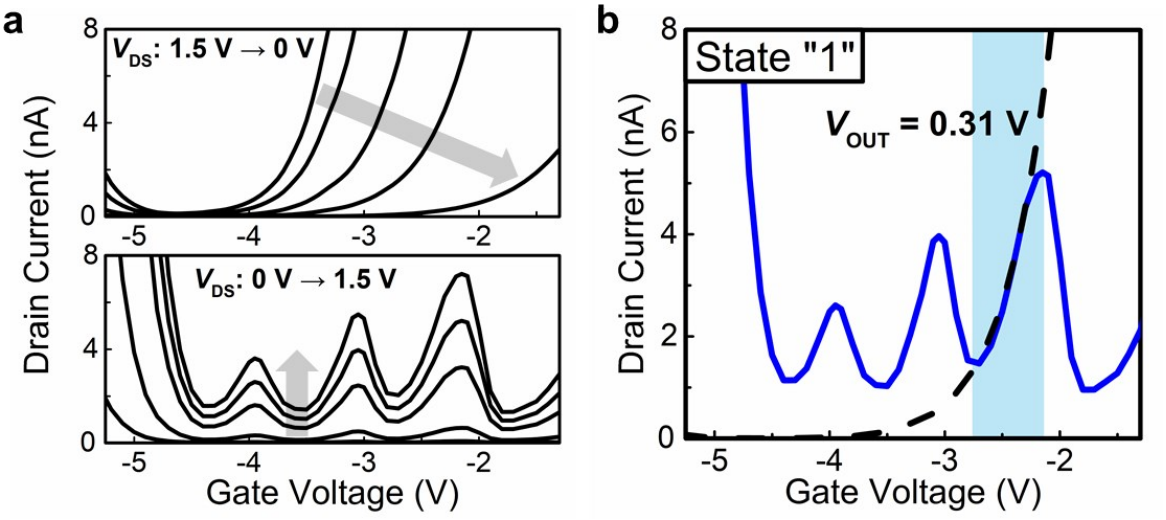

Fig. S6 On operation of the quinary inverter. a) Evolution of transfer characteristics of the load (top panel) and NDTFET (bottom panel) as a function of the drain-to-source voltage (V_{DS}) across them. b) Transfer characteristics of the NDTFET and load for the logic state "1".

During the V_{IN} sweep from -5.25 V to -1.3 V, V_{DD} constantly undergoes redistribution between the NDTFET and load – a larger (smaller) portion of V_{DD} falls across the NDTFET (the load). Fig. S6a illustrates how the transfer characteristics of NDTFET and load devices vary during V_G sweep from -5.25 V to -1.3 V when V_{DS} across the load (the NDTFET) changes from 1.5 to 0 V (from 0 to 1.5 V). Fig. S6b shows the transfer characteristics of the NDTFET and load devices for the logic state "1", corresponding to V_{OUT} of 0.31 V.

Simulated quaternary and ternary inverters

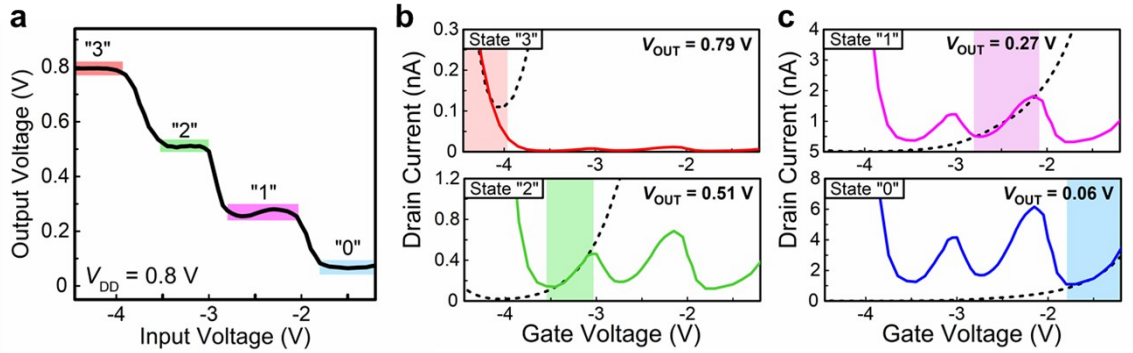

Fig. S7 Quaternary inverter. a) Input–output characteristic of the quaternary inverter. b,c) Transfer characteristics of the NDTFET and load for the logic states "3" and "2" (b); and for the logic states "1" and "0" (c).

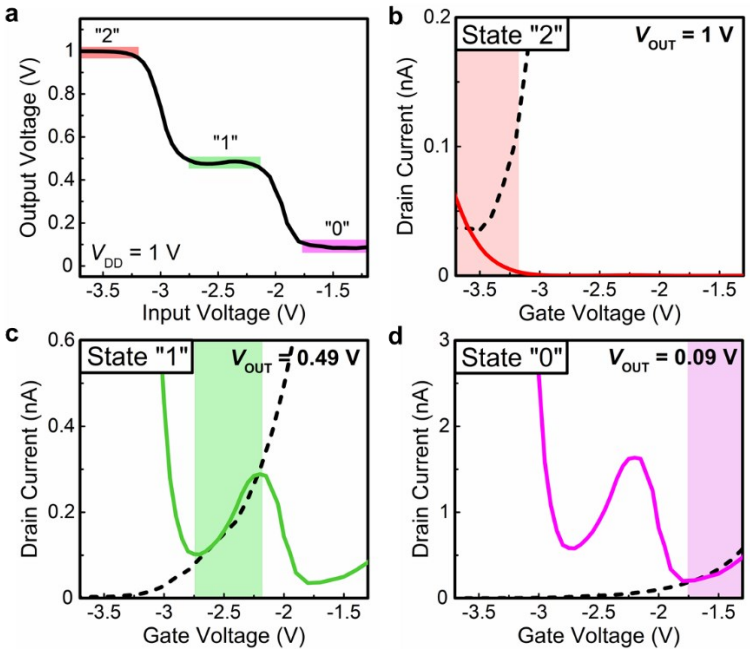

Fig. S8 Ternary inverter. a) Input–output characteristic of the ternary inverter. b-d) Transfer characteristics of the NDTFET and load for the logic states "2" (b), "1" (c), and "0" (d).

The same circuit diagram demonstrated in Fig. 4a can be applied to the quaternary and ternary inverters (Fig. S7, S8). In contrast to the quinary inverter shown in Fig. 4, the NDTFET of the ternary (quaternary) inverter has two (three) parts of different gate dielectric thickness (82 nm and 150 nm for ternary inverter; 82 nm, 150 nm, 212 nm for quaternary inverter). For all demonstrated inverters an ambipolar WSe_2 TFT is utilized as a load. As in case of the quinary inverter, to produce additional logic state(s) for ternary (quaternary) inverters, V_m of the load device is selected to have a more negative V_m than the most negative V_m among two (three) V_m values of the one-peak (two-peak) NDTFETs, which is realized by using thicker gate dielectrics.

Experimental implementation of the ternary inverter

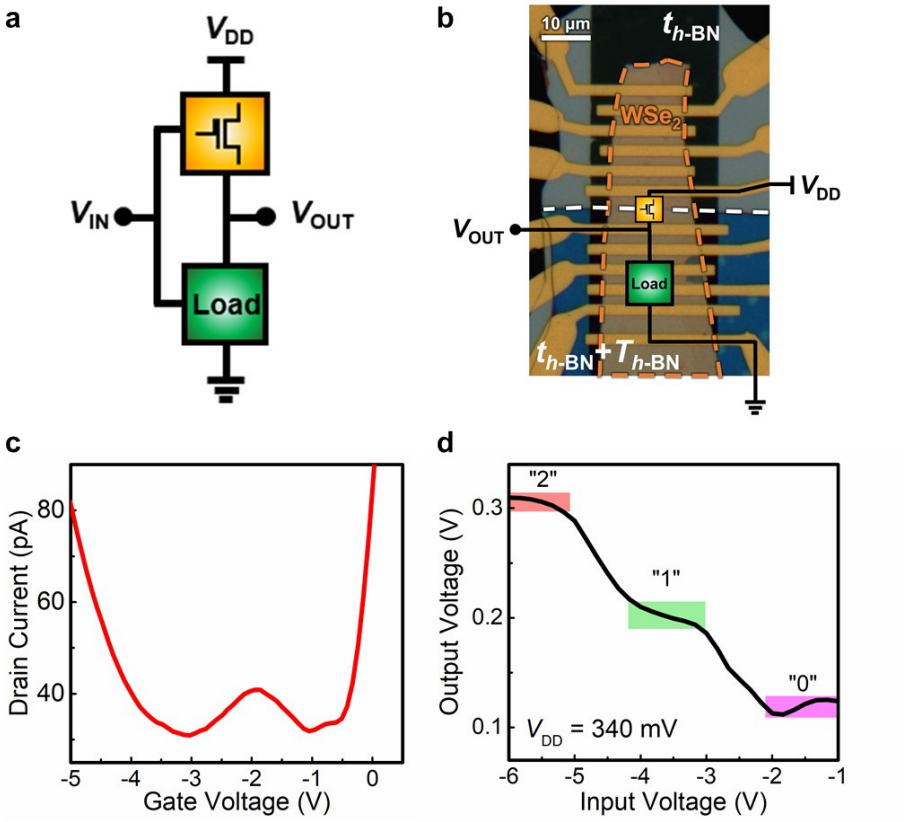

Fig. S9 Experimental implementation of the ternary inverter. a) Circuit diagram of the ternary inverter. b) Top-view optical image of the ternary inverter ($t_{h\text{-BN}} = 51$ nm, $T_{h\text{-BN}} = 170$ nm, $t_{WSe2} = 31$ nm). c) Transfer characteristic of the NDTFET included in the ternary inverter. d) Input–output characteristic of the ternary inverter.

In Fig. S9 we show an experimental implementation of the ternary MVL-inverter and prove the functionality predicted in simulations. The inverter is made with a single WSe2 flake as a channel, where the gate voltage is the input voltage, applied through the back gate. Multiple metal contacts allowed the selection of an optimal load for the NDTFET. Three distinguishable output voltage levels can be observed in Fig. S9d with approximately equal margins between logic states. The input-output voltage characteristics can be further improved with delicate optimization to approach the characteristic in Fig. S8a obtained in simulations. As for inverters with more logic states, they can be realized by further expanding the demonstrated experimental approach for the ternary inverter via increasing the number of gate dielectric steps.

Supplementary Video (MP4): Mechanism of logic states formation of the quinary inverter

The video demonstrates operation principle of the quinary inverter and its mechanism of logic state formation. During input voltage (V_{IN}) sweep, the supply voltage (V_{DD}) continuously redistributes between the NDTFET and load. The graph on the left-hand side shows evolution of transfer characteristics of the NDTFET and load, whereas the graph on the right-hand side indicates corresponding input and output voltages (V_{OUT}) with red circles.