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Supplementary Information

Interaction effects and superconductivity signatures in twisted double-bilayer WSe_2

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Section 1: Fabrication of twisted double bilayer devices

We fabricated twisted double bilayer device by stacking two separated bilayer WSe_2. First, a 20-30nm BN is selected and a pattern for the bottom electrode is designed by e-beam lithography. Then the patterned area of bottom BN is selectively etched by CHF_3 plasma via the reaction ion etching with a controlled etching rate. The etched thickness of bottom BN is usually10nm. Then a 15nm Pt layer is deposited at the patterned area as bottom electrode. This procedure is to make sure that the evenness of the bottom surface is acceptable. The height of the electrode top surface should match the height of bottom BN. This could effectively prevent the formation of bubbles between the bottom electrode and the WSe_2 flake.

The encapsulated twisted double bilayer WSe_2 devices are fabricated by a dry transfer method. Bilayer WSe_2 flakes are first exfoliated on the surfaces of 300nm-thick SiO_2/Si substrates and picked up by another flake of h-BN. The crystal orientation of bilayer WSe_2 is determined by its natural edges. Then, another bilayer WSe_2 flake with straight edges is selected and picked up by the first flake of WSe_2 at a specific twisting angle (4° for device D11, 1° for device E7 and 2° for device F2). The whole process is performed in glove box. We are able to control the twist angle between different layers. Without annealing, the accuracy of the twisted angles is about ± 0.2 degree. But the

device shows poor conductivity (0.1mS) at high carrier density ($6\times10^{12}/cm^2$) at low temperature. After performing annealing at 250℃, the TDBL WSe_2 shows high conductivity (5mS). However, there is always a deviation from the designed twist angles.

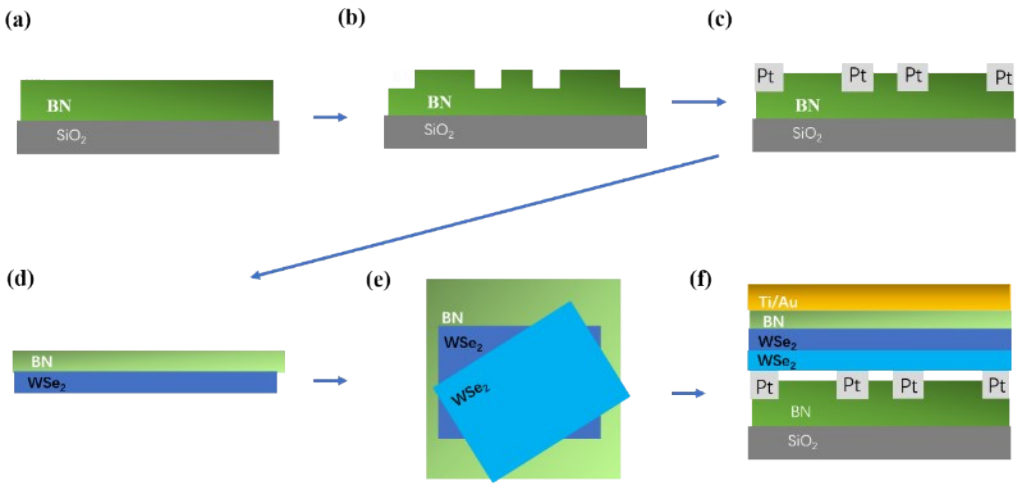

Fig. S1 Fabrication process of twisted double bilayer WSe_2. (a) Selected bottom BN with thicknesses around 20nm to 45nm. (b) and (c) The pattern on the bottom BN is designed by e-beam lithography and selectively etched. Then, a 15nm-thick Pt is deposited as the bottom electrode. (d) The first flake of bilayer WSe_2 (with long straight edges) is picked up by the top BN. (e) Another bilayer WSe_2 is picked up by the hetero-structure and the edge is carefully aligned with the first bilayer WSe_2. (f) The twisted double bilayer WSe_2 is put on the top of pre-patterned bottom electrode.

Section 2: Determination of the twist angles

During the transferring process, we use the optical image to identify the twist angle between two separated bilayer WSe_2 flakes. As shown in Fig. S2, S3, the angle between two long straight edges can be measured. The twist angle for sample #D11 is 3.6° and for sample #F2 is 2.5°. The target angle is set by our rotation motor. In this way, TDBL WSe_2 with twisting angle from 1°to 4° are fabricated.

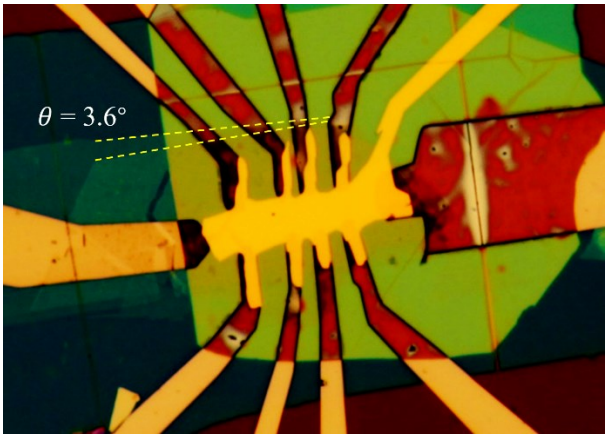

Fig. S2 The optical image of the encapsulated twisted double-bilayer WSe_2 sample #D11.

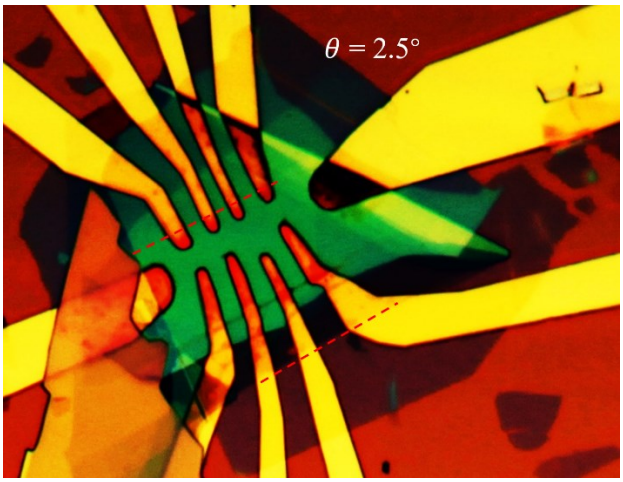

Fig. S3 The optical image of the encapsulated twisted double-bilayer WSe_2 sample # F2.

Section 3: Measuring the thickness of top BN

After stacking the device, the thickness of the top BN is characterized by atomic force microscopy (AFM) as shown in Fig. S4, S5, S6.

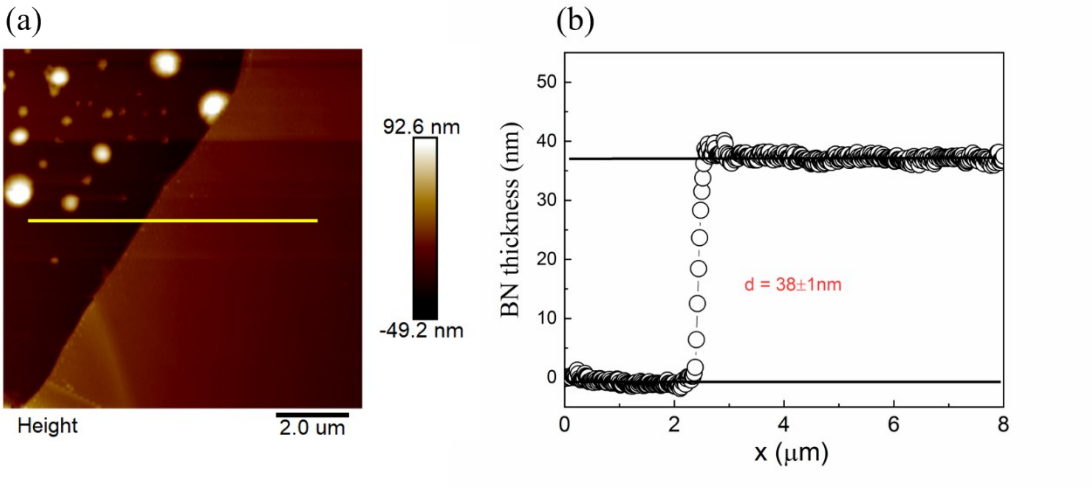

Fig. S4 (a) The AFM image showing the top BN used for twisted double-bilayer WSe_2 sample #D11. (b) Thickness change along the yellow line (a). The thickness of the top BN is 38±1nm.

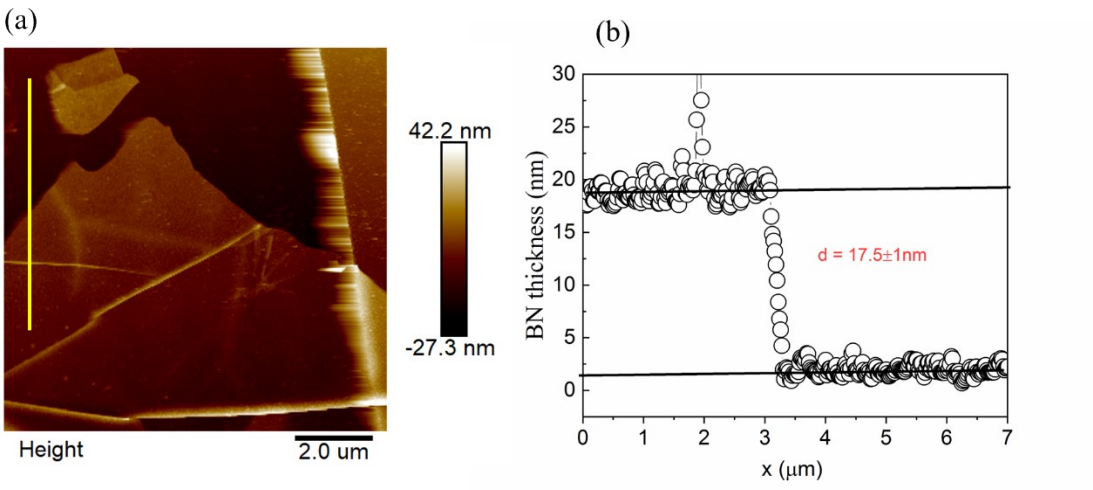

Fig.S5 (a) The AFM image showing the top BN used for twisted double-bilayer WSe_2 sample #F2. (b) Thickness change along the yellow line (a). The thickness of the top BN is 17.5±1nm.

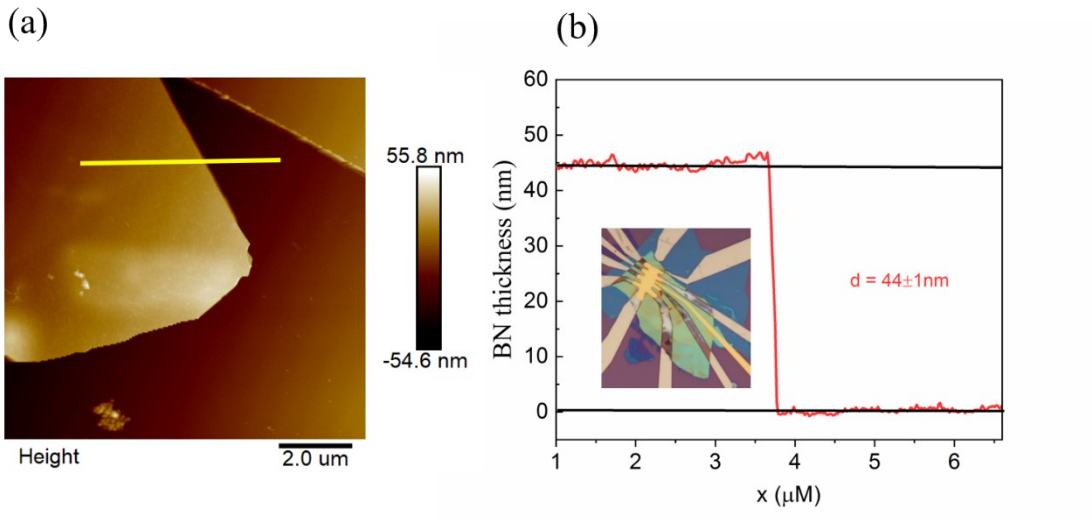

Fig. S6 (a) The AFM image showing the top BN of twisted double-bilayer WSe_2 sample #E7. (b) Thickness change along the yellow line (a). The thickness of the top BN is 17.5±1nm. The inset is the optical image of device #E7

Section 4: Uncertainty of the twist angles

We determined the uncertainty of the twist angles using scanning tunneling microscopy (STM). We used the same fabrication method for preparing the TDBL WSe_2 devices. The TDBL WSe_2 is transferred onto the top surface of a graphite, and a 200℃ thermal annealing is performed. The large-scale STM images (200nm×200nm) show relatively good uniformity of the moiré pattern, indicating that the method we introduced in this work is very effective to control the twist angles between bilayer WSe_2 flakes.

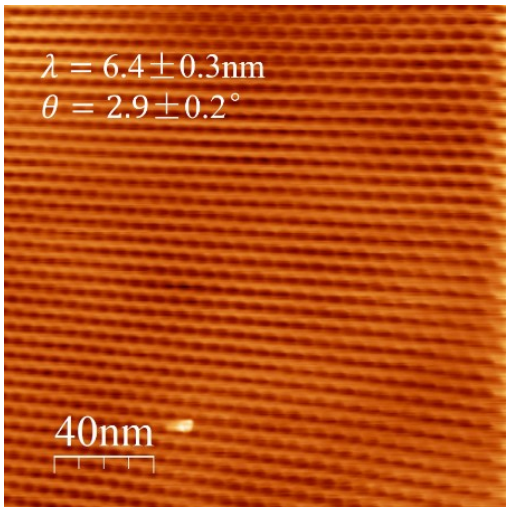

Fig. S7 The STM image of a twisted double bilayer WSe_2 device showing relatively good homogeneity in the observed 200nm×200nm region. The twist angle is set by the rotation stage at 3°. The resulted angle is 2.9±0.2°. Here, the observed moiré lattice wavelength is 6.4±0.3nm.

Section 5: Temperature dependent transport of sample #D11

In the manuscript, the longitude resistance is plotted as a function of the carrier density for sample #D11 in Fig. 2c. We did not perform the four terminal resistance measurement for a wide region of the gate voltage at relative high temperature, because a high gate voltage like -22V causes the breakdown of the 38nm top BN. For temperatures above 100K, we only set the top gate range from 0V to -12V as shown below in Fig. S8.

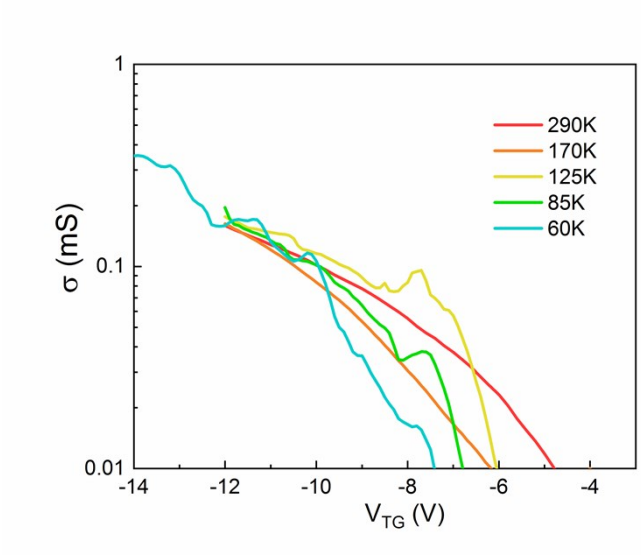

Fig. S8 Temperature dependent four-terminal conductance of twisted double-bilayer WSe_2 devices #D11.

Section 5: Transport properties of few-layer twisted WSe_2

Fig. S9 shows the four-end resistance of a six layer twisted WSe_2 device. The twist angle (about 2.5°±0.2) is worked out through the position of the full filling as a function of carrier density. No pronounced insulating or sudden drop of four-end resistance is

observed, indicating the effects of moiré superlattice become weak when the thickness of the 2D sheets is increased.

All the three devices #D11, #E7 and #F2 we discussed in this manuscript are fabricated by stacking two double bilayer WSe_2. Our experimental results indicated that further increasing the thickness of the 2D sheets did not change the Γ valley band characteristics. But, decreasing the 2D sheet thickness to monolayer, the K-valley band play the role for transport property.

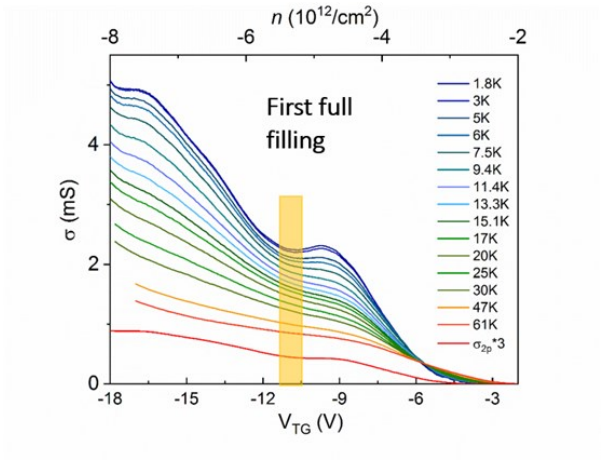

Fig. S9 Temperature dependent four-end conductance of six layer twisted WSe_2.

Section 6: The effects of the displacement fields

For sample #D11, we fabricated a top gate and a bottom gate. The top gate is applied through a 38nm BN and the bottom gate is applied through a 300nm SiO_2 plus a 15nm BN. It means we could control the carrier density and displacement field at the same time. Since the displacement could tune the hopping parameters between layers. The displacement field may have a strong effect on the properties of the flat bands. Fig. S10 is the transport properties for the bottom gate scanning (V_{BG} =30V). Compared with Fig. 2(c), we find that the displacement field has insignificant effects on the transport properties of the devices.

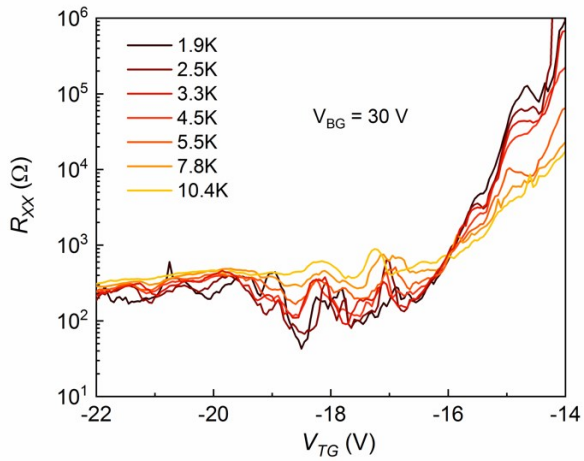

Fig. S10 Longitudinal resistance plotted as a function of the top-gate voltage V_{TG} at different temperatures for Sample #D11. The excitation V_{ds} = 1mV and the back gate V_{BG} = 30 V.

Section 7: Additional transport data from sample #F2

We provide additional transport data for sample #F2. We can see clearly that the four terminal resistance reaches zero with decreasing sample temperature to about 2K.

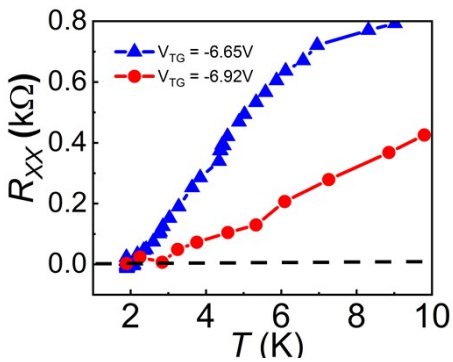

Fig. S11 Four terminal resistance of sample #F2 measured at two gate voltages.