Electronic Supplementary Material (ESI) for Nanoscale.

Supporting Information

Implementation of an Electrically Modifiable Artificial Synapse Based on Ferroelectric Field-Effect Transistor Using Al-doped HfO_2 Thin Film

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1. Microcrystalline structures and compositional analysis of MFMIS gate stack

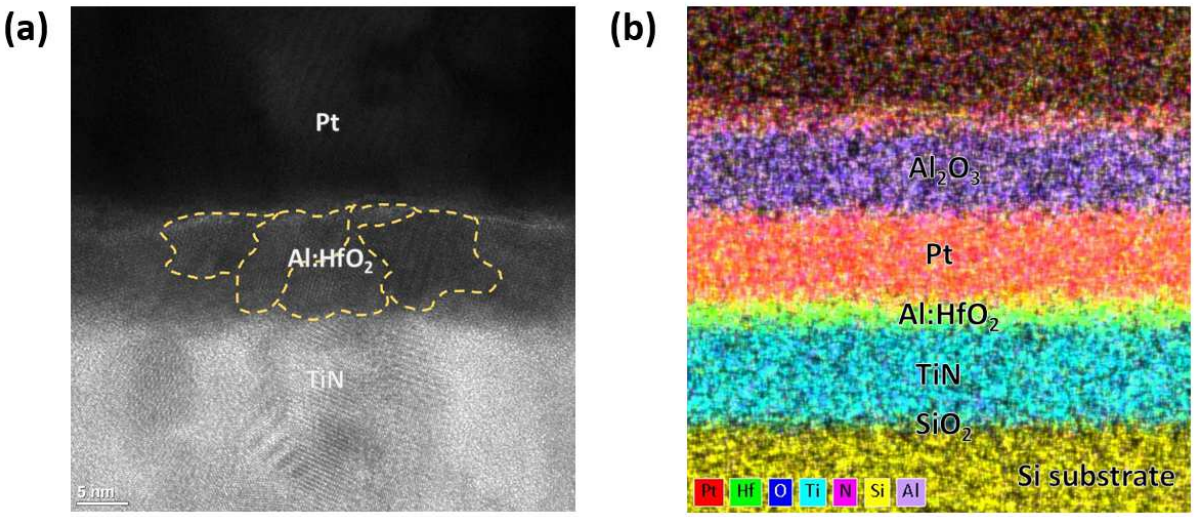

Fig. S1. (a) Magnified bright-field cross-sectional TEM image of the Pt/Al:HfO_2/TiN structure region, in which individual polycrystalline grains are described in dotted yellow lines, clearly showing polycrystalline structures of the Al:HfO_2 ferroelectric thin film. (b) EDS mapping image of the Al_2O_3/Pt/Al:HfO_2/TiN/SiO_2/Si structure. The interfaces were well defined with clear contrasts, resulting in no marked inter-diffusion between the layers.

2. Simple schematic of operation principle for the ferroelectric synapse transistor

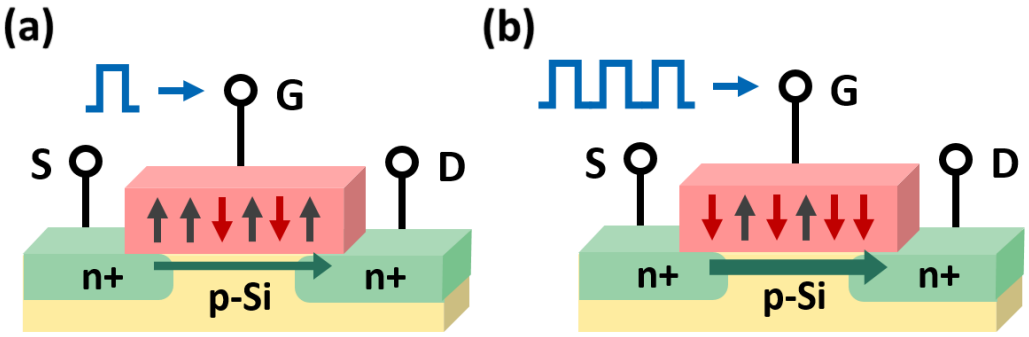

Fig. S2. Variations in channel conductance (regarded as multi-valued synaptic weights) of the FeFETs by partially controlling the ferroelectric polarization of the gate insulator when (a) a small number or (b) a larger number of input signals with given amplitude and durations are applied to the gate terminal. As shown in Fig. S2(a), when a small number of pulses are applied to the gate terminal, only a small value of drain current is obtained during 'read-out' operation. Whereas, when a larger number of pulses are applied, a larger 'read-out' drain current is obtained, since the evolution of switching event for ferroelectric polarizations can be enhanced, as shown in Fig. S2(b). This suggests that a various amount of reversed polarization can be assigned within the Al:HfO_2 ferroelectric gate insulator by controlling the pulse number as well as the amplitude and duration of applied pulses. In other words, the synaptic weights realized by gradually modulated channel conductance of the FeFET can be arbitrarily implemented during the potentiation and depression operations by means of partially modulating the ferroelectric polarization.

3. Excitatory and inhibitory operations of the fabricated ferroelectric synapse transistor

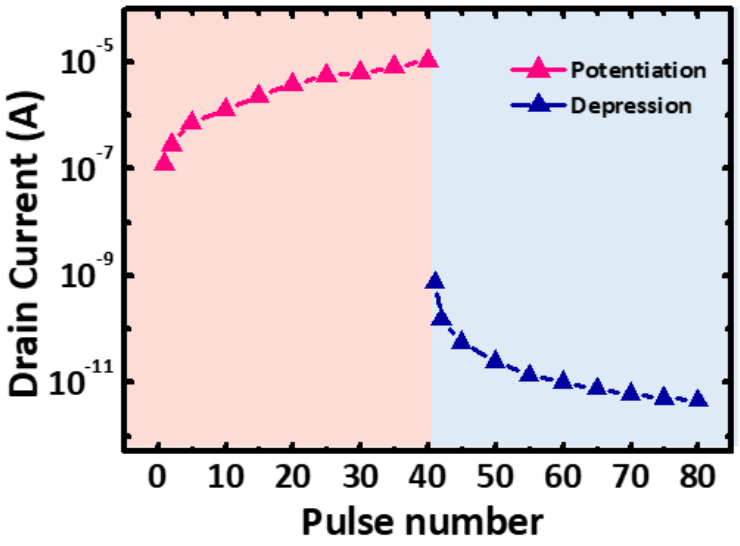

Fig. S3. Variations in drain current values during the excitatory/inhibitory operations of the fabricated MFMIS-FETs with increasing the numbers of potentiation/depression pulses. The pulse amplitudes for excitatory and inhibitory operations were set as +5 and -5 V, respectively, when the pulse width was fixed at 10 μs. The output drain current values were measured at a V_{DS} of 0.5 V. The drain currents were measured to incrementally increase and decrease for each excitatory and inhibitory operations with the evolutions of consecutively applied pulses, respectively, and finally become saturated.

4. Output current responses with variations in time intervals between two pulses for the PPF behaviors of the fabricated ferroelectric synapse transistor

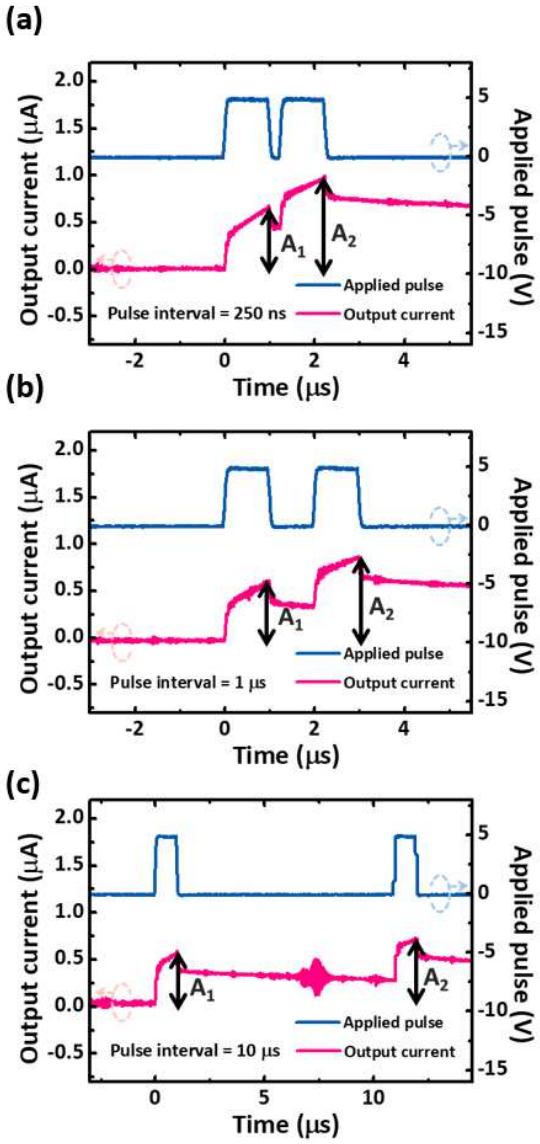

Fig. S4. Output current responses triggered by a pair of input pulse (+5 V, 1 μs) with variations in time intervals of (a) 250 ns, (b) 1 μs, and (c) 10 μs. A_1 and A_2 represent the output currents generated by the first and second pulses, respectively. It is noteworthy that the A_2 decreased with increasing the interval time between two presynaptic spikes, describing the fabricated MFMIS-FETs well emulated the PPF behaviors of synapse devices.

5. Transfer curves of MFMIS-FETs composing the transistor-array structure

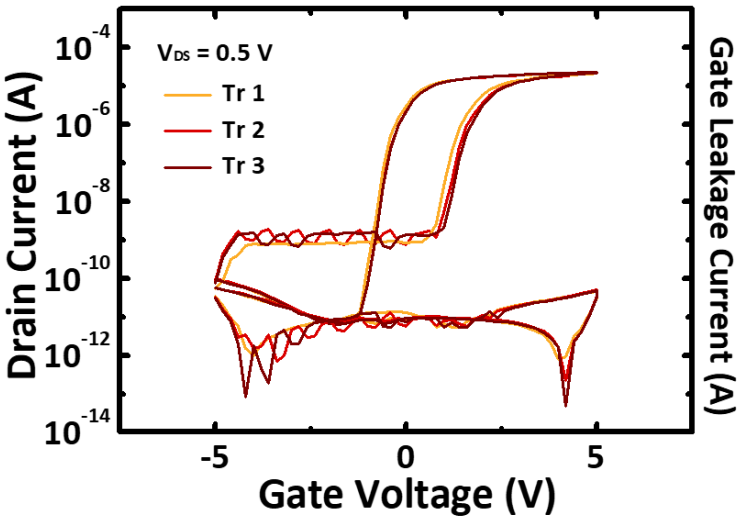

Fig. S5. Variations in I_{DS}-V_{GS} transfer characteristics and gate leakage currents of three transistors located in the same column sharing the same S/D lines. The devices exhibited almost the same operations including ferroelectric memory windows without marked variations.

6. Long-term stability of the programmed currents for the ferroelectric synapse transistor

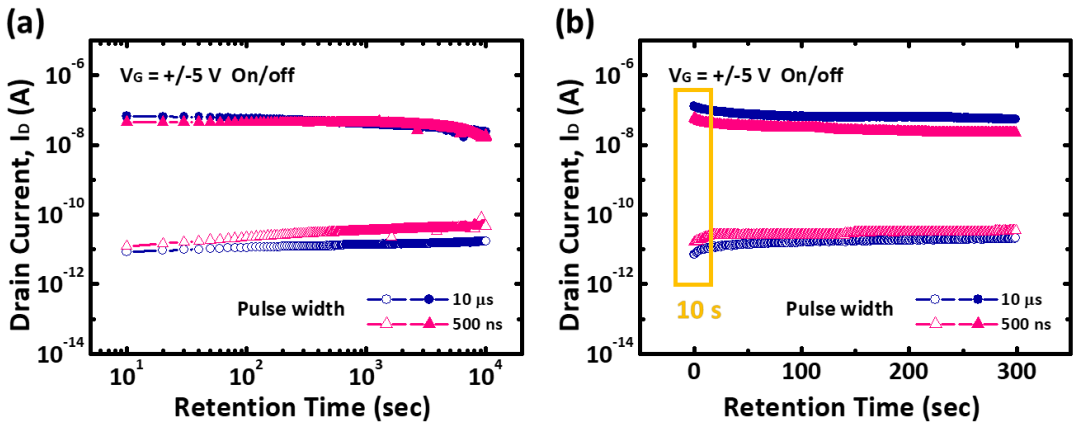

Fig. S6. Variations in the on- and off-programmed I_{DS}'s as a function of retention time with a lapse of (a) 10^4 s and (b) 300 s for the MFMIS-FETs. When the time duration of presynaptic spike was chosen as 10 µs, which is much longer than the switching time of ferroelectric Al:HfO_2 thin films, the device showed stable memory retention characteristics during a retention period of 10^4 s. Alternatively, even when the time duration of presynaptic spike was chosen as 500 ns, which is close to the switching time for the Al:HfO_2 thin films, the device also showed sufficiently stable retention characteristics to implement the LTP behaviors, although the device showed slight degradation of on/off ratio during a retention period of 10^4 s. Furthermore, as shown in Fig. S6(b), it is noticeable that the programmed currents experienced a larger degree of decays during initial 10 s owing to temporarily applied depolarization field generated within the gate stack after the removal of pulse signal. However, these initial decays were quickly stabilized with the evolution of retention time, even when the pulse width was reduced to 500 ns.