Electronic Supplementary Material (ESI) for Nanoscale.

Supporting Information

Multi-terminal ionic-gated low-power silicon nanowire synaptic transistors with dendritic functions for neuromorphic systems

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1. The key process to fabricate IGNWFET

Firstly, the nanowires were patterned by electron beam lithography, and then the modulation gates, source and drain were patterned by optical lithography and formed by reactive ion etching on p-type SOI wafer. The modulation gates are 4 μm away from silicon nanowires and each other. After As^+ implantation at source and drain and thermal activation, a 200 nm SiO_2 layer was deposited as the isolation layer in which the aluminum contacts were formed. After that, a 13μm x 25μm window was opened by the dry etching and wet etching at depth of 550 nm to expose the silicon nanowires for assembling the ionic gels. A 4 nm HfO_2 was then deposited by ALD as the gate dielectric and also the ionic trapping layer. A 2 wt% ionic-liquid-based gel was then made by the methanol dissolved mixture of Polyethylene oxide (PEO) and $LiClO_4$ in mass ratio of 9:1. The ionic gel was spin-coated on the wafer at 6000r/s and patterned by lift-off process. And it was evaporated at 50℃ for 10min to completely remove the methanol and form the polymer electrolyte. The bird-view SEM image of final device were shown in Fig.1 (d). The zoom-in view in Fig.1(e) shows that 40nm-width nanowires have been fully released and suspended due to the lateral over-etching of the buried oxide during the window open.

2. Device structure characterization

To characterize the device structure in a nanoscale level, the cross-section transmission electron microscope (TEM) analysis and energy dispersive X-ray spectrometer (EDS) characterization were carried out and the results were shown in Fig. S2. The height and width of each silicon nanowire are 24 nm and 40 nm, respectively. The 4-nm thick HfO_2 layer uniformly surrounds the nanowires, which plays as an ion trapping layer in the synaptic potentiation process.

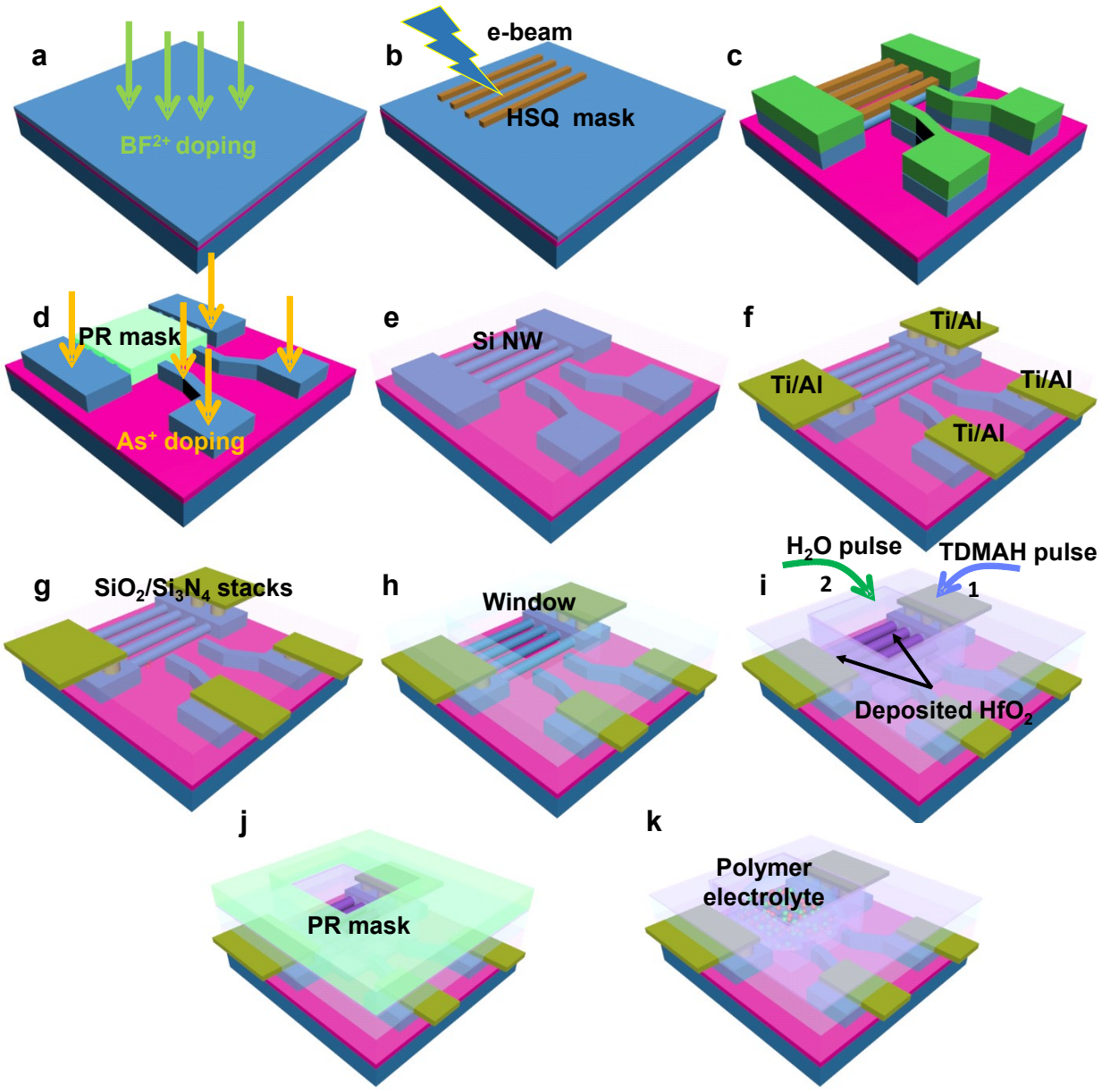


Figure S1. **a,** The SOI wafer with 40 nm thick Si layer was lightly doped with BF^{2+} at 1×10^{16} cm^{-3}. **b,** Electron beam resist here hydrogen silsesquioxane (HSQ) was patterned by e-beam lithography to form nanowire mask. **c,** Optical photoresist was patterned by UV light to form the mask for drain, source and dual coplanar gates, then remove redundant Si film by reactive ion etching. **d,** Source, drain and gates were heavily doped by As^{+} at around 1×10^{20} cm^{-3} to form N-type FET. **e,** The e-beam resist and optical photoresist were removed by buffer hydrofluoric acid

solution and acetone, respectively. A 200 nm thick SiO_2 layer was deposited by LPCVD as isolation layer **f,** Contact holes defined and electrode formation. **g,** 50 nm thick SiO_2 and 500 nm thick Si_3N_4 stacks were deposited as a passivation layer. **h,** The window for polymer electrolyte situating was patterned by UV lithography, and opened by dry etching and wet etching at depth pf 550 nm to expose the silicon nanowires for assembling the ionic gels. **i,** Two consecutive steps were carried out to remove the natural oxide on the nanowire surface and then deposit a 4-nm thick HfO_2 layer using Atomic layer deposition (ALD) at substrate temperature of 300 ℃. **j,** The UV lithography was used to pattern gate region. **k,** Ion gel was spin-coated on the wafer. Then the ion gel was lift-off and evaporated methanol at 50 ℃ for 10 min.

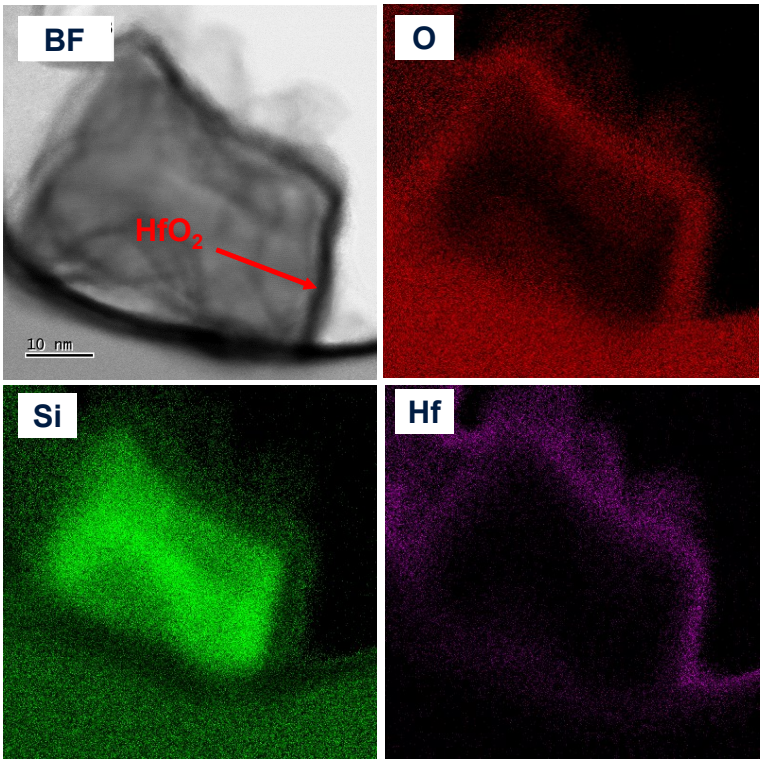


Figure. S2. The cross-section transmission electron microscope of the nanowire and the energy dispersive spectrometer (EDS) mapping of O, Si and Hf elements.

3. The short-circuit test of PE and long-term depression of IGNWFET

To characterize the leakage current of IGNWFETs, the double sweeping short-circuit test of PE was carried out as shown in Fig. S3a, where the distance between two modulation gates is 4 μm. The leakage current reached to about 60 pA with voltage increasing to 5 V, which is much lower than the drain current under the same gate voltage, so it can be neglected in this work. Fig. S3b shows the long-term synaptic depression characteristics of IGNWFETs, where the drain current reduced by 32.83% compared with the initial current value, it is supposed to be related to the Li^+ extrusion from HfO_2 dielectric.

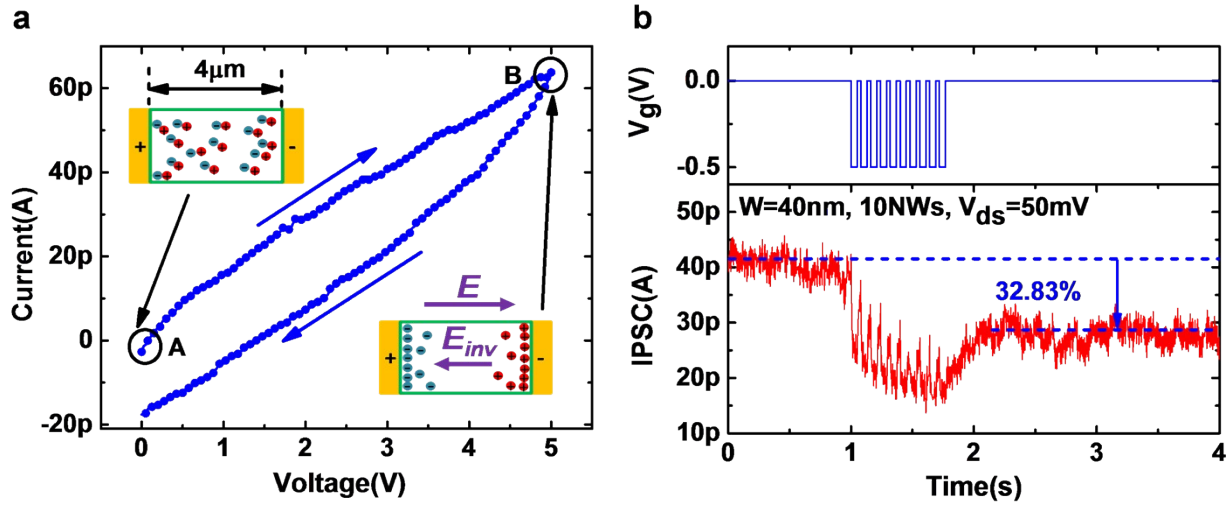


Figure S3. a, The double sweeping short-circuit current of the polymer electrolyte. **b,** The long-term depression triggered by a train of negative voltage pulses (-0.5 V, 50 ms) to show current reduction by 32.83%.

4. Tunnable conductance

To test the modulation of nanowire conductance at different pulse amplitudes, a series of 10 consecutive pulse trians with the same duration time but different amplitude were applied, the

relative conductance change ($^{\Delta w/w_0}$) was detected after 2s, the continuously conductance update was obtained as shown in Fig. S4b. On the other hand, the modulation of nanowire conductance with different pulse widths was shown in Fig. S4c and Fig. S4d. It indicates the nanowire conductance can be flexibly modulate the nanowire conductance by regulating the stimuli duration and intensity.

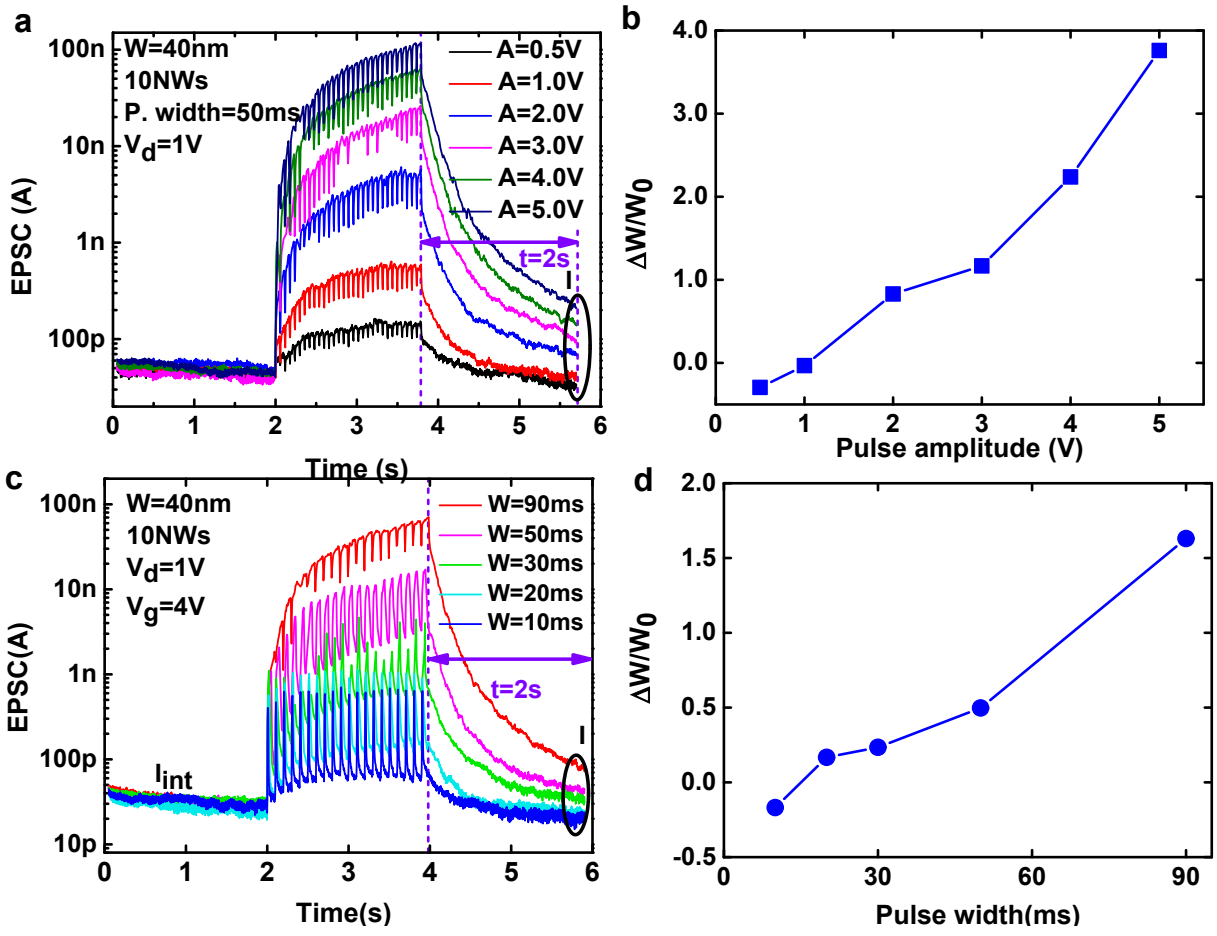
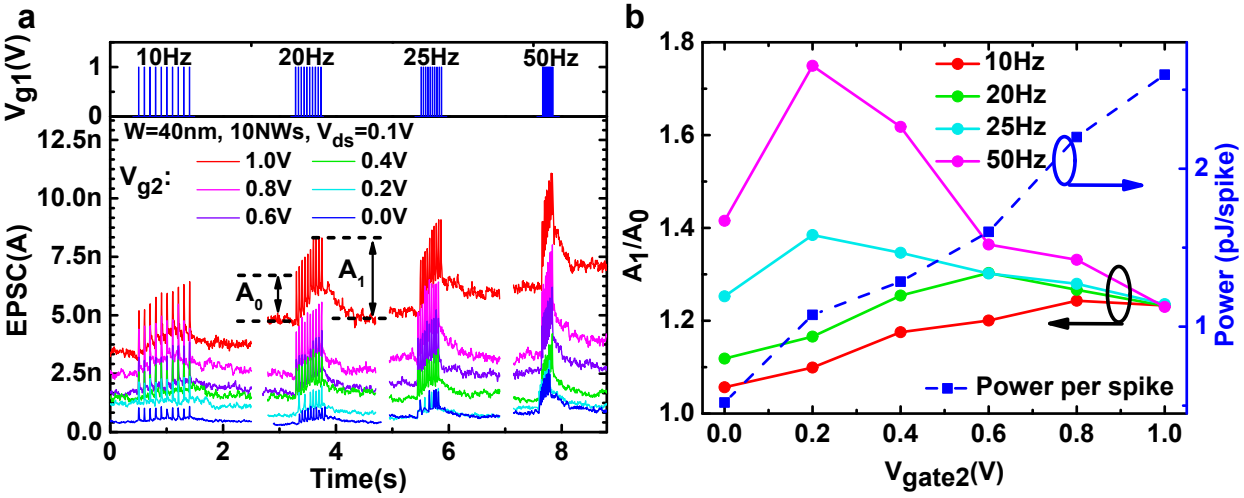


Figure S4. The EPSC modified by a series of pulses with different **(a)** amplitude and **(c)** width versus time, and the difference between I and I_{int} is defined as the change of weight ($^{\Delta W}$). **(b)** and **(d)** are the extracted results.

5. The spiking rate-dependent gain modulated by steady voltage bias

Firstly, the EPSC gain (A_1/A_0) increased when the gate2 was biased at relatively low voltage because extra Li^+ ions accumulated at the HfO_2/PE interface. Eventually, the EPSC gain triggered by a train of pulses with different frequency decayed to a stable value, which is attributed to most of Li^+ ions moved to HfO_2/PE interface driven by the steady voltage bias and caused strong repulsive to subsequent Li^+ ions, thus reduced the sensitivity of nanowire conductance to frequency-coded pulses.



Meanwhile, there is larger A_1/A_0 under the stimulus with higher frequency, the frequency-dependent characteristics are attributed to the limited dispersion rate of ions in the PE. In addition, energy-consumption per spike with 10 Hz stimuli increased linearly with the increasing of V_{gate2}, which is mainly caused by the enhanced peak current. In summary, A_1/A_0, energy per spike and current driving capability can be tuned efficiently by the modulation gate.

Figure S5. a, The EPSC activated by 10 gate1 pulses (1 V, 10 ms) with different frequency under different gate2 biases. **b**, The EPSC gain and energy efficiency per spike dependent on V_{gate2}.

6. "AND" logic based on IGNWFET

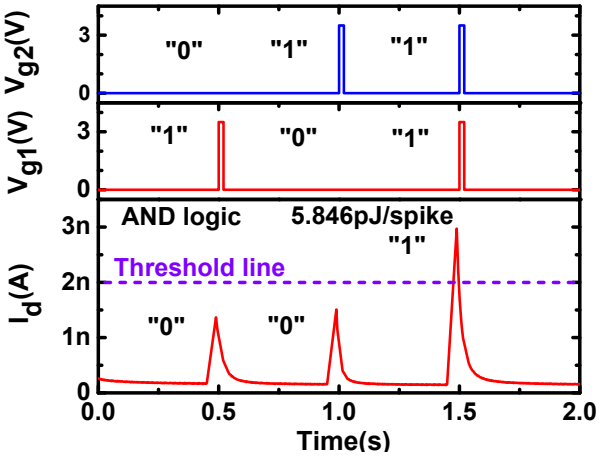


Figure S6. The dynamic "AND" logic realized based on IGNWFET, where the threshold line is set to 2nA. Besides, the energy-consumption per spike is 5.846 pJ/spike, which is comparable to the advanced reported synaptic transistors[4,5].

7. The mechanism of ion migration

As shown in Fig. S7, the cations, here Li^+ ions were attracted to the nanowire surface and piled up to induce the inversion charge to turn the device on. With the increase of Li^+ ion accumulated on the nanowire surface, the ion diffusion driven by the concentration gradient and the ion drift determined by the external electric field reached dynamic equilibrium, so there is no ionic current density anywhere at this steady state, this case can be expressed by equation (1) and its solution is shown in (2).

$$J = -D\frac{\partial C}{\partial x} + vC = 0 \quad (1)$$

$$\Rightarrow C(x) = C_0 \exp\left(-\frac{v}{D}x\right) = C_0 \exp\left(-\frac{q\mu E}{D}x\right) \quad (2)$$

Where C is the ionic concentration, D is the diffusion coefficient, E is the external electric field, v and μ are ion migration velocity and mobility, respectively. The constant total number of Li^+ ions per unit area (N) can be obtained by integrating the ion concentration in the whole region.

$$N = \int_0^L C_0 \exp\left(-\frac{q\mu E}{D}x\right)dx \tag{3}$$

$$\Rightarrow C_0 = \frac{q\mu EN}{D(1 - exp(-\frac{q\mu EL}{D}))} \tag{4}$$

The cations (Li^+) distributed within the Debye length (λ) range at the boundary can induce the charge on the nanowire surface. After considering the effect of Debye length, the calculated effective ionic surface concentration (n_s) around the nanowire is shown in equation (5), and the induced nanowire conductance enhances with the increased electric field as shown in equation (7), where the Debye length is much shorter than the distance between gate and nanowire surface.

$$n_s = \int_0^\lambda C_0 \exp\left(-\frac{q\mu E}{D}x\right)dx = N\frac{1 - \exp\left(-\frac{q\mu E\lambda}{D}\right)}{1 - \exp\left(-\frac{q\mu EL}{D}\right)} \tag{5}$$

$$\sigma = \frac{2q\mu_n}{R}n_s = \frac{2q\mu_n N}{R}\frac{1 - \exp\left(-\frac{q\mu E\lambda}{D}\right)}{1 - exp\left(-\frac{q\mu EL}{D}\right)} \quad (\lambda \ll L) \tag{6}$$

$$G = \frac{\sigma S}{L_g} = \frac{2\pi q\mu_n NR}{L_g}\frac{1 - \exp\left(-\frac{q\mu E\lambda}{D}\right)}{1 - exp\left(-\frac{q\mu EL}{D}\right)} \quad (\lambda \ll L) \tag{7}$$

Where μ_n is the electron mobility and R is the radius of the silicon nanowires. The ions trapped in the HfO_2 thin film can affect the carries on the nanowire channel surface through electrostatic induction and remote Coulomb scattering, which can affect the expression of the relationship between the

channel conduction and the applied electric field in equation (7). After reaching the steady state, the number of ions finally inserted into the HfO_2 determined by the strength of external electric field. The diffusion process of ions is quite different between the polymer electrolyte and HfO_2 dielectric. For example, the ionic mobility in HfO_2 film is much smaller than that in PEO electrolyte[8], so trapped ions in HfO_2 cannot diffuse into electrolyte within short time. Therefore, the influence of trapped ions in thin HfO_2 on the channel conductance in a short time can be regarded as constant. Based on the above analysis, we have modified the derivation of the ion transport mechanism and the corresponding equation (7) and obtain the equation (8).

$$G = G_H(E) + \frac{\sigma S}{L_g} = G_H(E) + \frac{2\pi q \mu_n N R}{L_g} \frac{1 - \exp\left(-\frac{q\mu E\lambda}{D}\right)}{1 - exp\left(-\frac{q\mu EL}{D}\right)} \quad (\lambda \ll L) \tag{8}$$

Where $G_H(E)$ is a constant representing the channel conductance induced by the trapped ions in HfO_2 determined by the strength of external electrical field.

After the removal of external electric field, the Li^+ ions started to diffuse away from the nanowire surface. With the semi-infinite approximation at the boundary of the gate electrode, the second Fick equation can be solved and give the final calculated nanowire conductance as shown in the following equation (9).

$$\begin{cases} \dfrac{\partial C}{\partial t} = D\dfrac{\partial^2 C}{\partial x^2} \quad 0 \le x \le L \\ \dfrac{\partial C}{\partial x}\Big|_{x=L} = 0 \\ C(x,0) = \varphi(x) = \dfrac{q\mu EN\exp\left(-\frac{q\mu E}{D}x\right)}{D\left(1 - exp\left(-\frac{q\mu E}{D}L\right)\right)} \end{cases} \tag{9}$$

As shown in equation (10), its corresponding solution can be expressed in the form of infinite series, and the corresponding coefficients are calculated in formula (11). After considering that only the Li^+ ions within the Debye length range makes contribution to induce the inversion electrons in nanowire channel, the nanowire conductance can be derived as shown in equation (12), and it can be further simplified to equation (13).

$$C(x,t) = T_0 + \sum_{k=1}^{\infty} A_k exp\left(-\frac{k^2\pi^2}{L^2}Dt\right)\cos\left(\frac{k\pi}{L}x\right), k = 1, 2... \tag{10}$$

$$\begin{cases} T_0 = \frac{1}{L}\int_0^L \varphi(x)dx = \frac{N}{L} \\ A_k = \frac{2}{L}\int_0^L \varphi(x)\cos\left(\frac{k\pi}{L}x\right)dx, \quad k = 1, 2... \end{cases} \tag{11}$$

$$G = \frac{2\pi q\mu_n R}{L_g}\int_0^{\lambda} C(x,t)dx = \frac{2\pi q\mu_n R}{L_g}T_0\lambda + \sum_{k=1}^{\infty} A_k \frac{2Lq\mu_n R}{kL_g}\sin\left(\frac{k\pi\lambda}{L}\right)exp\left(-\frac{k^2\pi^2}{L^2}Dt\right) \tag{12}$$

To simplify the complex computation in equation (13), only item with k=1 is kept and higher order items are neglected to obtain equation 14, there is negative correlation between $\ln(G - G_0)$ and time (t). The larger extracted slope of channel conductance-related term $\ln(G - G_0)$) to decayed time (t) indicates higher diffusion coefficient with higher gate bias, as shown in Fig. 6b, which is attributed to the stronger repulsive force between charges due to higher accumulated Li^+ ions.

$$G = G_0 + \sum_{n=1}^{\infty} A_n exp\left(-\frac{k^2\pi^2}{L^2}Dt\right) \tag{13}$$

$$ln(G - G_0) = ln(A_1) - \frac{\pi^2}{L^2}Dt \tag{14}$$

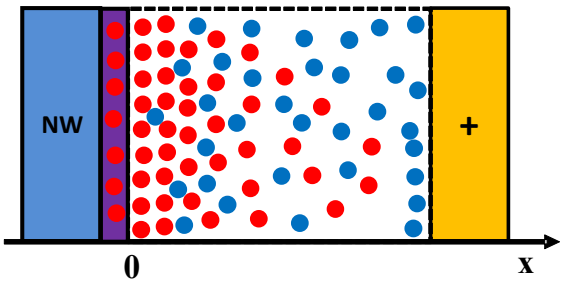


Figure. S7. The distribution of anions and cations in the region between gate and nanowire at dynamic equilibrium.

8. The influence of the input pulse sequence

In order to characterize the impact of the input pulse sequence on the EPSC strength and neuronal gain (A_1/A_0), two pulse trains with the frequency combinations ("gate1: 50Hz, gate2: 25Hz" and "gate1: 25Hz, gate2: 50Hz") are applied to two gates, the drain-source voltage (V_{ds}) is fixed at 0.5V for EPSC measurements, as shown in Figure. S8. The neuronal ESPC gain in these two cases are 11.588nA/0.522nA =22.199 and 12.028nA/0.539nA =22.315, which means that the pulse sequence has little effect on the device electrical performance.

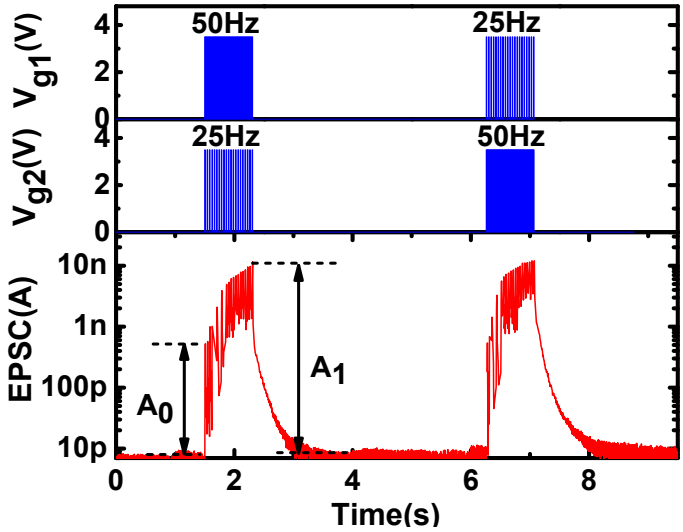


Figure. S8. The influence of the input pulse sequence on EPSC strength and neuronal EPSC gain

(A_1/A_0).

9. The sensitivity to frequency combinations

In order to obtain the exact value of the sensitivity limit, the stimulus trains with different frequency combinations (such as "1.25Hz Add 1.25Hz", "5Hz Add 5Hz" and so on) were applied, the extracted EPSC gains (A_1/A_0) were shown in Figure S9b. For a crude estimation of the sensitivity limit, the pulse signal input to the two gates in each combination is same. It can be seen that when input "5Hz Add 5Hz", the corresponding EPSC gain is 2.12. However, when the input frequency drops to "1.25Hz Add 1.25Hz", the corresponding EPSC gain dramatically decreased to 1.10. It implies that when the input frequency changes by 3.75Hz, the EPSC gain still exhibit a high sensitivity to the input frequency combination. The parameter that determines the sensitivity limit is the ionic mobility. When the ions migrate fast in the electrolyte, the ions drifted by the previous pulse to the nanowire surface have completely diffused to equilibrium positions, thereby not enhancing the subsequent EPSC so that the EPSC gain value closes to 1. As the frequency continues to increase, it still shows high sensitivity when the input frequency combination is increased to "50Hz Add 50Hz". It is presumably that due to the limited ionic mobility and long relaxation time, the EPSC gain value will reach saturation after increasing to a certain frequency. However, in Figure S9b, due to the trade-off between the sampling frequency and current integration time in the rapid measurement equipment, we cannot accurately sample the EPSC peak value (<1nA) triggered by shorter pulses with short interval (<2ms) thus it's difficult to effectively evaluate the limit of sensitivity in relatively high frequency region, which will be considered in our future work.

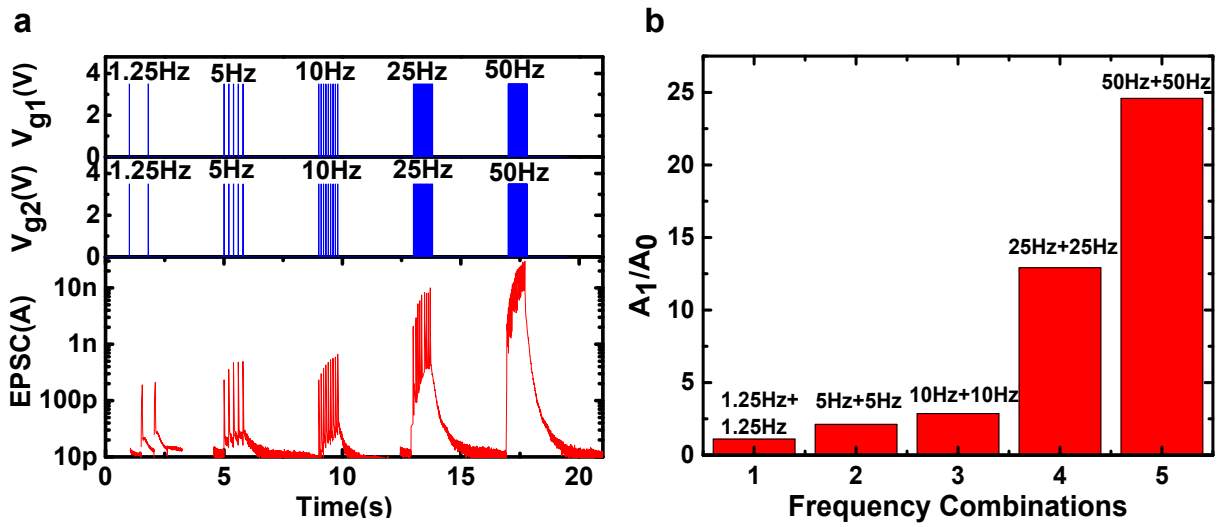


Figure. S9. a, A sample "Add" operation deals with "1.25Hz Add 1.25Hz", "5Hz Add 5Hz" and so on. The input signals have same stimulus width (10ms) and same total length (810ms) but with different frequency combinations. **b,** The EPSC sensitivity (A_1/A_0) measurement results for different frequency combinations in **a**.

10. The gate leakage characteristics

To quantitatively compare the gate leakage current with drain current, gate current and drain current were monitored simultaneously when the gate bias was swept from -5V to 5V as shown in Fig. S10a. When the gate voltage is lower than 1V, the gate leakage current cannot be ignored compared with the drain current, which may be caused by trap-assisted tunneling in amorphous HfO_2 layer. However, the gate leakage current is much lower than the drain current when gate voltage is larger than 2V, so they can be neglected in this work. To characterize the leakage current of the 2nm thick HfO_2 layer, a 50μm × 50μm TiN/HfO_2/p-Si/Al stack capacitor was

fabricated and direct sweeping test was carried out as shown in Fig. S10b. When a voltage of 3V was applied, current density increased to 37.95mA/cm^2 due to the enhanced tunneling probability and thermoelectric emission probability. The gate leakage current of IGNWFETs was calculated to 455pA, which is deduced from the product of the current density and statistical nanowire surface area. In practice, the HfO_2 layer and the PE layer are connected in series to play as the gate dielectric, the 4μm thick PE layer has larger resistance and thus shares a significant portion of the gate voltage. So the actual gate leakage current is lower than 455pA.

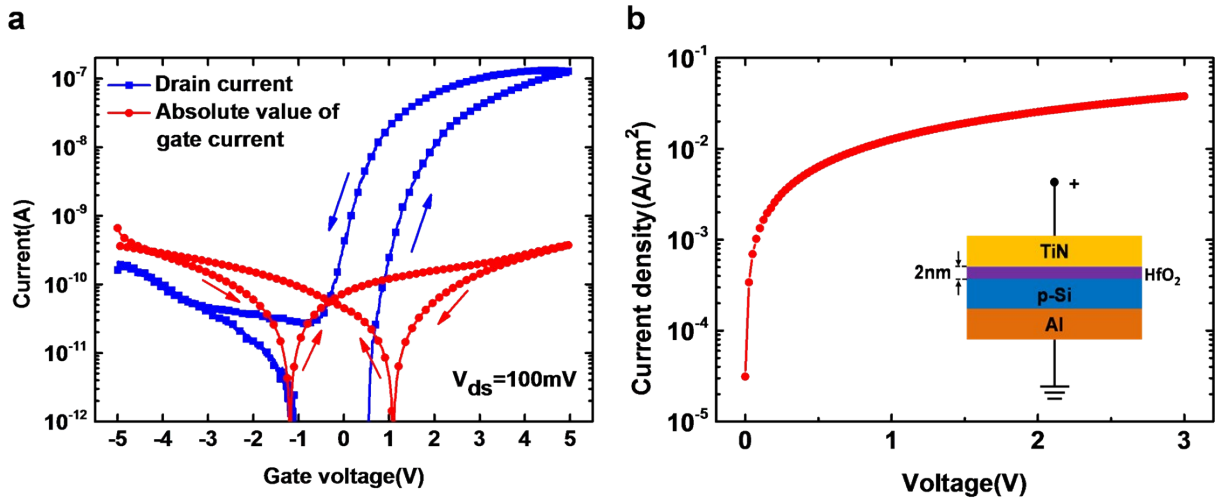


Figure. S10. a, The output current of drain terminal and gate terminal when gate voltage was swept from -5V to 5V, with V_{ds}=100mV. **b,** The leakage current of the TiN/HfO_2/p-Si/Al stack capacitor, where the thickness of HfO_2 layer is 2nm.

11. An estimation of the energy consumption per spike

A crude estimation of the energy consumption per spike for IGNWFETs can be deduced according to Joule's law.

$$W = UIt$$

$$\approx 50 \times 10^{-3} \times 0.5 \times 0.3 \times 10^{-9} \times 50 \times 10^{-3}$$

$$= 375fJ$$

Where U, I and t are drain voltage, effective drain current and EPSC duration, respectively. Further reducing the pulse width can achieve lower energy consumption. Limited by accuracy of measurement instruments, we have not used shorter pulse width in our work.

12. Comparison between IGNWFETs and other synaptic transistors

Table 1 shows the comparison between IGNWFETs and other synaptic transistors, IGNWFETs realize a great compromise between device size, integration capability and energy consumption. Especially, dual-synaptic dendritic computations (such as "Add" and "Subtraction") were realized by processing frequency coded spikes with a single device. It should be noted that the calculation method of the energy consumption of IGNWFETs is the same as that of other reported synaptic devices, and the calculation method can be found in S11. From the comparison in Table 1, IGNWFETs have a great potential to be used as a highly dense and energy-efficient synaptic device into the large-scale artificial neural network.

Table1. Comparison between IGNWFETs and other synaptic transistors.

	Technology	Device size	Material: Dielectric Channel	Waferscale Integration capability	Minimum Power	Coupling computing	"ADD" power	"AND" power
Ref [1]	2D FET	1μm-L 3μm-W	PEO ($LiClO_4$) /WSe_2	No	~30fJ per spike	No	/	/
Ref [2]	Thin film FET	16μm-L 100μm-W	SiO_2/IZO	Yes	1pJ per spike	Yes	8.7pJ per operation (5Hz+20Hz)	/
Ref [3]	Plane FET	80μm-L 1mm-W	PSG /IZO	No	12.5nJ per spike	No	/	17.5nJ per group
Ref [4]	2D FET	6μm-L 3μm-W	PVA/MoS_2	No	23.6pJ per spike	No	/	900pJ per group
Ref [5]	2D FET	80μm-L 1mm-W	GO/Graphene	No	90pJ per spike	Yes	/	1.1nJ Per group
Ref [6]	Nanowire FET	300nm-L 70nm-W	Ion gel/ P_3HT:PEO	No	1.23fJ Per spike	No	/	/
Ref [7]	Polymer redox FET	10^3um^2	PEDOT:PSS/Nafion	No	<10pJ per spike	NO	/	/
This work	Nanowire FET	2μm-L 40nm-W	PEO ($LiClO_4$) HfO_2/Si	Yes	≤300fJ per spike	Yes	2.9pJ per operation (5Hz+25Hz)	5.85pJ per group

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