Electronic Supplementary Material (ESI) for Nanoscale.
This journal is © The Royal Society of Chemistry 2020

Supporting Information for

Ultrathin catalyst-free InAs nanowires on silicon with distinct 1D sub-band transport properties

F. del Giudice[1], J. Becker[1], C. de Rose[1], M. Döblinger[2], D. Ruhstorfer[1], L. Suomenniemi[1], J. Treu[1], H. Riedl[1], J. J. Finley[1], and G. Koblmüller[1]

[1] *Walter Schottky Institute and Physics Department, Technical University of Munich, Garching, Germany*
[2] *Department of Chemistry, Ludwig-Maximilians-University Munich, Munich, Germany*

---

1. Influence of SiO_2/Si(111) patterning parameters on mask dimensions and NW growth

To identify optimum process parameters during the substrate pre-patterning using electron beam lithography (EBL), we investigated the influence of exposure dose of the electron beam on resulting key parameters such as mask opening size, NW yield, and NW diameter. Using conventional PMMA EBL resist we thereby explored a large variation in exposure dose ranging from 2 – 400 fC. Fig. S1(a) shows the impact of exposure dose on the mask opening size d_0 for different pitches ranging from p = 0.25 µm to 2 µm. Clearly, it is obvious that higher exposure dose leads to larger mask opening size. Up to a dose of ~20 fC the corresponding increase in mask opening diameter was rather independent of the pitch. However, for larger doses the influence by the pitch becomes quite strong, leading to significantly larger mask opening diameter when the pitch is smaller. This is most likely due to increased exposure in the limit of a high density of exposure spots at narrow pitch. Overall, this allowed us to tune the mask opening diameter from below 50 nm to about 200 nm, as measured by scanning electron microscopy (SEM).

Given the large size tunability of the mask openings, we further recognize a substantial impact on the yield of as-grown InAs NW arrays. As shown in Fig. S1(b), higher exposure dose, i.e., larger mask opening diameter, significantly improves the yield of NWs. As expected from the inter-dependence between exposure dose and mask opening size, we therefore notice a shift of the optimum NW yield with exposure dose for the different pitches. For example, for p = 0.32 µm it requires at least an exposure dose of > 75 fC to achieve a maximum yield of >80%. The equivalent dose for such high yield in arrays with p = 1 µm is much larger, i.e., 400 fC. According to Fig. S1(a) these doses for the two exemplary cases correspond to a mask opening diameter of ~ 120-140 nm. In contrast, with decreasing mask opening size the NW yield drops continuously. Specifically, the NW yield drops to below 20% for mask opening diameters below ~50 nm. Finally, the mask opening diameter also impacts the resulting NW diameter as shown in Fig. S1(c) for an array of p = 1 µm grown for 10 min. We clearly observe that the NW diameter increases continuously for larger opening diameters.

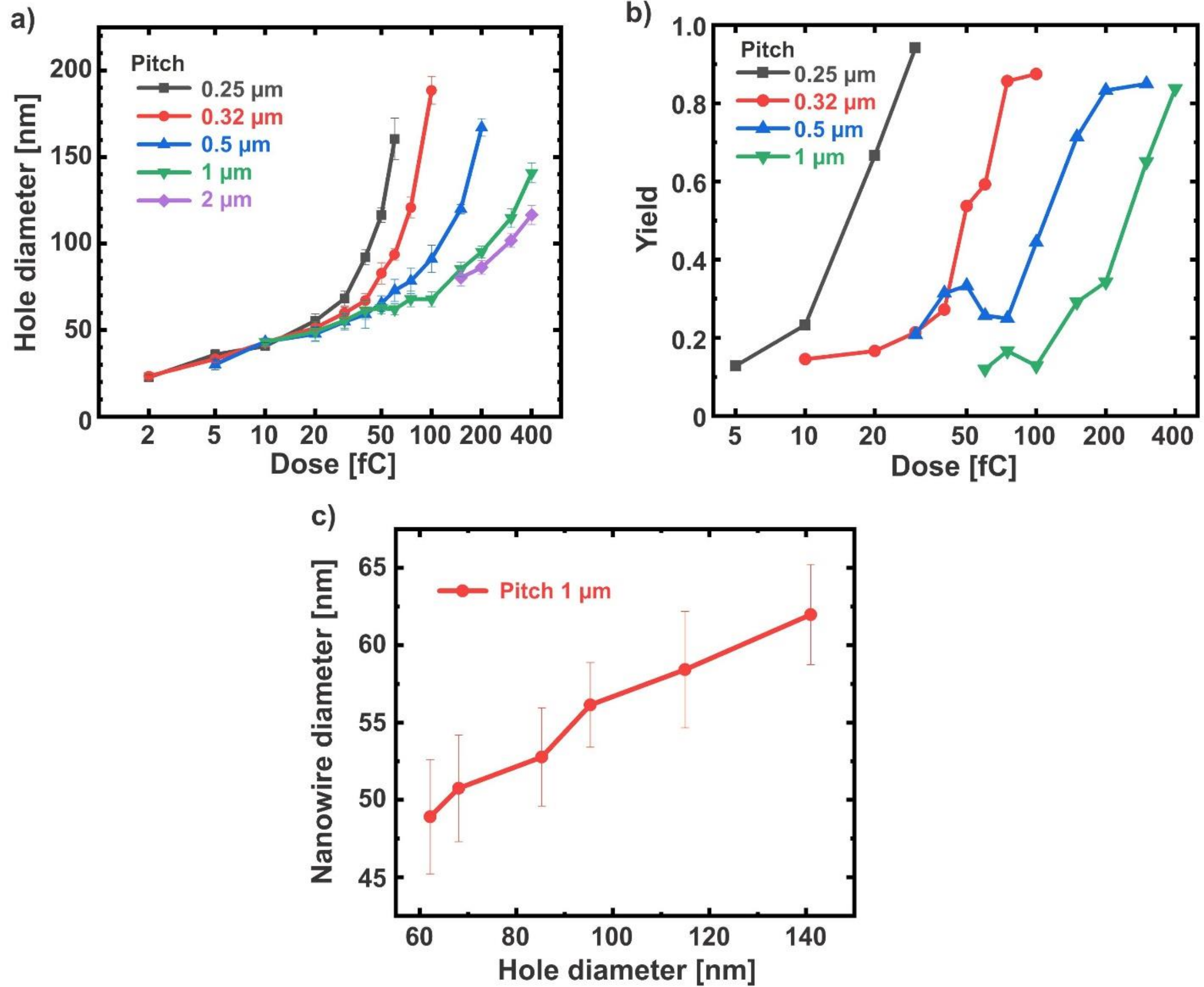

Figure S1: Dependence of EBL exposure dose on the mask opening diameter (a) and the resulting NW yield (b) for different pitches. (c) Exemplary evolution of NW diameter as a function of mask opening diameter as obtained for a 10-min long growth of InAs NWs with an array pitch of 1 µm.

2. Microstructure of bottom-up vapor-solid grown InAs nanowires

To illustrate the typical microstructure of very thin, bottom-up vapor-solid InAs NW grown by MBE without the use of a catalyst, high-resolution transmission electron microscopy (HR-TEM) analysis was performed on NWs that stem from a similar growth study. Fig. S2 shows representative TEM micrographs and corresponding selected area diffraction (SAD) pattern of ultrathin InAs NW, grown for $t_G = 3$ min on an array with pitch $p = 0.25$ µm and under high V/III ratio (~100) / high-temperature (500 ºC). NWs from this growth are approximately ~280-320 nm long and ~21-25 nm wide, as seen in the overview micrograph of Fig. S2(a). The SAD pattern, shown in Fig. S2(b), exhibits wurtzite (WZ)-sensitive reflections (i.e., $0\bar{1}12$ and $01\bar{1}2$) indicating a predominant WZ stacking along the NW, while additional streaks between individual reflections

evidence a very high stacking disorder and random layer stacking along the [0001] growth orientation. This type of microstructure is commonly observed in catalyst-free MBE-grown InAs NWs under high V/III ratio and high temperature (> 480 ºC), and is in line with all our previous reports [2-5] irrespective of the size (diameter) of the NWs. The HR-TEM images depicted in Fig. S2(c) represent three different regions along the recorded NW (tip-1, middle-2, bottom-3). These images directly confirm the dominant WZ stacking with WZ segment lengths of up to ~10 nm, and the presence of very large densities of stacking defects along the entire NW.

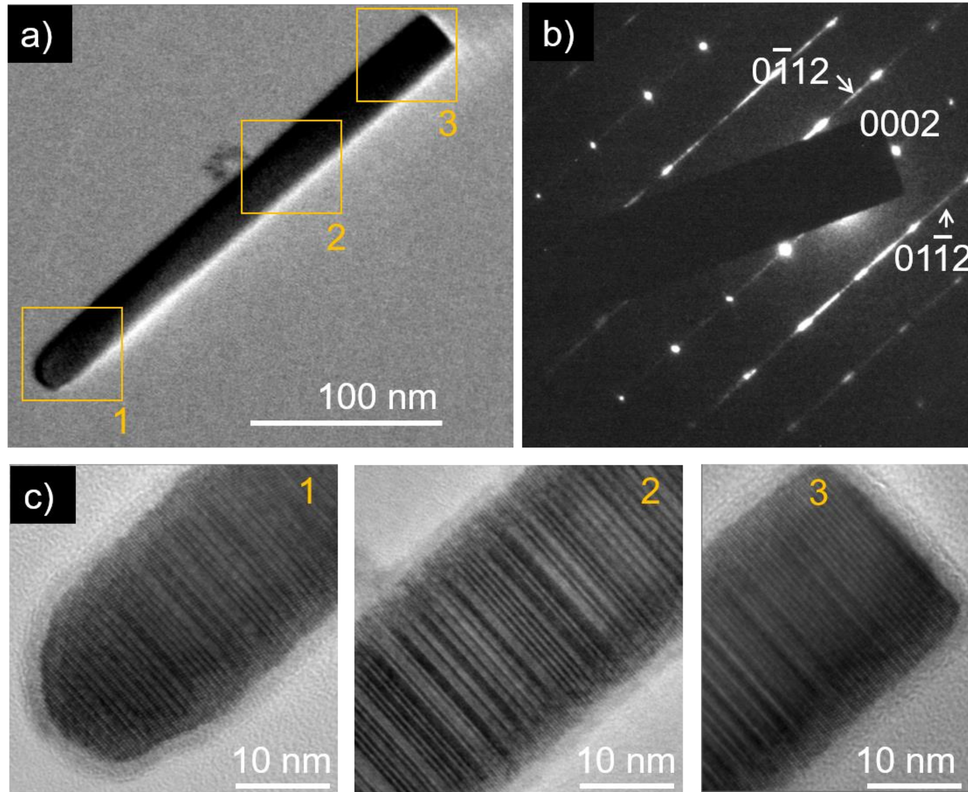

Figure S2: (a) Overview TEM micrograph and (b) corresponding SAD pattern of an ultrathin InAs NW grown under bottom-up catalyst-free growth process, illustrating the WZ-dominated crystal phase and many stacking defects along the [0001] NW growth direction. (c) HR-TEM images taken at different regions along the NW further confirm the characteristic stacking of these NWs.

3. Role of Si(111) surface pre-treatment on NW growth

In order to achieve consistently high yield and high-uniformity in InAs NW arrays we introduced a specific in-situ pretreatment of the patterned SiO_2/Si (111) substrate prior to growth. Following a procedure previously established for catalyst-free GaAs NWs grown on Si (111) by selective area epitaxy [1], we apply the following sequences outlined in the process flow diagram of Fig.

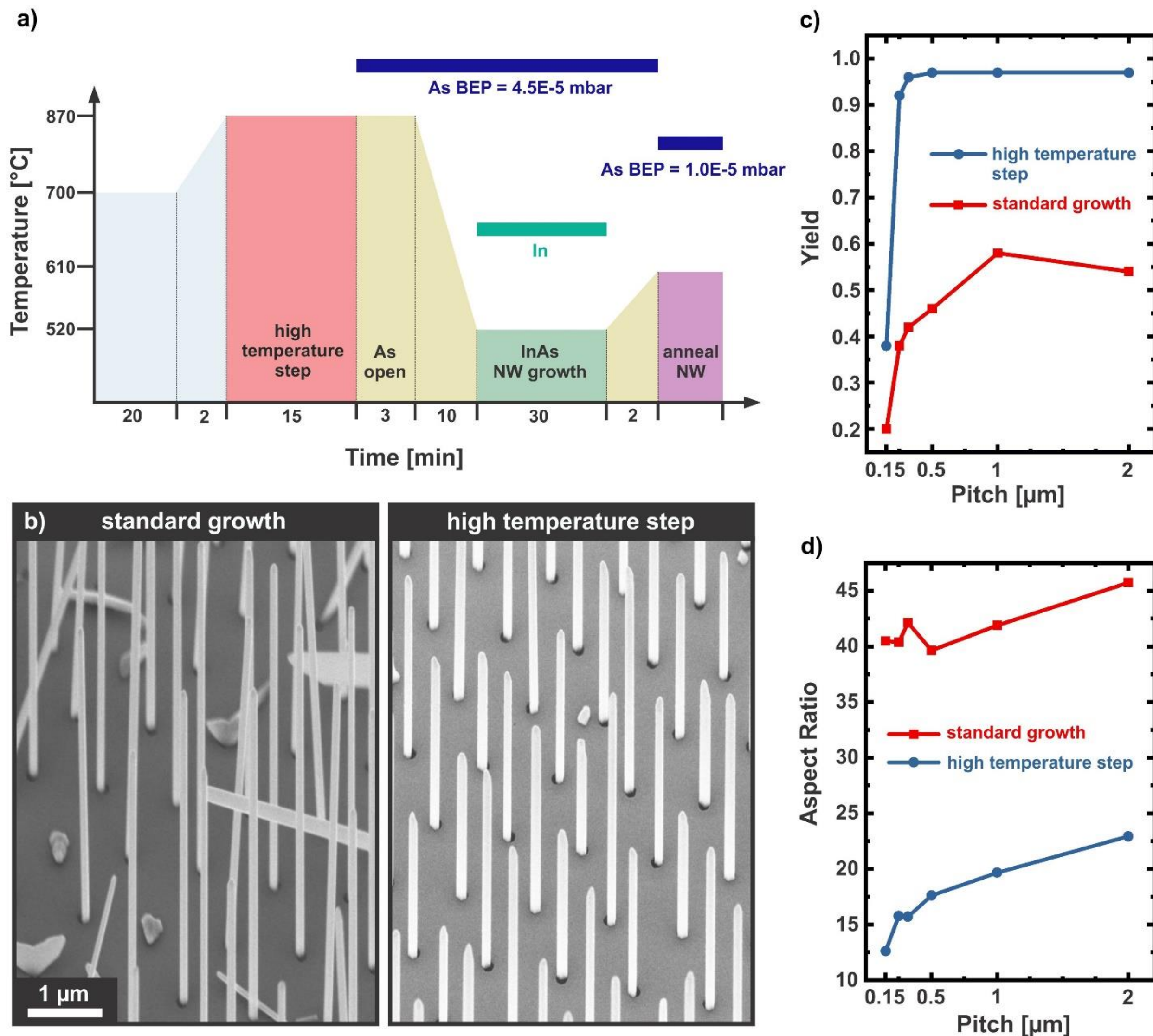

Figure S3: (a) Process flow diagram for the in situ pretreatment and successive growth steps of high-yield InAs NWs on SiO_2-masked As-terminated Si (111). (b) Comparison of SEM morphologies of InAs NW arrays obtained without (left) and with high-temperature pretreatment (right). The pitch and mask opening diameter for these growths are 1 µm and 140 nm, respectively. NW yield (c) and aspect ratio (d) as a function of pitch for the two growth cases.

S3(a): In a first step, the Si substrate was heated to 700°C for 20 min to remove hydrogen (H) atoms from the H-terminated Si (111) surface inside the SiO_2 mask openings, which was formed by the HF-dip prior to loading the samples into the MBE. Once the H atoms are removed, the Si (111) surface is expected to modify its surface phase to a (7×7) reconstructed surface. Further heating to 870°C transforms the surface to a (1×1) reconstructed surface phase. To enable high probability of As-polar [111]B-oriented NWs, we supplied an As flux of 4.5×10^{-5} mbar (equivalent

to the flux used during growth) to stabilize an As-terminated (1×1)-reconstructed surface. After this, the temperature was ramped to the growth temperature at 520°C and by opening the In shutter InAs NWs were grown for 30 min, forming the base for post-growth annealing experiments as described in the main text. The annealing procedure is also illustrated in the process flow diagram (i.e., temperature ramp to 610 °C and supply of As–flux 1.05×10^{-5} mbar).

Fig. S3(b) compares SEM morphologies of InAs NW arrays right after 30 min of growth on patterned fields with pitch p = 1 µm for the cases with pretreatment (right) and without (left). Clearly, the NW array grown on the pretreated substrate exhibits much higher homogeneity and a yield in excess of 95%. This is further confirmed in the plot of Fig. S3(c), which illustrates the NW yield for different pitches. Consistently, NW yield larger than 90% was observed almost for all investigated pitches, when pretreatment was performed. In contrast, for samples grown without pretreatment the yield was lower (typically less than 80%) along with fluctuations amongst different growth runs. The exemplary sample presented in Fig. S3(c) has a maximum yield of ~60% for $p > 1\mu m$, whereas the yield decreases towards lower pitch. Here, we investigated even pitch as low as p=0.15 µm, where the yield drops markedly for both types of samples, and is systematically observed for all growths. Since the yield at such small pitch was too low to unambiguously study the effects of interwire-spacing dependent thermal decomposition dynamics, we limited our investigations in the main text to pitches in excess of 0.25 µm. Furthermore, the pretreatment had an interesting effect on the aspect ratio of the NWs (Fig. S3(d)). While the NW diameters changed only marginally, the NW length was highly affected, leading to much shorter NWs on pretreated Si substrates. Aspect ratios are, hence, about a factor of 2-3 smaller as compared to NW arrays grown on untreated substrates and depend on pitch, in analogy with the observations in the main text.

4. Reverse-reaction growth without As overpressure

To illustrate the effect of the UHV environment on the reverse-reaction growth during in situ annealing, we performed a comparative experiment without the use of As overpressure. In this case, after growth the temperature was ramped to 590°C under the same As-flux used during growth (4.5×10^{-5} mbar). Once the set temperature was reached (after 2 min) the As-flux was turned off and different annealing times were applied to explore the reverse-reaction growth dynamics. Fig. S4 on the left shows the typical reference obtained without undergoing the temperature ramp. As expected, the NWs have an original length of several µm with a non-tapered morphology. For 3 min of in situ annealing at 590°C (i.e., without any As-flux) pencil-shaped NW tips start to evolve, similar to the observations made under the presence of As-overpressure in the main text. After another 3 min of annealing, only few NWs remained that became progressively thinner. However, the majority of NWs were decomposed, leaving macroscopic droplet-shaped clusters on the underlying substrate. Additional annealing by another 3 min (total of 9 min) leads to the

complete decomposition of all NWs. Only metallic In droplets are visible on the substrate, indicating the non-congruent evaporation conditions under the absence of As overpressure.

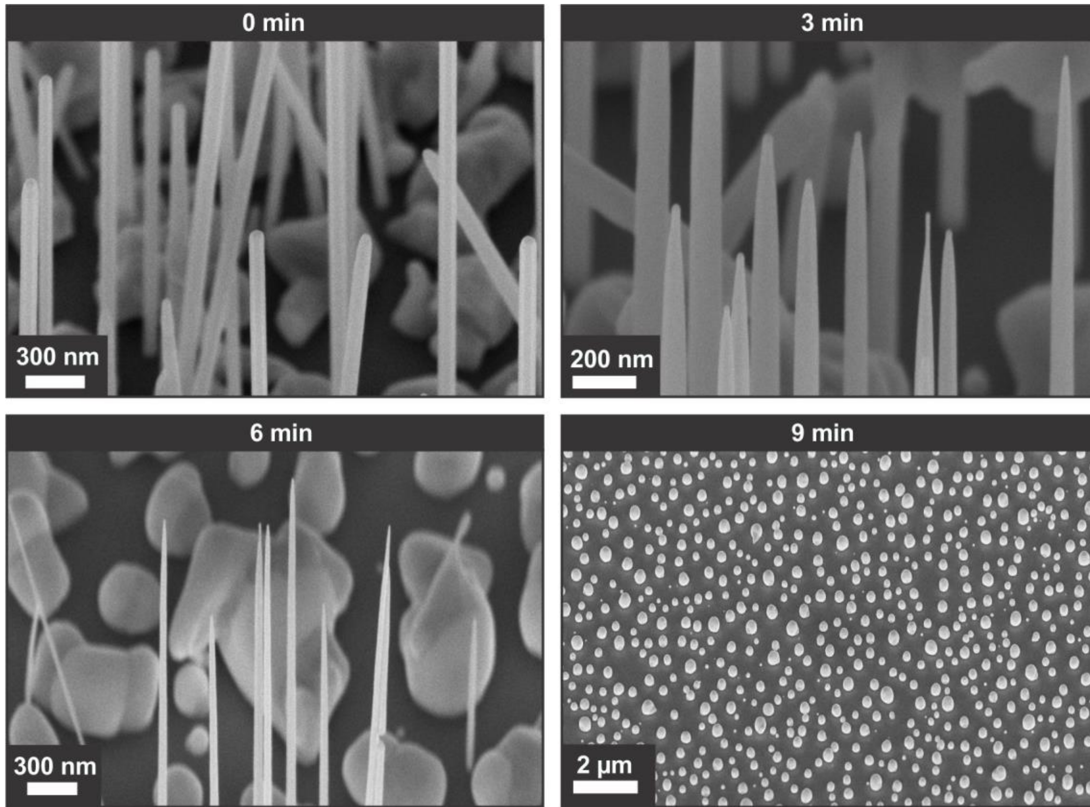

Figure S4: SEM morphologies of InAs NWs upon in-situ annealing at 590°C under the absence of As-overpressure. (Upper left) Reference sample prior to annealing. The other images depict morphologies obtained for annealing times of 3 min, 6 min, and 9 min, respectively. After 9 min all NWs are evaporated leaving only metallic In droplets behind.

5. Energy eigenvalues and radial carrier distribution in dependence of gate voltage

Using the Hartree solver nextnano++ [6] we self-consistently calculated the spatial distribution of the wavefunction amplitudes (Ψ^2_n) for a significant number of eigenstates in dependence of the applied backgate voltage V_{BG}. Fig. S5(a) shows the resulting distribution of the squared wavefunction amplitudes in the cross-section of the hexagonal InAs NW (width of 25 nm), where the bottom facet of the NW is anchored to the 215-nm thick SiO_2 gate dielectric (not shown in the viewgraphs). In total, these are illustrated for the first 10 eigenstates ($\langle\Psi_n|E|\Psi_n\rangle$) at four different

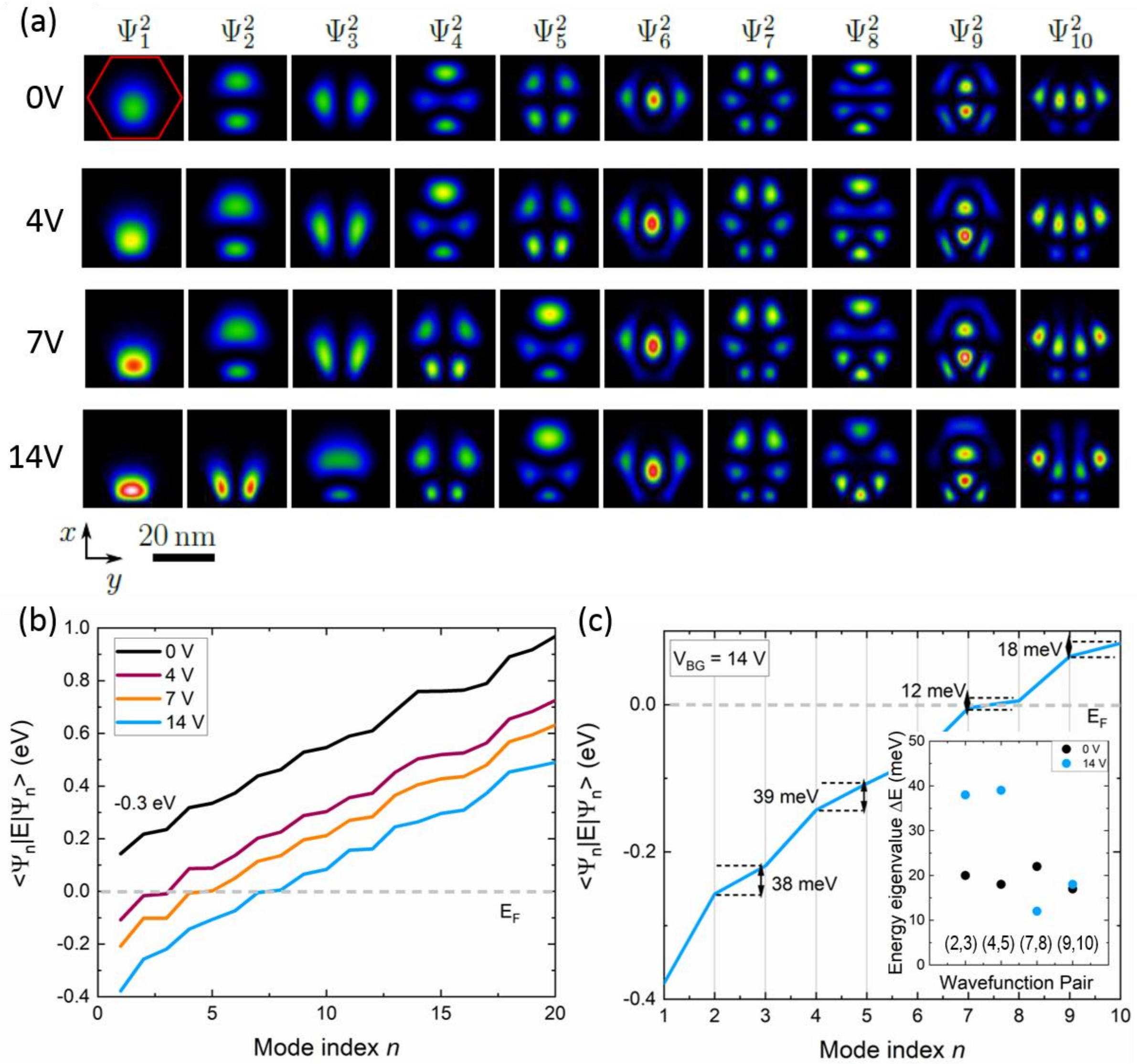

Figure S5: (a) Squared electron wavefunction amplitudes $\Psi_n^2(\vec{r}) = \Psi_n^*(\vec{r}) \cdot \Psi_n(\vec{r})$ of the first 10 eigenfunctions in a 25-nm wide InAs NW for applied backgate voltages of 0V, 4V, 7V, and 14V, respectively. The red hexagon in the top left image delineates the cross-section of the NW. The wavefunction amplitudes are ordered according to their energy eigenvalue $\langle\Psi_n|E|\Psi_n\rangle$. (b) Energy eigenvalues versus mode index n for the different backgate voltages V_{BG} = 0V, 4V, 7V and 14 V for the first 20 eigenstates in the same device (the trace for V_{BG} = 0V was shifted by -0.3eV for clarity). The Fermi level E_F is indicated by the dashed line. (c) Detailed view of the energy eigenvalue spectrum for the first 10 eigenstates at V_{BG} = 14V, depicting the different energy separation for the two-fold degenerate states related to the wavefunction pair amplitudes (Ψ_2,Ψ_3), (Ψ_4,Ψ_5), (Ψ_7,Ψ_8), (Ψ_9,Ψ_{10}). The inset compares the corresponding energy separation (in meV) for these two-fold degenerate states for gate voltages of 0V (black data) and 14 V (blue data).

backgate voltages V_{BG} = 0V, 4V, 7V, and 14 V. When looking at the ground state Ψ_1 we can clearly see that the center of gravity of the wavefunction amplitude Ψ_0^2 is pulled closer to the gate dielectric upon increasing V_{BG}. For the remaining states we find that pair amplitudes (Ψ_2,Ψ_3), (Ψ_4,Ψ_5), (Ψ_7,Ψ_8), (Ψ_9,Ψ_{10}) exhibit energy eigenvalues that are relatively close to each other at V_{BG} = 0V, with values of ~20 ± 2 meV for all pairs (mode index 2-3, 4-5, 7-8, 9-10, see Fig. S5(b) and the energy eigenvalue data in inset of Fig. S5(c)). For increased gate voltage these energy values start to deviate, e.g. at V_{BG} = 14V the corresponding values change to ~38 meV for pairs 2-3 and 4-5, while for pairs 7-8 and 9-10 the values are 12 meV and 18 meV (see Figs. S5(c)). As shown in Fig. S5(a), for increased backgate voltage one wavefunction of the pair amplitude is pulled closer to the gate dielectric and the other one further away, increasing the asymmetric carrier distribution. Thus, the degeneracy of the lowest two-fold degenerate states (e.g. 2-3,4-5) at V_{BG} = 14V are lifted almost by up to 20 meV with respect to the case at V_{BG} = 0. Also we notice that due to the shifting of the wavefunction towards the gate dielectric with increasing V_{BG}, some of the almost degenerate states are swapped. For instance, this is seen for state $\Psi_2(7V) \leftrightarrow \Psi_3(14V)$ and $\Psi_4(4V) \leftrightarrow \Psi_5(7V)$.

[1] D. Ruhstorfer, et al., Appl. Phys. Lett. **116**, 052101 (2020).

[2] G. Koblmüller, et al., Appl. Phys. Lett. 101, 053103 (2012).

[3] S. Morkötter, et al., Phys. Rev. B **87**, 205303 (2013).

[4] J. Becker, et al., ACS Nano **12**, 1603 (2018).

[5] J. Becker, et al., Phys. Rev. B **97**, 115306 (2018).

[6] S. Birner, et al., IEEE Trans. Electron Dev. **54**, 2137 (2007).