Electronic Supplementary Material (ESI) for Nanoscale.

Supplementary Information

Tailoring the transfer characteristics and hysteresis in MoS_2 transistors using substrate engineering

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S1. Transfer characteristics and hysteresis in Type-I devices

In this section we report data on an additional type I device (named T1B), which is fabricated devoid of surface plasma treatment. We use this device as a reference device to highlight the stronger hysteresis features observed in Type-II devices. A study of sweep rate shown in Fig. S1 shows negligible hysteresis for various step sizes. In comparison to Fig. 3a in the main text, this suggests that the hysteresis effects in Type-I devices are minimal and the observed features in Type-II devices are due to the substrate engineering via plasma treatment. Fig. S2 summarizes the gate stressing analysis in device T1B performed under similar experimental conditions, as Fig. 4 in the main text. Notably, while the threshold voltages where the device current turns ON shows a minor dependence on the voltage range accessed after gate bias stressing, the hysteresis curves shown in the insets show very minimal hysteresis in linear scale. This indicates that the mechanisms responsible for hysteresis in Type-I and Type-II devices are distinct. The minimal hysteresis observed in Type-I devices may be attributed to negligible amounts of adsorbed species, intrinsic oxide traps or intrinsic defects in the MoS_2 layer, as observed in previous studies.

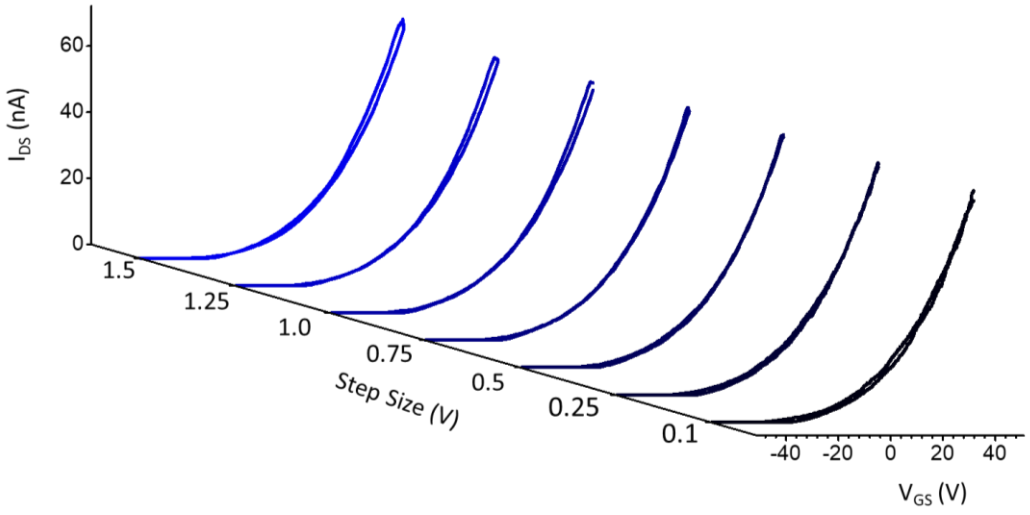

Fig S1. Sweep rate analysis on Type I device T1B acquired for step sizes (ΔV_{GS}) ranging varying from 0.1 V to 1.5 V, with Δt =800 ms.

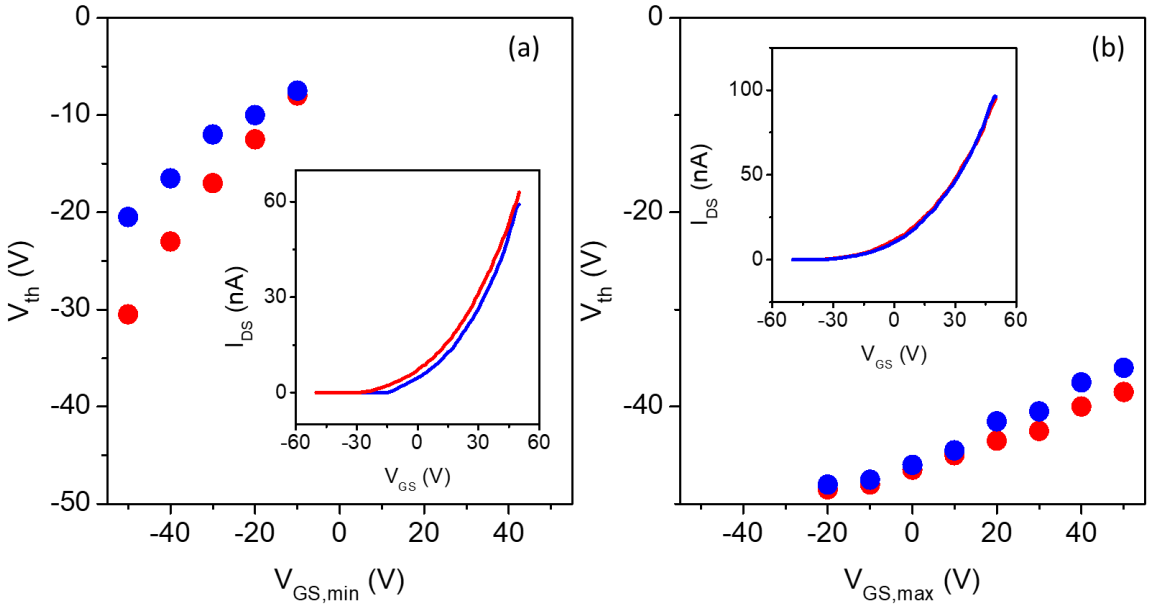

Fig S2. Gate bias stressing studies on Type I device T1B. Gate bias was kept at +50 V and -50 V for 24 hours before acquiring the two graphs (a) and (b) respectively. Threshold voltages for down sweep (blue) and up sweep (red) (a) for different minimum V_{GS} while keeping maximum V_{GS} as 50 V, and (b) for different maximum V_{GS} while keeping minimum V_{GS} as -50 V. Insets show the transfer characteristics for the full range ($\pm$ 50 V) sweeps, with red and blue denoting the up and down sweeps respectively.

Transfer characteristics and hysteresis in Type-II devices with modified substrate processing

In order to demonstrate substrate engineering using plasma treatment, we also fabricated another Type II device T2B with 20 seconds of plasma treatment. Note that the device T2A reported in the main text was fabricated using plasma treatment for 10 seconds. Fig. S3 shows the sweep rate analysis for device T2B, which follows the same trend as T2A discussed in the main text. It is also observed that by increasing the plasma treatment duration from 10s (Fig. 3) to 20s (Fig. S4), the width of the hysteresis in the transfer characteristics increases. To compare the hysteresis in different devices, the hysteresis width ΔV was calculated as the difference between the threshold voltages (V_{th}) for down sweep and up sweeps. Fig. S4 compares the width of hysteresis in the two devices in terms of ΔV for various step sizes, demonstrating that an increase in the duration of plasma treatment results in increase in the density of trap states and hence the hysteresis width.

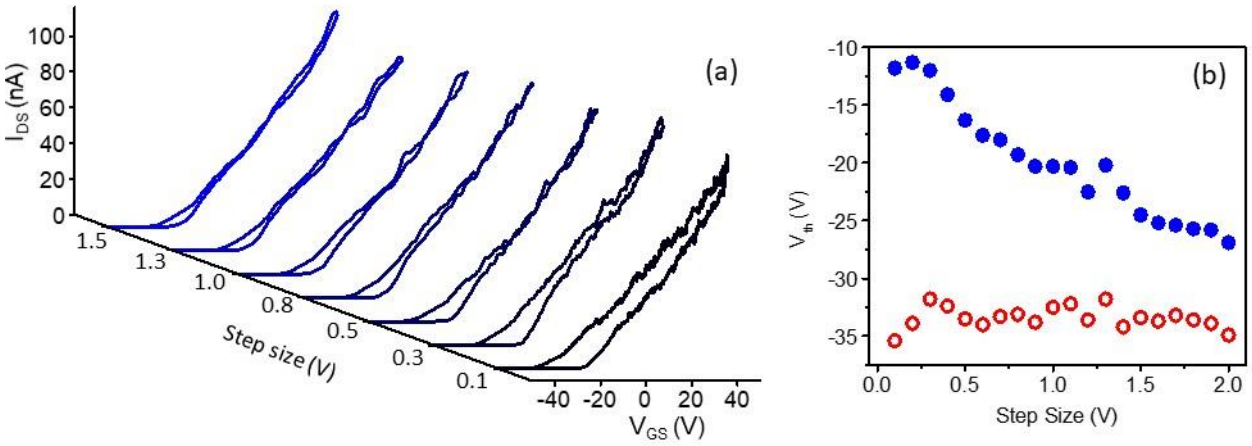

Fig S3. Sweep rate analysis on Type II device T2B, which was subjected to plasma treatment for 20s. (a) Transfer characteristics for various step sizes ΔV_{GS}. (b) Threshold voltages for the down (blue) and up (red) sweeps, as a function of step size (or sweep rate).

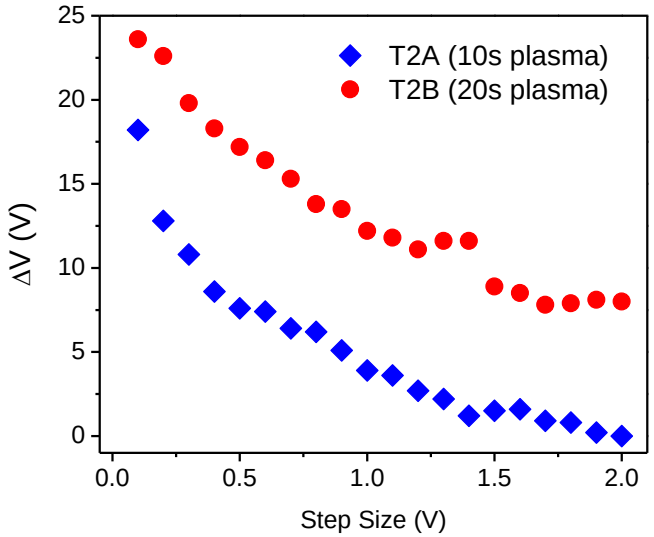

Fig S4. Comparison of hysteresis width in type II devices T2A and T2B, with plasma treatment for 10s and 20s respectively. Clearly, the hysteresis width is enhanced in the case for T2B, due to higher density of trap states.