Supplementary Information

Flexible Organic Field-Effect Transistor Arrays for Wearable Neuromorphic Device Applications

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Fig. S1 shows the schematic fabrication process of the organic field-effect transistor (FET) device arrays on flexible substrate. In general, a flexible indium-tin-oxide (ITO) coated poly(ethylene terephthalate) (PET) substrate was cleaned with acetone, isopropyl alcohol (IPA) and deionized water. The poly(methyl methacrylate) (PMMA) solution was filtered through a microfilter with the 0.22 μm pore size before coating. The filtered solution was spin-coated on the substrate. Then, the sample was heated on a hot plate at 120 ℃ for 30 min. High-k dielectric ZrO_2 trapping layer of 24 nm is deposited by atomic layer deposition (ALD) at 130 ℃. 5 nm tunneling layer Al_2O_3 is deposited by the same method. 2,7-dioctyl[1]benzothieno[3,2-b][1]benzothiophene (C8-BTBT) was deposited onto the substrate by thermal evaporation. Au (50 nm) was deposited onto the C8-BTBT using a shadow mask by sputtering.

Fig. S2a shows the schematic molecular structure of the C8-BTBT and PMMA used in the experiment. Fig. S2b demonstrates the X-ray photoelectron spectroscopy (XPS) spectra obtained from the C8-BTBT surface. The main peaks at 163 eV and 285 eV correspond to the excitation of S2p, and C1s, respectively.

Fig. S3a and S3b show the schematic band diagrams during programing and erasing operations, respectively. In the programing operations, when V_G reaches a threshold negative voltage, the holes in C8-BTBT can tunnel through the 5 nm thick Al_2O_3 tunneling dielectric to the ZrO_2 trapping layer and stored in the ZrO_2 charge-trapping layer. Meanwhile, electrons in the ZrO_2 charge-trapping layer will tunnel to the C8-BTBT channel through the 5 nm Al_2O_3 tunnel layer. The increased positive charges in ZrO_2 will screen electric field to reach the channel, which leads to a ΔV_{TH} in negative direction[1]. In the erasing operations, the pre-stored holes will tunnel back to the C8-BTBT channel and the electrons in C8-BTBT will tunnel into the charge-trapping layer, and reversely leading to a positive threshold voltage shift (ΔV_{TH}).

Filter behaviors can be used to mimic short-term synaptic plasticity (STP). When continuous stimulation is applied to the transistor, the subsequent stimulation will have a gain effect due to the previous stimulation[2]. In the transistor, it appears as an increase in EPSC peak value. Along with the stimulus frequency increases from 2 Hz to 50 Hz, the time interval between adjacent stimuli gradually shortens, and the EPSC gain (A_5/A_1) increases from 1.02 to 10.38. This process is similar to the memory process of organisms. More frequent learning will lead to deeper memory, which shows the synaptic facilitation behavior. The results shown in Fig. S5 clearly suggest that the biological synaptic potentiation and depression have been successfully emulated by the increase and decrease of the channel conductance.

During the bending process, the force of the device is shown in Fig. S6 in which M is the bending moment and y is the distance between the cross section and the neutral layer. d is the thickness of the ITO/PET substrate, and R is the bending radius. Since the linear strain ε is proportional to the distance y from the neutral layer, the maximum strain of the device occurs at the surface, where y=d/2. The maximum strain can be calculated with the following equation:

$$\varepsilon_{max} = 100\% \times \frac{y}{\rho} = 100\% \times \frac{\frac{d}{2}}{R + \frac{d}{2}}$$

Since the bending radius R=7 mm and the thickness of the ITO/PET substrate is d=0.175 mm, the maximum strain of the device can be calculated to be ε_{max}=1.2%.

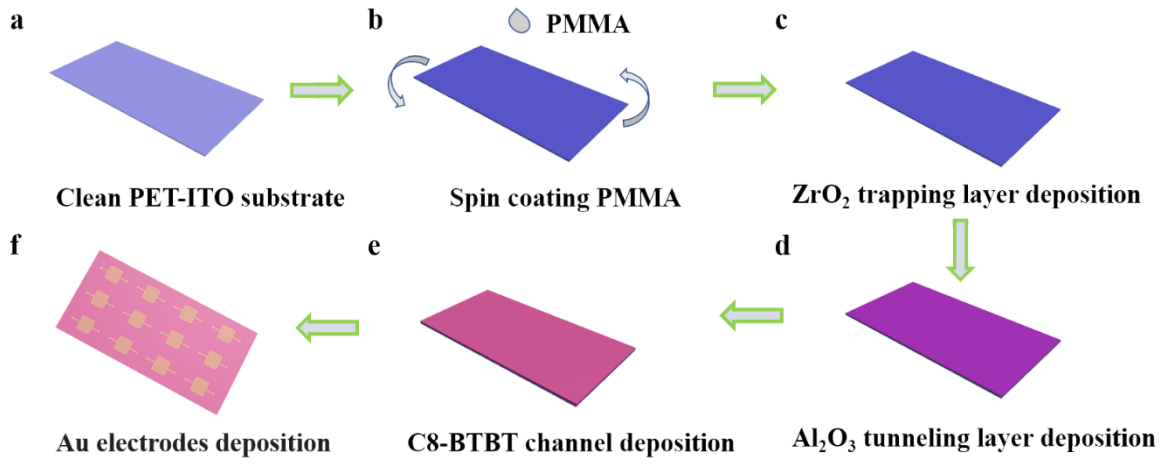

Fig. S1 The fabrication process of the transistor.

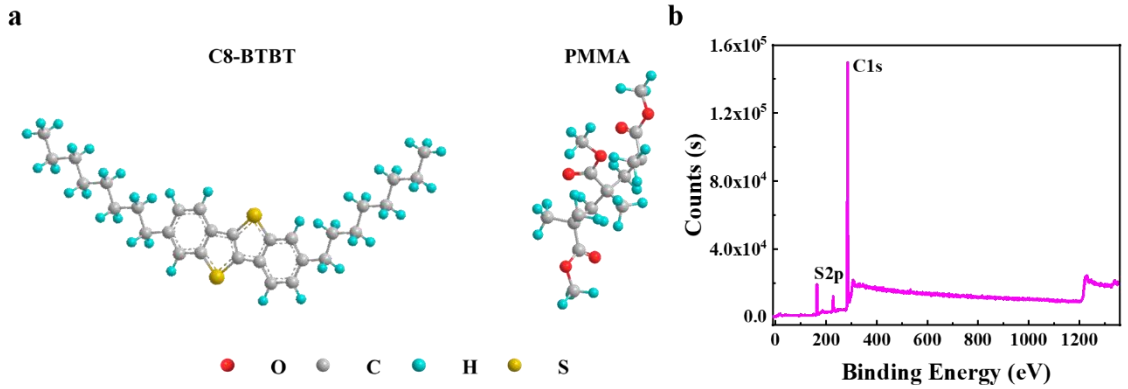

Fig. S2 Chemical structures and XPS characterizations of C8-BTBT. (a) The molecular structures of the C8-BTBT and PMMA used in the experiment. (b) XPS characterizations of C8-BTBT surface.

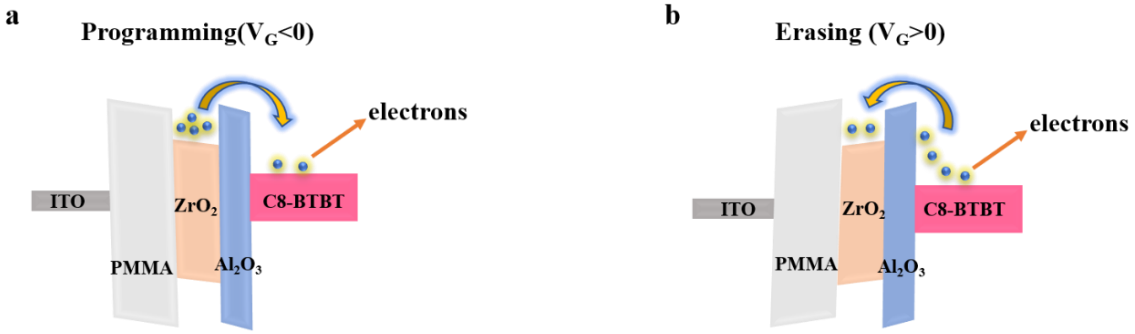

Fig. S3 Schematic band diagram of the C8-BTBT memory under (a) program operation (V_G < 0), and (b) erase operation (V_G > 0).

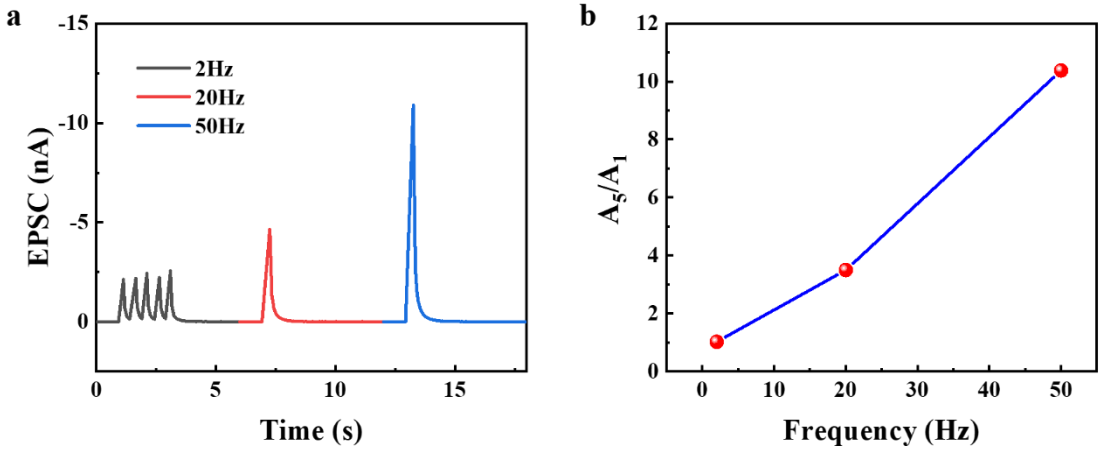

Fig. S4 Filter behaviors of the device. (a) EPSCs recorded in response to the stimulus chain with different frequencies. The stimulus chain at each frequency consists of 5 stimulus spikes

(-20 V, 10 ms). V_{DS} was kept at 10 mV. (b) EPSCs amplitude gain (A_5/A_1) plotted as a function of presynaptic spike frequency.

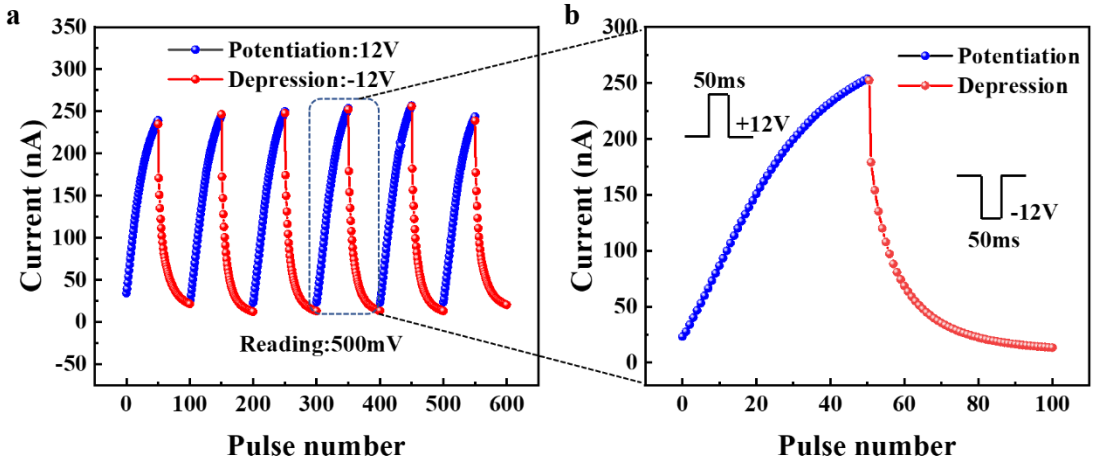

Fig. S5 (a) Repetitive channel conductance modulation by applying repeated positive (12 V for 0.05 s with 2 s interval, V_{DS} = 0.5 V) and negative (-12 V for 0.05 s with 2 s interval, V_{DS} = 0.5 V) gate spikes. (b) Enlarged image of one waveform in (a).

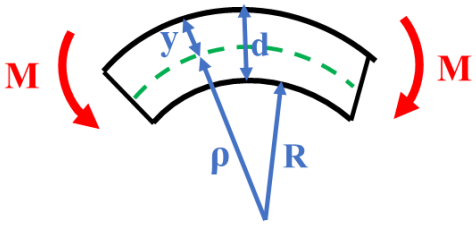

Fig. S6 Schematic of the bending test structure.

References

1 R. Bez, E. Camerlenghi, A. Modelli and A. Visconti, Proc IEEE, 2003, 91, 489-502.

2 E. S. Fortune and G. J. Rose, Trends in Neuroences, 2001, 24, 381-385.