Supporting Information for

A charge sensor integration to tunable double quantum dots on two neighboring InAs nanowires

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In the supporting information we provide additional data of the device we reported in the main article and extra transport measurement results obtained from another device with similar structure used in the main article. We assign the device of main article as CS device#1 and label the device with similar structures we are going to show here as CS device#2.

I. Back-gate transfer characteristics of CS device#1

The I_{SD} is the current through NW1 channel and the I_{sd} is the current through NW2 channel. The threshold voltage of back-gate for NW1 and NW2 are -2.380 and 1.745 V, respectively. The measurement of the main article is carried out at $V_{BG} = 10$ V in order to gain sufficient carrier concentration. The resonance-like fluctuations observed in the figure dominantly arise from abrupt changes in the potential profiles induced by charge traps in the oxides. This is not a problem if we work the device near or below the pinch-off voltages.
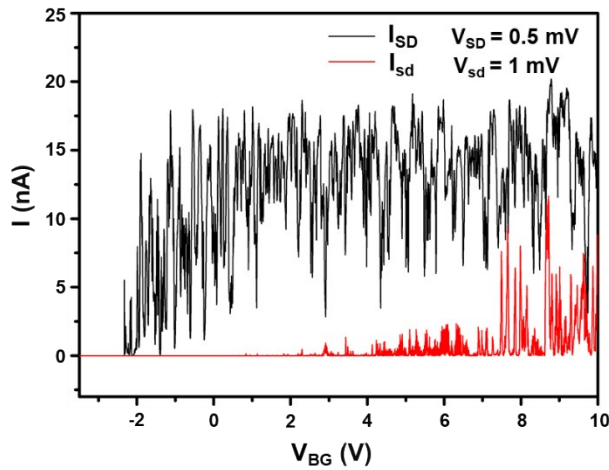

Figure S1. Source-drain current as a function of back-gate voltage (transfer characteristics) of the device investigated in the main article at base temperature $T = 20$

mK, while all finger top-gates are grounded in the measurements.

II. Threshold voltage of back gate and finger top-gates

Unit(V)	NW1					NW2		
$V_{BG\,th}$	-2.380					1.745		
V_{BG}	$V_{G1\,th}$	$V_{G2\,th}$	$V_{G3\,th}$	$V_{G4\,th}$	$V_{G5\,th}$	$V_{g1\,th}$	$V_{g2\,th}$	$V_{g3\,th}$
4.3	-1.475	-1.115	-1.160	N.A.	N.A.	-0.375	-0.210	-0.390
8.0	-1.545	-1.550	-1.635	N.A.	N.A.	-0.465	-0.380	-0.585
10.0	-2.035	-1.820	-1.840	-1.845	-2.815	-0.595	-0.470	-0.655

Table S1. Threshold voltages of back gate and finger top-gates for NW1 and NW2 of CS device#1 at base temperature T = 20 mK; The second row presents the threshold voltage of back gate for NW1 and NW2 separately with all finger top-gate grounded. The rows from the fourth to the sixth present the threshold voltage of each finger top-gate at relative back-gate voltages, showing that the Ω-shaped finger top-gates on each nanowire have a uniformed capacitive coupling capability.

III. Response to charge population of QD1 from sensor dot

The charge readout of QD1 at another confinement condition via CS-QD is demonstrated in CS device#1. To build the QD1, we set V_{BG} at 8 V, outer barriers of QD1 at V_{G1} = -1.845 V and V_{G3} = -1.655 V for gates G1 and G3, respectively. The sensor dot is constructed at V_{g1} = -0.489 V and V_{g3} = -0.557 V, and biased at V_{sd} = 3 mV The working point of CS-QD is initialized at V_{g2} = -219.7 mV for applicable sensitivity. The resonance current I_{sd} through CS-QD shows pronounced modulations in terms of abrupt shifts when an electron is populated into QD1. Moreover, the resonance current

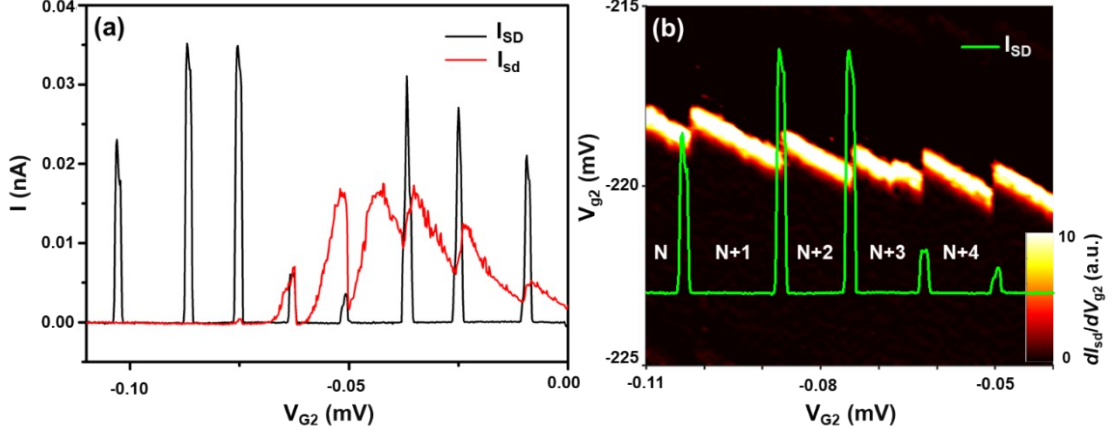is slightly tilted because of the capacitive coupling from gate G2 via the metal bridge-gate.

Figure S2. (a) Coulomb oscillations (I_{SD} in black color) of QD1 with simultaneous response (I_{sd} in red color) of CS-QD, which is set in Coulomb blockade regime. QD1 is a single dot confined in NW1. (b) CS-QD oscillation peak modulation in V_{g2}-V_{G2} space when electron population (indicated by Coulomb oscillation peaks in green color) happens in QD1.

IV. Inter-dot process of electron occupation state transition

We focus on the inter-dot process of electron occupation state transition from (M, $N+1$) to ($M+1$, N), where the total number of confined electrons is fixed in the DQD. The gate-voltage scanning range is limited within 10 mV both for V_{G2} and V_{G4}. Pronounced high conductance lines are emerged in Figure (d), (e), and (f) to connect two triple-points. The detuning $\varepsilon = 0$ is indicated by gray dotted line in Figure (f). These high conductance lines allow us to perform inter-dot process measurements of electron occupation state transition between double quantum dots at different inter-dot coupling strength by applying voltage along the detuning line as described in main article.
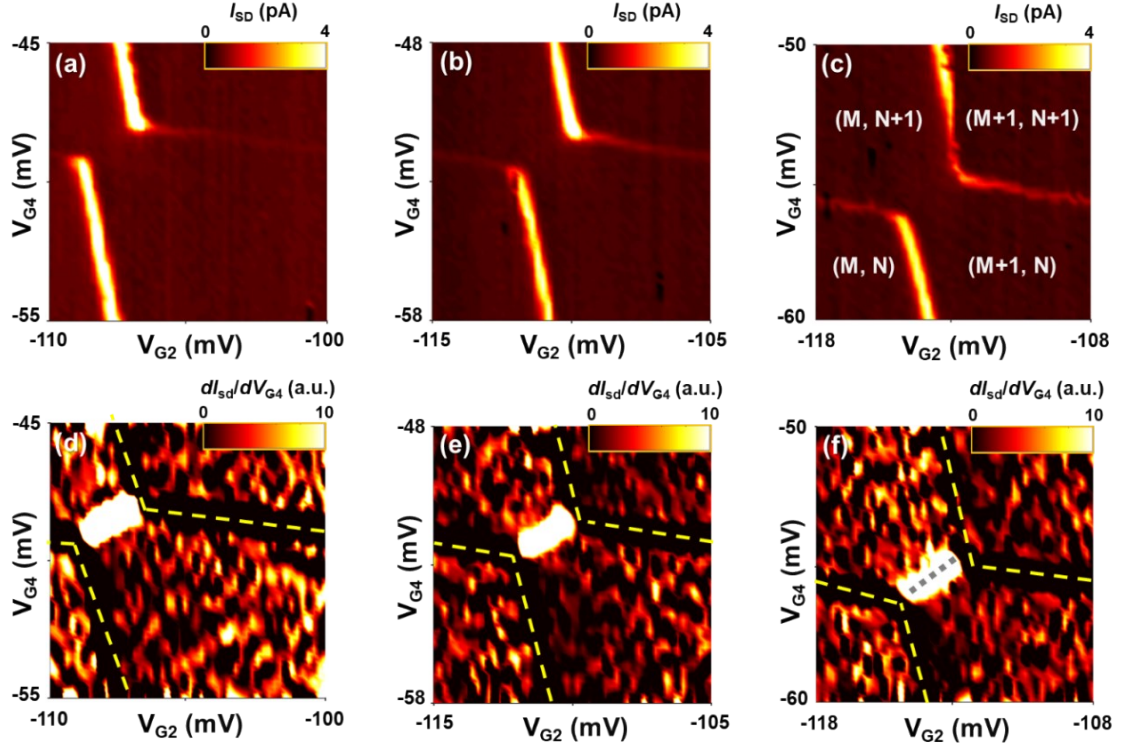
Figure S3. Transition of electron occupation states around (M, N) illustrated by tunneling current I_{DS} spectroscopy and inter-dot processes between double quantum dots demonstrated by transconductance dI_{sd}/dV_{G4} spectroscopy in V_{G2} - V_{G4} space. The main features of DQD transport spectroscopy in Figs. 2(a), 2(b), and 2(c) are well monitored by the charge sensor and accurately reproduced by the sensor conductance spectroscopy point-to-point, as shown in Figure 2(d), 2(e), and 2(f), respectively. Moreover, the inter-dot tunneling process between the double dots can be recognized by the bright conductance lines, which connect two triple-points, in Figure (d), (e), and (f). Here the voltage applied on the gate G3 is V_{G3} = -1.50 V for Figure (a) and (d), V_{G3} = -1.49 V for Figure (b) and (e), and V_{G3} = -1.48 V for Figure (c) and (f). The notation of electron occupation states is indicated in Figure (c).

V. Another device of multiple dots with a charge senor

Here, we demonstrate another charge sensor device we have measured in company with the device reported in the main article. We assign the device of main article as CS device#1 and label the device we are going to show in the following as CS device#2. As shown in Figure S4, the device of CS device#2 possesses similar structures with those of the CS device#1. Single quantum dot of the charge sensor (CS-QD) is defined with top finger gates from g1 to g3 and multiple quantum dots (QDs) are defined with gates labeled from G1 to G8. The CS-QD capacitively couples with one of multiple QDs via a metal bridge-gate (the electrode in red color). The pitch of all the top finger gates is 80 nm.
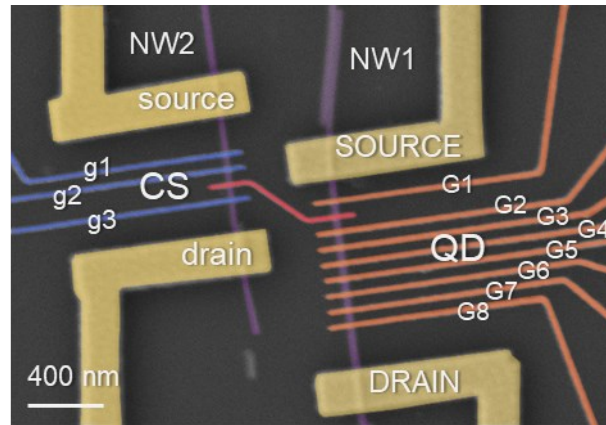

Figure S4. A false color SEM image of charge sensor device (CS device#2).

VI. Charge stability diagrams of CS device#2

The back-gate voltage V_{BG} is set at $V_{BG} = 2$ V to gain sufficient carrier concentration for both InAs nanowires. With outer barrier gates g1 and g3 being set at $V_{g1} = -1.101$ V and $V_{g3} = -0.410$ V, a single QD is formed (CS-QD) as shown in Figure S5(a). The typical even-odd alternating behavior is clearly observed. We choose several Coulomb oscillation peaks ranging from $V_{g2} = -200$ to -160 mV, as shown in Figure S5(b), to

perform magnetic field dependences at linear response regime V_{sd} = 0.1 mV. The oscillation peak responses to the external magnetic field B perpendicular to the substrate are shown in Figure S5(c). An even number of N represents the number of electron occupation in the dot. The g factor of CS-QD can be obtained from Zeeman splitting $\Delta E = |g^*|\mu_B B$ and reaches at 5.9 and 4.2 for the two neighboring orbits, indicating a g factor fluctuation [1].
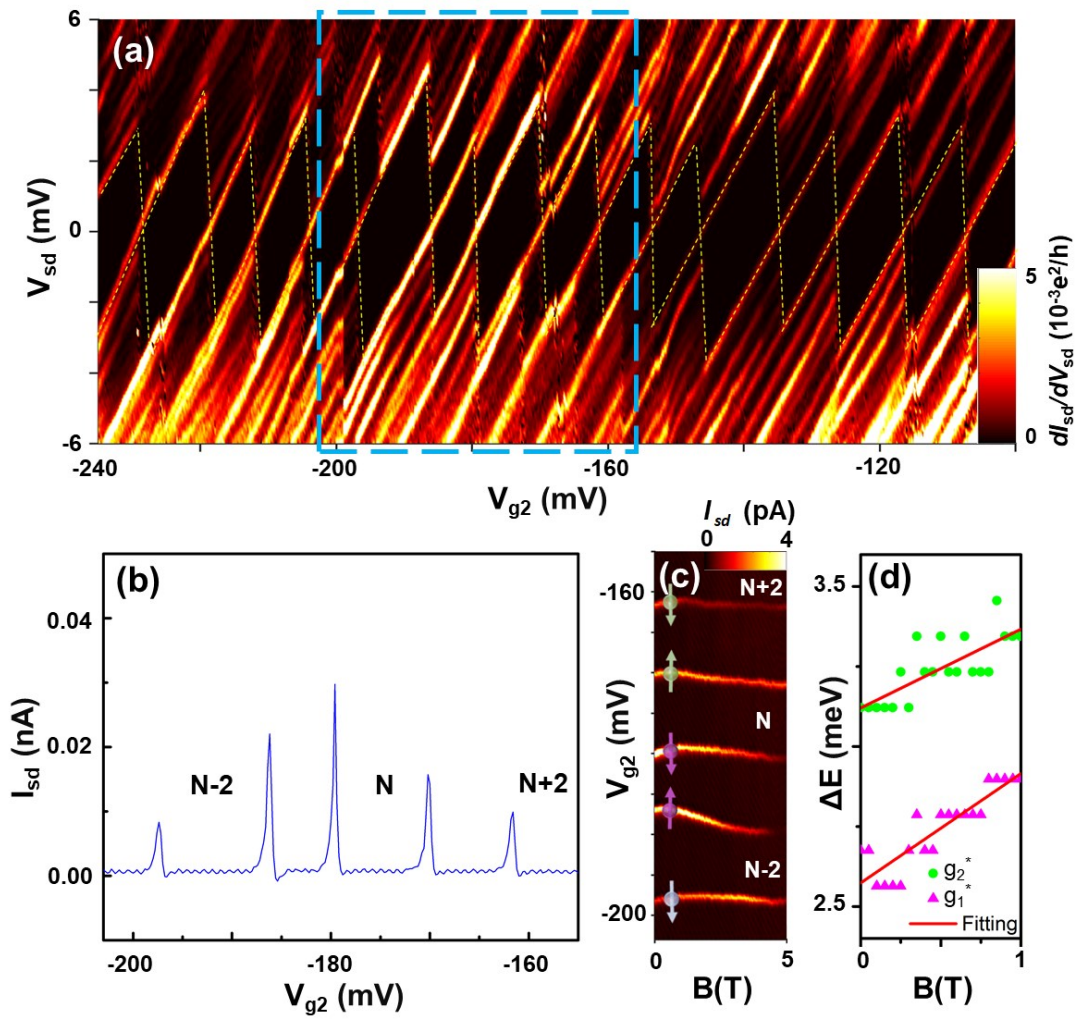

Figure S5. (a) Differential conductance (dI_{sd}/dV_{sd}) as a function of source-drain voltage (V_{sd}) and gate voltage (V_{g2}) shows diamond-shaped Coulomb blockade regions and altering even-odd filling behavior in CS-QD of CS device#2. (b) Two consecutive even-odd pairs of Coulomb oscillation peaks of source-drain current I_{sd} at V_{sd} = 0.1 mV

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picked up from the gate voltage region of blue rectangle shape in figure (a). (c) The evolution of Coulomb oscillation current peaks, depicted in Figure (b), with regard to external magnetic field B. (d) The evolution of orbits, extracted with subtracting charging energy between even-odd pairs. $|g|$ factor can be calculated to be 5.9 and 4.2 for these two consecutive orbits.

VII. Coupling capability of metal bridge-gate

We slightly low outer barriers by setting the gate voltages less negatively to V_{g1} = -0.936 V and V_{g3} = -0.344 V to obtain charge stability diagrams of CS-QD from CS device#2, as shown in Figure S6(a). Figure S6(b) shows the high resolution charge stability diagram with V_{g2} ranging from -250 to -200 mV to highlight the blue dotted rectangular region of Figure S6(a). Serials Coulomb diamonds can be recognized as guided to eyes by yellow dotted lines. Here, the V_{SD} is set at V_{SD} = 0 V with the other gates on NW1 grounded and the electrochemical potential of CS-QD is tuned by gate g2 only. Alternatively, the electrochemical potential of CS-QD can be tuned not only by gate g2 but also by the metal bridge-gate. The voltage change of V_S, which is applied on the SOURCE-lead with DRAIN-lead open, is passed to CS-QD by the capactively coupling via two gate capacitances between NW1 and the bridge gate as well as between the bridge gate and NW2. Again all the gates on NW1 are grounded. Hence, we employ the bridge gate as another plunger gate to tune the electrochemical potential of CS-QD by varying V_S. Figure S6(c) demonstrates identical charge stability diagram of Figure S6(b) as we sweep V_S by setting V_{g2} = -235 mV. The vertical dotted gray lines

in Figure S6(b) and S6(c), therefore, represent identical measurement conditions. The main features of the single QD in Figure S6(b) is well duplicated in Figure S6(c), except several gate voltage jumps happening in Figure S6(c) probably due to two gate capacitors involved in the V_S sweeping that offers extra charge traps. The bridge-gate capacitance can be extracted by $C_g=e/\Delta V_s$ from Figures S6(c) to be 3.4 aF. Here, e is the elementary charge, ΔV_s the Coulomb diamond dimension along gate voltage axis (V_s). The resistance between two nanowires is adopted by an empiric value of ~10 GΩ. Therefore, we obtain a RC time constant of 34 nS, which could be a typical time scale of response and recover times. As a consequence, response and recover times in this work is significantly shorter than the charge sensing operations and potentially support dynamical response with high-bandwidth operation [2].
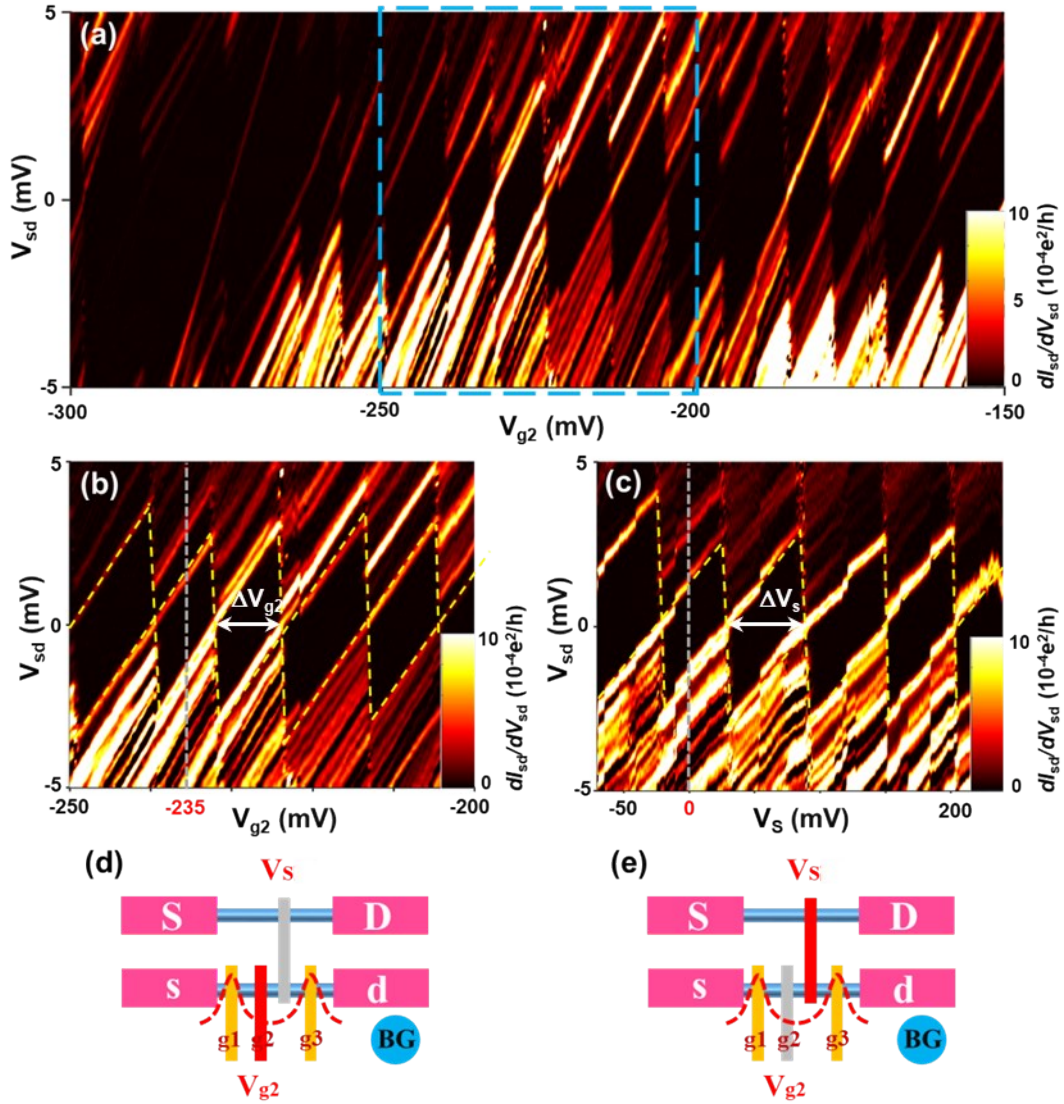
Figure S6. (a) Charge stability diagram of CS-QD measured from CS device#2 as a function of source-drain voltage (V_{sd}) and plunger gate voltage (V_{g2}) is shown in a wide gate-voltage range. (b) High resolution charge stability diagram in V_{sd}-V_{g2} space, where the electrochemical potential of QD is tuned by plunger gate g2 only, highlights the blue dotted rectangular region of Figure (a). In the measurements, the other gates on NW1 are grounded; (c) Charge stability diagram as a function of NW2 source-drain voltage (V_{sd}) and NW1 SOURCE voltage (V_S) with DRAIN-lead open rebuilds the Figure (b) in the blue dotted rectangular region of Figure (a); the electrochemical

potential is altered by V_S while gate g2 is kept at V_{g2} = -235mV. (d) Schematics of measurement setup used to measure Figure (b); (e) Schematics of measurement setup used to measure Figure (c). The red-colored lead means the scanning gate and the gray-colored lead means the idling gate.

Reference

[1] H. A. Nilsson, P. Caroff, C. Thelander, M. Larsson, J. B. Wagner, L.-E. Wernersson, L. Samuelson, H. Q. Xu, *Nano Lett.*, **2009**, 9, 3151-3156.

[2] R. J. Schoelkopf, P. Wahlgren, A. A. Kozhevnikov, P. Delsing, D. E. Prober, *Science*, **1998**, 280, 1238-1242.