Electronic Supplementary Material (ESI) for Materials Chemistry Frontiers.

Supporting Information for:

Polymer Masks Weakening Grain-Boundary Effect: Towards High-Performance Organic Thin-Film Transistors with Mobility Closing to 20 $cm^2 V^{-1} s^{-1}$

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Polymer mask fabrication: First, poly (sodium-4-styrene sulfonate) (PSS), polystyrene (PS) and the photoresist were successively spin coated onto an Indium Tin Oxide (ITO)/glass substrate and then annealed at 150 °C, 80 °C and 95 °C in sequence. Second, the photolithography was used to pattern the electrode structures on the photoresist. Third, the O_2 plasma treatment was adopted to etch the PS layer with the same structure of the upper photoresist layer. And then the free-standing polymer mask can be lift off onto the wafer and then transferred to the holding metal mask for depositing the metal electrodes.

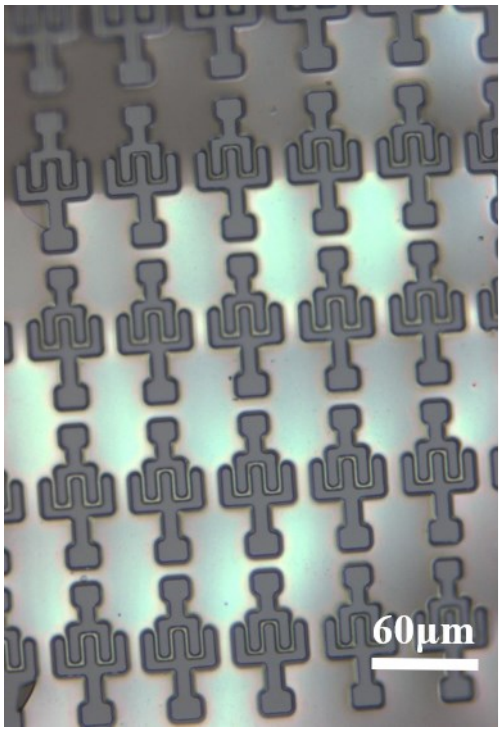

Figure S1 The optical image of the final structure of the polymer mask.

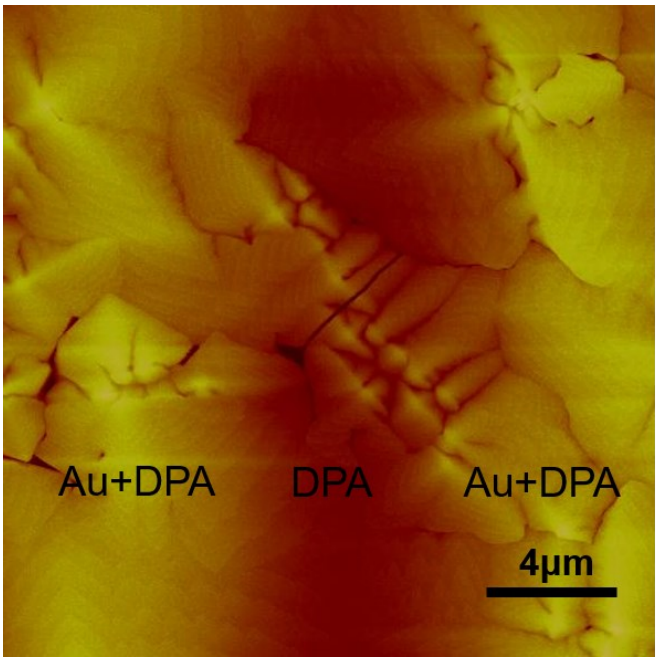

Figure S2 AFM image of the channel and semiconductor.

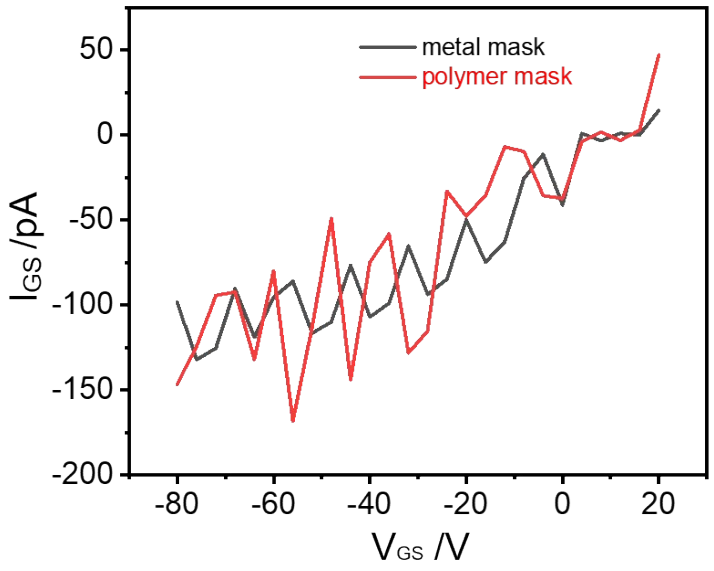

Figure S3 The leakage current of the device with metal mask and polymer mask.

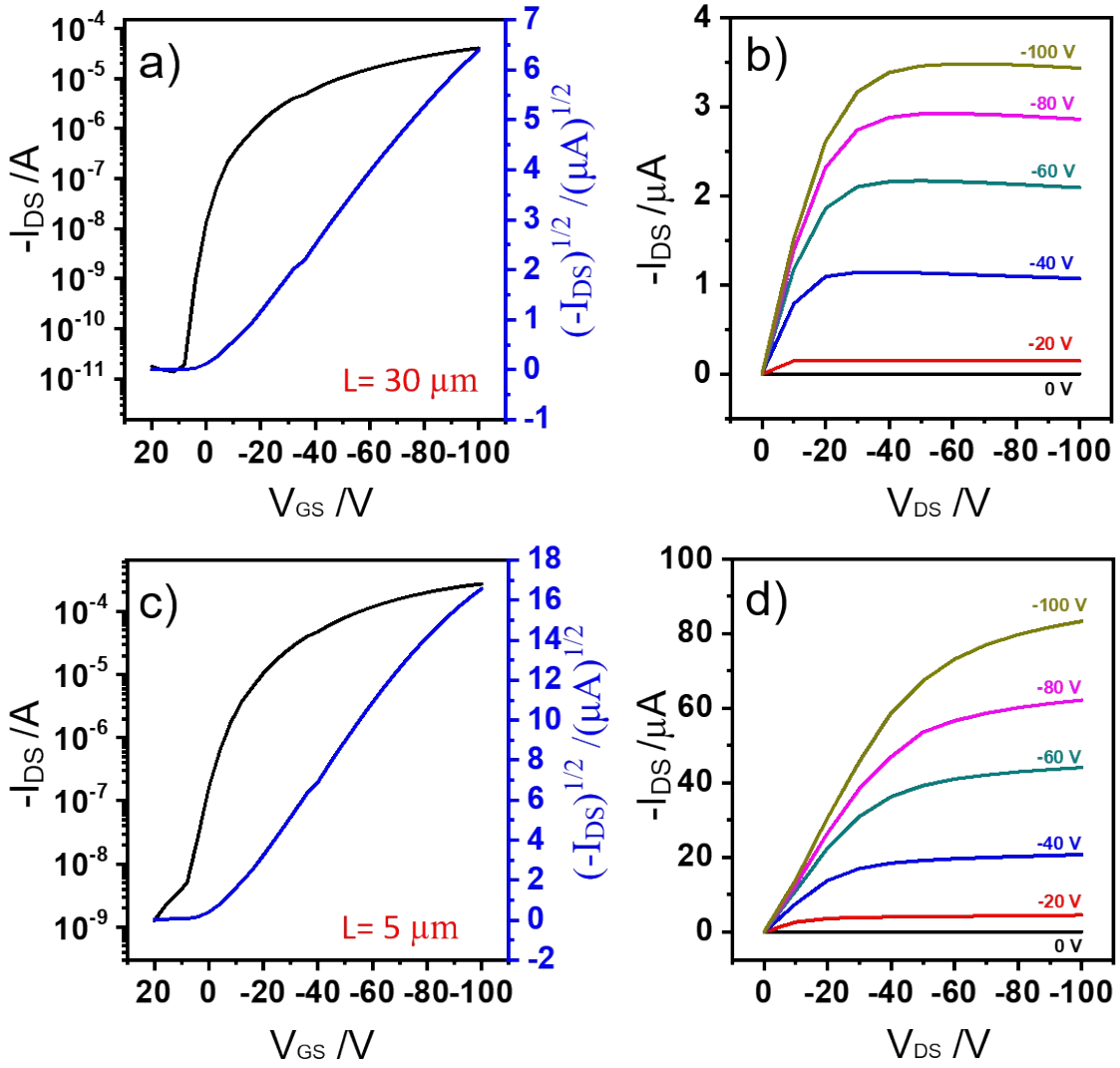

Figure S4 (a-b) Typical transfer and output characteristics of the transistor based on pentacene using metal mask. (c-d) Typical transfer and output characteristics of the transistor based on pentacene using polymer masks.

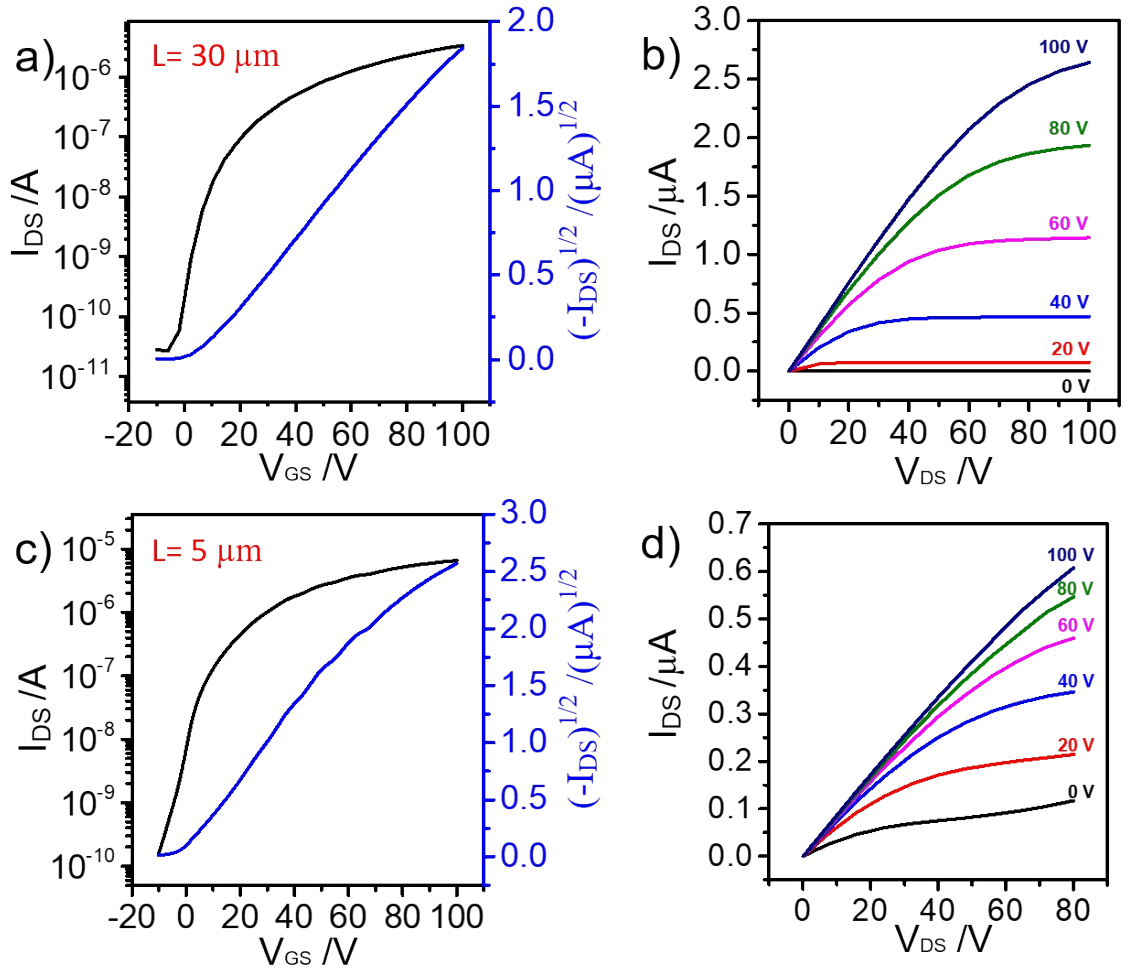

Figure S5 (a-b) Typical transfer and output characteristics of the transistor based on CuPc using metal mask. (c-d) Typical transfer and output characteristics of the transistor based on CuPc using polymer masks.

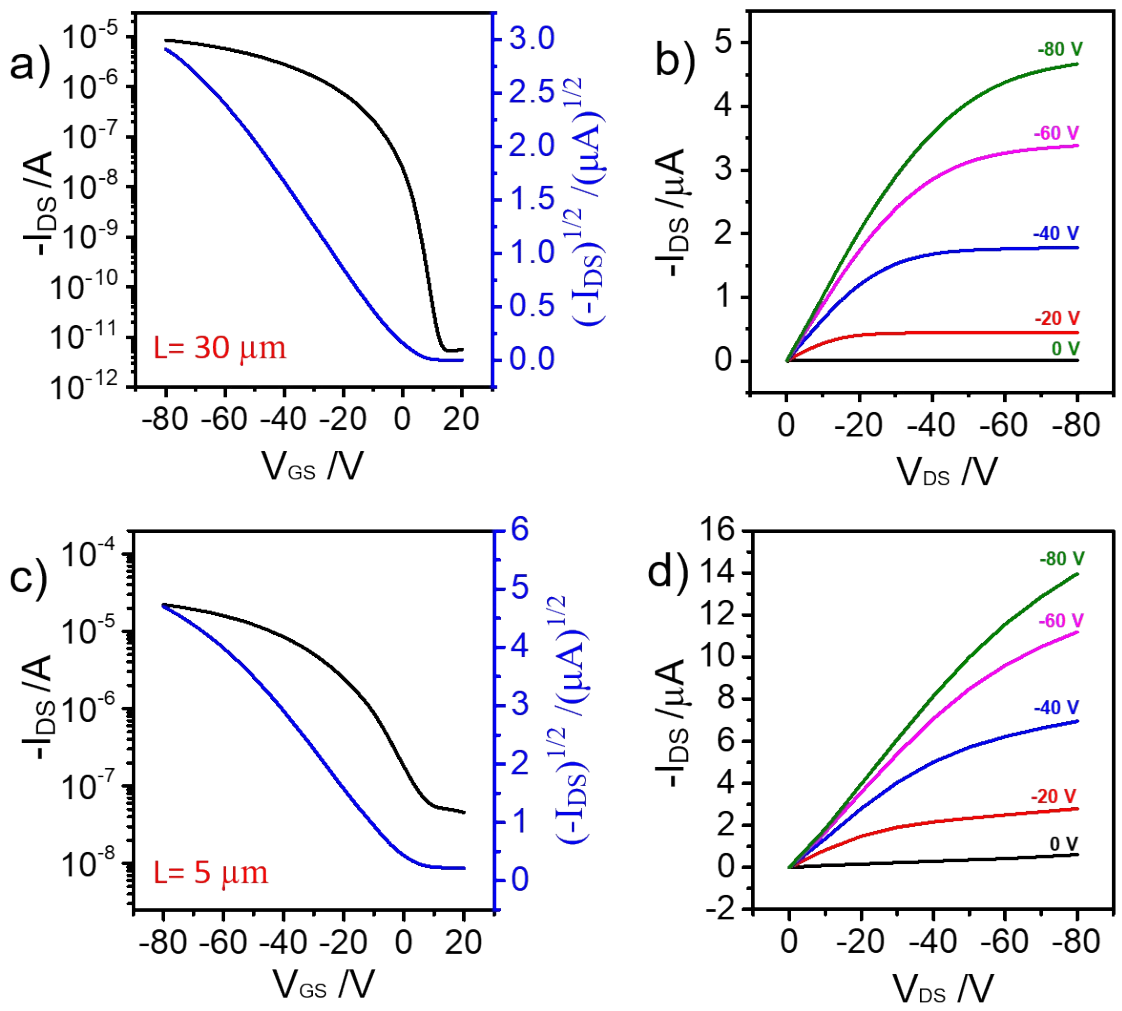

Figure S6 (a-b) Typical transfer and output characteristics of the transistor based on F_{16}CuPc using metal mask. (c-d) Typical transfer and output characteristics of the transistor based on F_{16}CuPc using polymer masks.