Electronic Supplementary Material (ESI) for RSC Advances.

Supplementary Material

Vertical Stacked SnSe Homojunction and Negative Capacitance for Fast Low-Power Tunneling Transistors

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Table S1. The optimized lattices and band gaps of bulk, BL, and ML SnSe obtained with the PBE, Grimme DFT-D2, and Grimme DFT-D3 functionals using linear combination of atomic orbitals (LCAO) compared with former theoretical data using the projector augmented wave (PAW) formalism and experimental data [1]. E_g values in the parentheses are the direct band gap.

		a (Å)	**b (Å)**	**c (Å)**	$\boldsymbol{E_g}$ **(eV)**
Bulk	PBE (LCAO)	4.25	4.54	11.84	0.63 (0.87)
	D2 (LCAO)	4.23	4.41	11.84	0.57 (0.71)
	D3 (LCAO)	4.25	4.60	11.86	0.72 (1.00)
	PBE (PAW) [1]	4.22	4.49	11.66	0.73
	D2 (PAW) [1]	4.17	4.44	11.51	0.79
	Exp [1]	4.15	4.44	11.50	0.86, 0.90
BL	PBE (LCAO)	4.29	4.44	2.97[d]	0.91 (1.08)
	D2 (LCAO)	4.24	4.41	3.17[d]	0.80 (1.00)
	D3 (LCAO)	4.28	4.54	2.79[d]	1.04 (1.20)
	D2 (PAW) [1]	4.25	4.43	—	0.82
ML	D2 (LCAO)	4.25	4.38	—	0.88 (0.98)
	D2 (PAW) [1]	4.30	4.36	—	0.92

[d] is the nearest distance between the two layers.

Table S2. Effect of the stacked positions on I_{leak} and I_{on} of the vertical SnSe homojunction TFET. I_{on} of the ITRS HP device is given for comparation. Here, L_g = 10 nm; V_{dd} = 0.74 V; N_s/N_d: $5/5\times10^{13}$ cm^{-2}. I_{leak}: leakage current; I_{off}: off-state current; I_{on}: on-state current.

	stacked position	I_{leak} (μA/μm)	I_{off} (μA/μm)	I_{on} (μA/μm)
p-type	left	0.0027	0.1	716
	central	0.0027	0.1	791
	right	0.0013	0.1	444
n-type	left	0.0027	0.1	653
	central	0.0027	0.1	695
	right	0.0013	0.1	684
ITRS	—	—	0.1	1287

Table S3. Effect of the doping concentration on I_{leak} and I_{on} of the vertical SnSe homojunction TFET. Those of the ITRS HP/LP devices and that of its planar counterpart are given for comparation. Here, stacked site is central; L_g = 10 nm; V_{dd} = 0.74 V. N_s/N_d: source/drain doping concentration. I_{leak}: leakage current; I_{off}: off-state current; I_{on}: on-state current; HP: high performance; LP: lower power.

	N_s/N_d ($\times 10^{13}$ cm^{-2})	I_{leak} (μA/μm)	I_{off} (HP) (μA/μm)	I_{on} (HP) (μA/μm)	I_{off} (LP) (μA/μm)	I_{on} (LP) (μA/μm)
p-type	1/5	~10^{-4}	0.1	790	—	—
	0.3/5	~10^{-5}	0.1	700	2×10^{-5}	389
	0.1/5	~10^{-5}	0.1	727	2×10^{-5}	488
n-type	5/1	~10^{-4}	0.1	640	—	—
	5/0.3	~10^{-5}	0.1	443	2×10^{-5}	225
	5/0.1	~10^{-7}	0.1	722	2×10^{-5}	235
Planar SnSe TFET [2]	1/5	~10^{-2}	0.1	1667	—	—
ITRS	—	—	0.1	1287	2×10^{-5}	461

Table S4. The SS_{min}, SS_{ave_4dec}, and I_{60} of the optimal sub-10 nm vertical SnSe homojunction *p*-TFETs.

L_g (nm)	V_{dd} (V)	UL (nm)	SS_{min} (mV/dec)	SS_{ave_4dec} (mV/dec)	I_{60} (μA/μm)
10	0.74	0	43.4	45.8	7
10	0.5	0	42.0	44.2	5
7	0.65	3	60.7	71.2	——
5	0.65	5	66.7	90.1	——

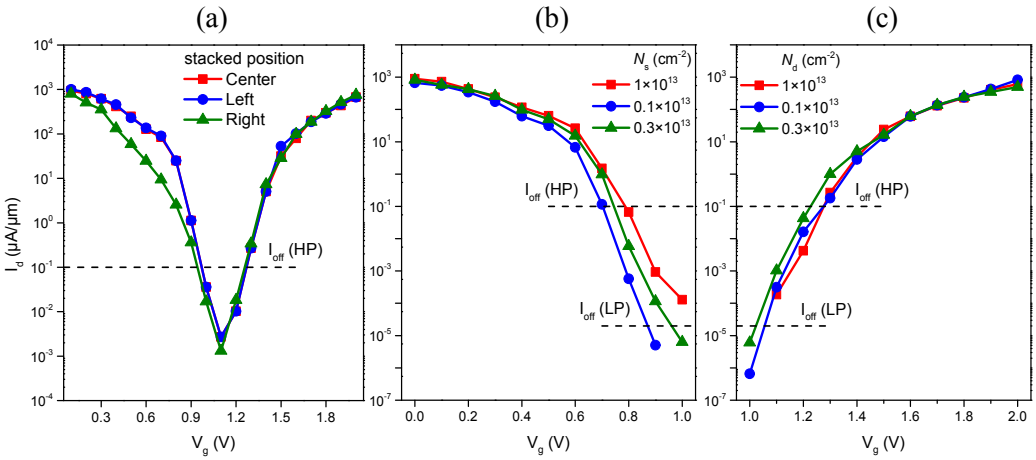

Figure S1. Transfer characteristics of the vertical SnSe homojunction TFETs with (a) stacked position and (b-c) doping concentrations.

References

[1] Y.C. Huang, X. Chen, C. Wang, L. Peng, Q. Qian, S.F. Wang, Layer-dependent electronic properties of phosphorene-like materials and phosphorenebased van der Waals heterostructures, Nanoscale, 9 (2017) 8616-8622.

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