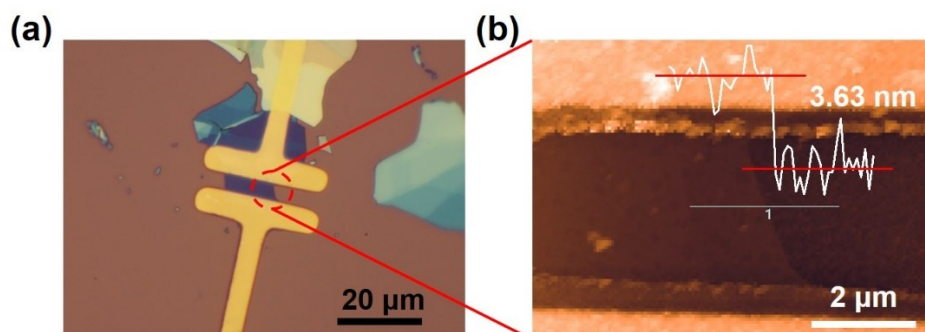**Supporting Information**

Figure S1. Optical microscopy image and atomic force microscopy (AFM) image

of few-layer WSe_2 field effect transistors. (a) Optical microscopy image of few-layer

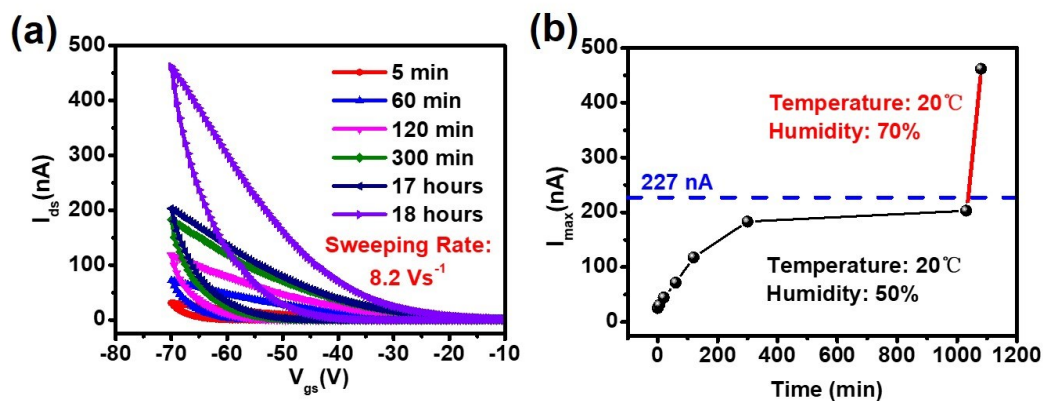WSe_2 field effect transistors. (b) Atomic force microscopy image of the channel in (a),

3.63-nm thick.

Figure S2. Electrical properties of the WSe_2 FETs exposed in ambient. (a) Double

sweeping transfer curves of the WSe_2 field effect transistors exposed in ambient with

different time. In the first 17 hours, the device was placed in an atmosphere with 50%

1

humidity, and the last transfer curve was measured in an atmosphere with 70% humidity for 60 minutes. (b) Maximum output current (I_{max}) as a function of exposure time in ambient, where the initial maximum output current value is 227 nA corresponding to the blue dotted line in (b).
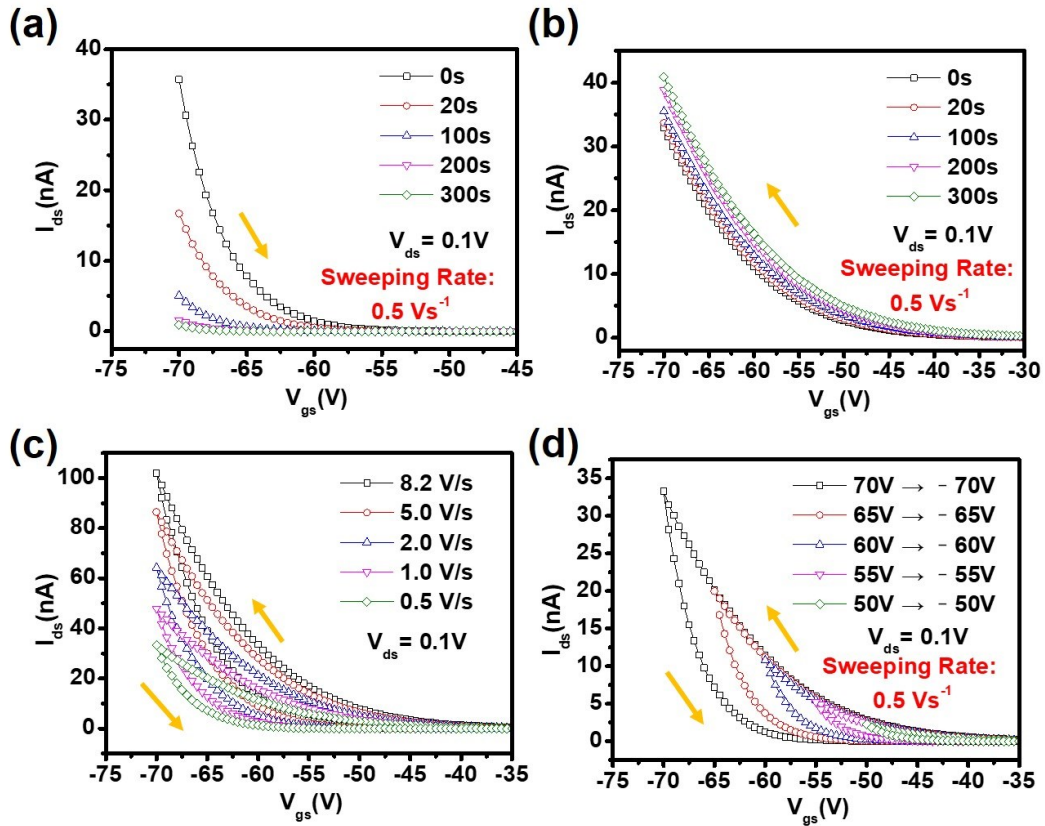

Figure S3. Gate bias instability of the WSe$_2$ FETs in vacuum. (a) Negative gate bias stress under different stress time. (b) Positive gate bias stress under different stress times. (c) Double sweeping transfer curves with different sweeping rates. (d) Double sweeping transfer curves with different gate sweeping ranges. The source-drain voltage is 0.1 V while the sweeping rate is 0.5 V·s^{-1} except for (c).
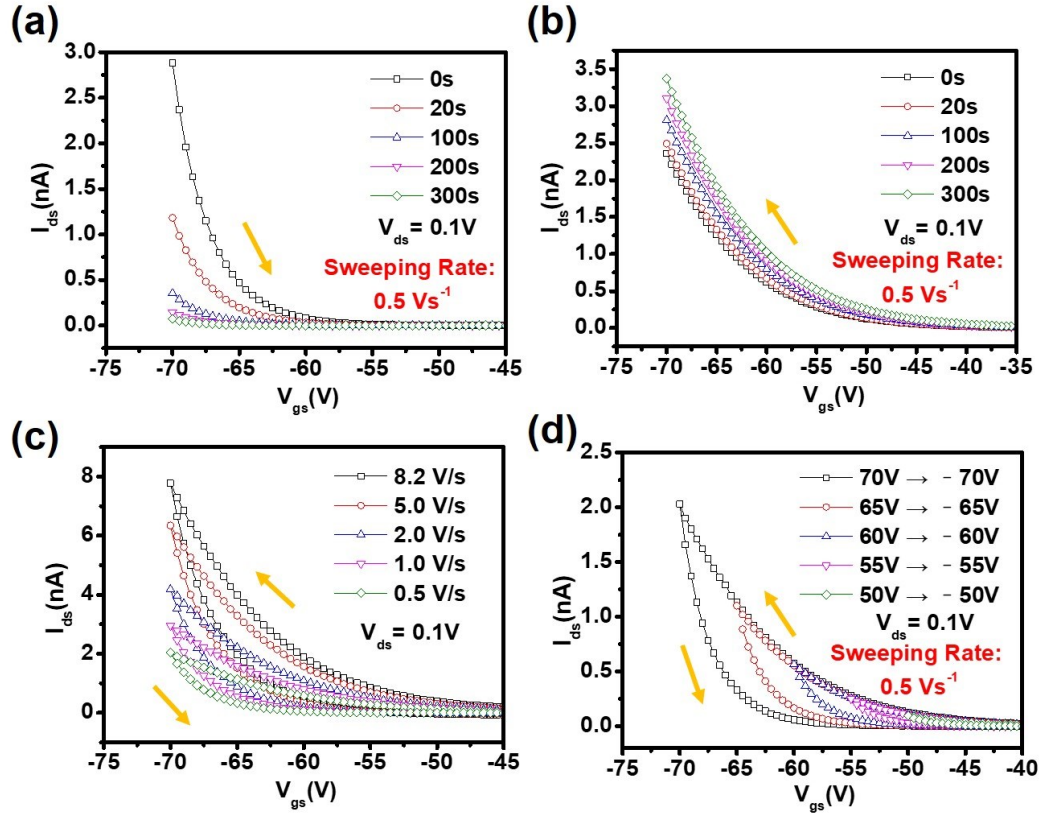
Figure S4. Gate bias instability of the WSe_2 FETs after in-situ annealing in vacuum. (a) Negative gate bias stress under different stress time. (b) Positive gate bias stress under different stress times. (c) Double sweeping transfer curves with different sweeping rates. (d) Double sweeping transfer curves with different gate sweeping ranges. The source-drain voltage is 0.1 V while the sweeping rate is 0.5 V·s^{-1} except for (c).
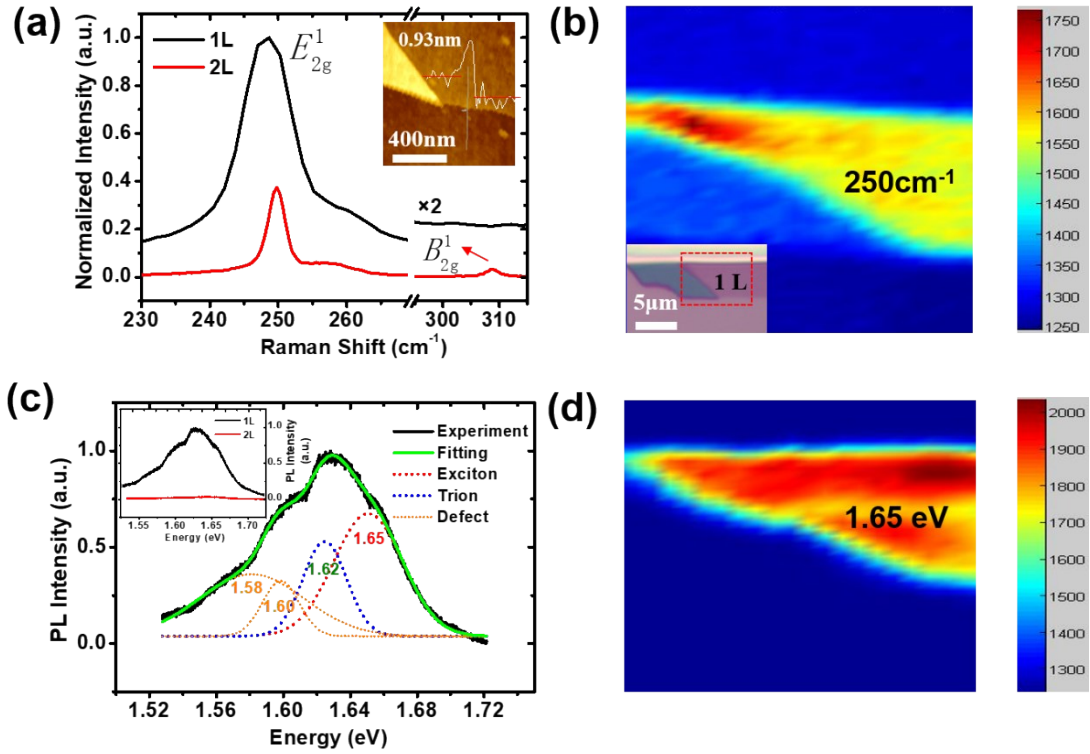
Figure S5. Raman and PL properties of the exfoliated WSe$_2$ flakes. (a) Raman spectra of WSe$_2$, where 248.6 cm^{-1} (1L) and 249.8 cm^{-1} (2L) correspond to the E_{2g}^1 Raman modes. There is no B_{2g}^1 Raman modes (~308 cm^{-1}) in black Raman spectrum, which indicates that WSe$_2$ is monolayer.[1] (Inset) The upper right corner is the AFM image of monolayer WSe$_2$, 0.93-nm thick. (b) Raman mapping corresponding to the red dashed area in the lower left corner. (Inset) The lower left corner is the optical microscopy image of monolayer WSe$_2$. (c) PL spectrum of monolayer WSe$_2$. PL spectrum were fitted with exciton, trion and defects emission peaks, which indicates the existence of intrinsic defects in monolayer WSe$_2$.[2, 3] Therefore, it can be indirectly proved that there are intrinsic defects in the few-layer WSe$_2$. (Inset) The upper left corner inset shows the PL spectra of monolayer WSe$_2$ and bi-layer WSe$_2$. (d) PL mapping corresponding to the red dashed area in (a). Raman and PL measurements were conducted on Andor

SR-500i-A-R Raman spectrometer system with a 532 nm excitation laser. The measurements are performed in a confocal micro configuration using a 100X microscope objective lens, and the corresponding numerical aperture is 0.9. The power of laser excitation is set to be 60 μW for the Raman and PL properties of WSe_2. All measurements are performed in ambient.
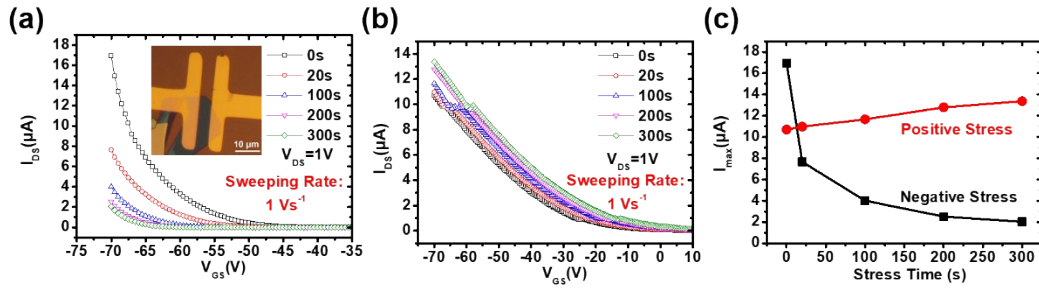

Figure S6. Effect of gate bias stress on the electrical properties of 9-layer WSe_2 FETs. (a) Negative stress under different stress time. (b) Positive stress under different stress time. (c) Maximum output current (I_{max}) as a function of stress time. During the measurement of these transfer curves under atmosphere, the source-drain voltage is fixed at 1 V, while the voltage sweeping rate is controlled to 1 $V·s^{-1}$.
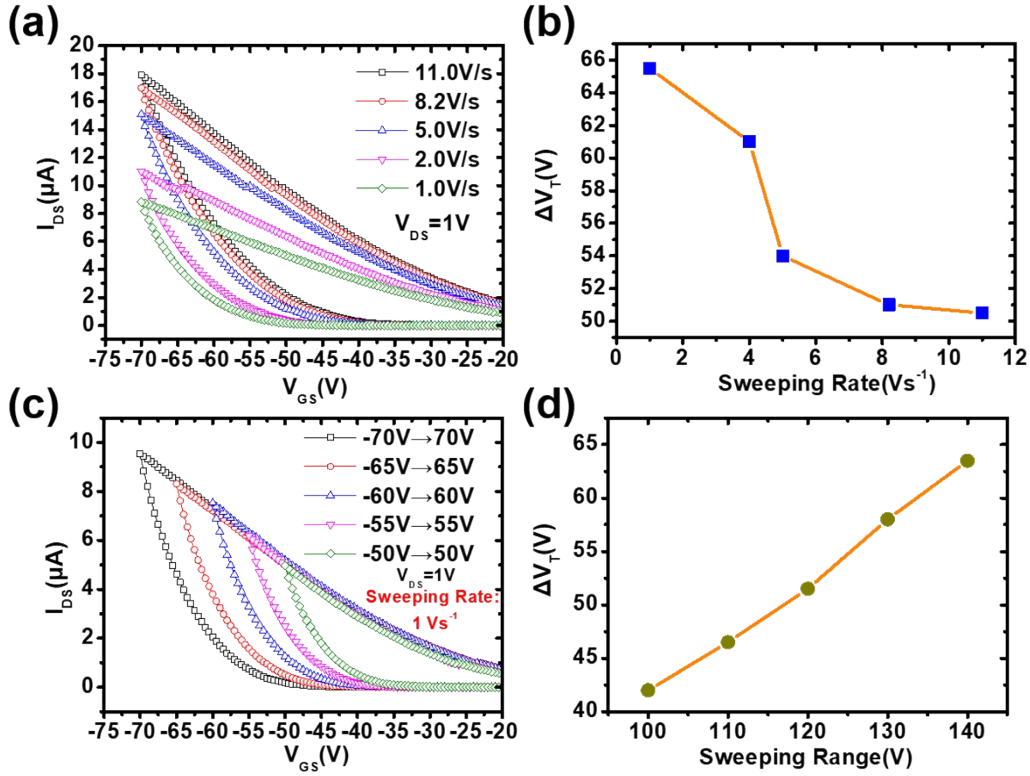
Figure S7. Hysteresis characteristics of the 9-layer WSe$_2$ FETs. (a) Double sweeping transfer curves with different sweeping rates. (b) Change of threshold voltage as a function of the voltage-sweeping rate. (c) Double sweeping transfer curves with different gate sweeping ranges, where the sweeping rate is 1 V·s^{-1}. (d) Threshold voltage difference as a function of the sweeping range. The source-drain voltage is 1 V.
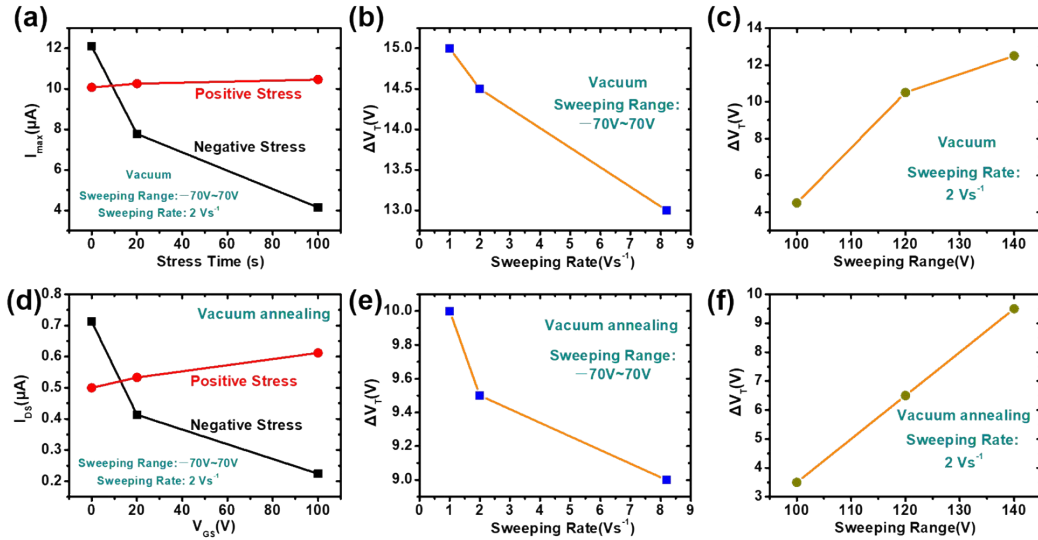

Figure S8. Gate bias instability of the 9-layer WSe$_2$ FETs in different conditions. (a) Maximum output current (I_{max}) as a function of stress time in vacuum (b) Threshold

6

voltage difference as a function of sweeping rate in vacuum. (c) Threshold voltage as a function of the sweeping range in vacuum. (d) Maximum output current (I_{max}) as a function of stress time after in-situ annealing in vacuum (e) Threshold voltage difference as a function of sweeping rate after in-situ annealing in vacuum. (f) Threshold voltage as a function of the sweeping range after in-situ annealing in vacuum.
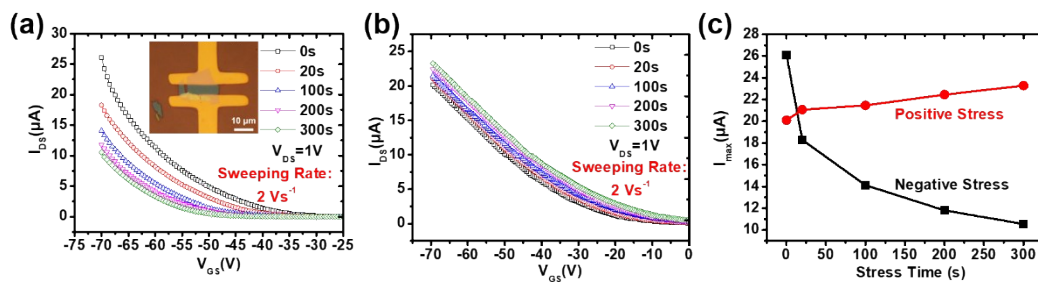

Figure S9. Effect of gate bias stress on the electrical properties of 14-layer WSe_2 FETs.

(a) Negative stress under different stress time. (b) Positive stress under different stress time. (c) Maximum output current (I_{max}) as a function of stress time. During the measurement of these transfer curves under atmosphere, the source-drain voltage is fixed at 1 V, while the voltage sweeping rate is controlled to 2 V·s^{-1}.
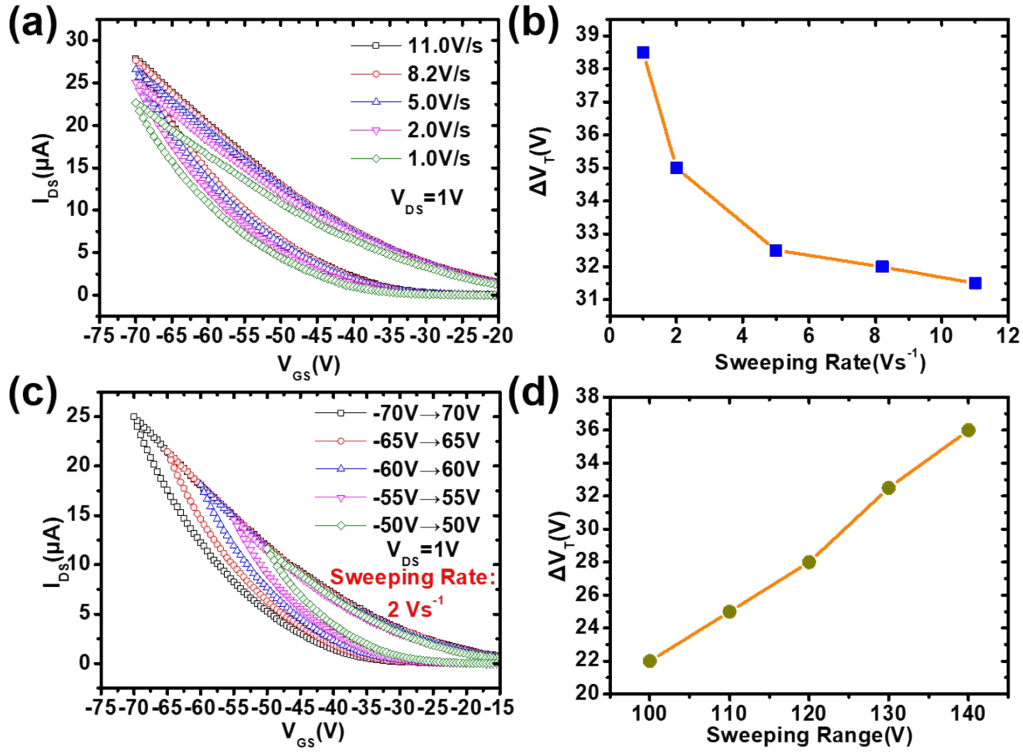
Figure S10. Hysteresis characteristics of the 14-layer WSe$_2$ FETs. (a) Double sweeping transfer curves with different sweeping rates. (b) Change of threshold voltage as a function of the voltage-sweeping rate. (c) Double sweeping transfer curves with different gate sweeping ranges, where the sweeping rate is 2 V·s^{-1}. (d) Threshold voltage difference as a function of the sweeping range. The source-drain voltage is 1 V.
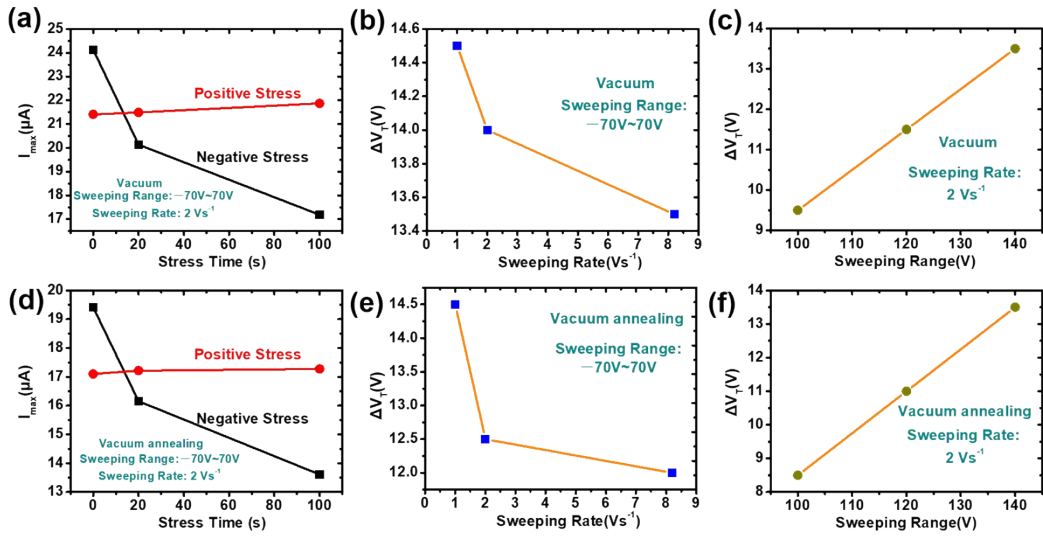
Figure S11. Gate bias instability of the 14-layer WSe_2 FETs in different conditions. (a) Maximum output current (I_{max}) as a function of stress time in vacuum (b) Threshold voltage difference as a function of sweeping rate in vacuum. (c) Threshold voltage as a function of the sweeping range in vacuum. (d) Maximum output current (I_{max}) as a function of stress time after in-situ annealing in vacuum (e) Threshold voltage difference as a function of sweeping rate after in-situ annealing in vacuum. (f) Threshold voltage as a function of the sweeping range after in-situ annealing in vacuum.
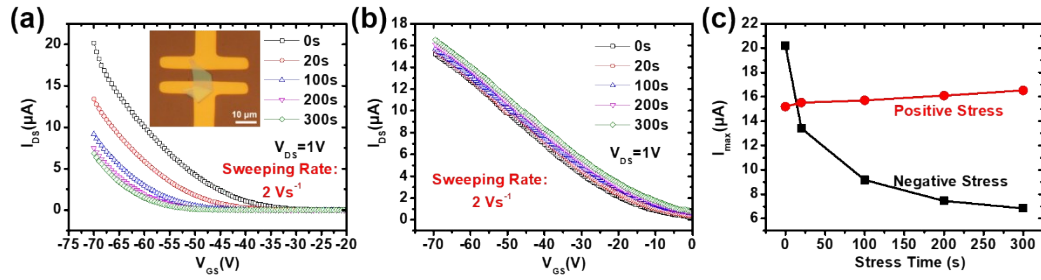

Figure S12. Effect of gate bias stress on the electrical properties of 18-layer WSe_2 FETs.

(a) Negative stress under different stress time. (b) Positive stress under different stress time. (c) Maximum output current (I_{max}) as a function of stress time. During the measurement of these transfer curves under atmosphere, the source-drain voltage is fixed at 1 V, while the voltage sweeping rate is controlled to 2 V·s^{-1}.
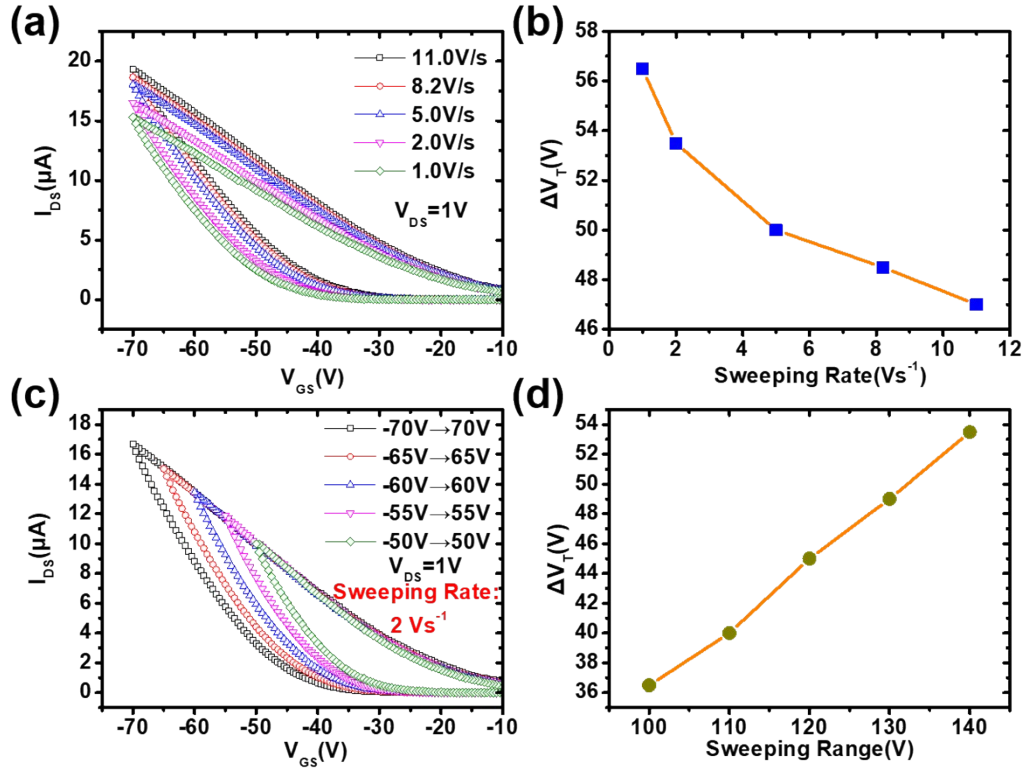
Figure S13. Hysteresis characteristics of the 18-layer WSe$_2$ FETs. (a) Double sweeping transfer curves with different sweeping rates. (b) Change of threshold voltage as a function of the voltage-sweeping rate. (c) Double sweeping transfer curves with different gate sweeping ranges, where the sweeping rate is 2 V·s^{-1}. (d) Threshold voltage difference as a function of the sweeping range. The source-drain voltage is 1 V.
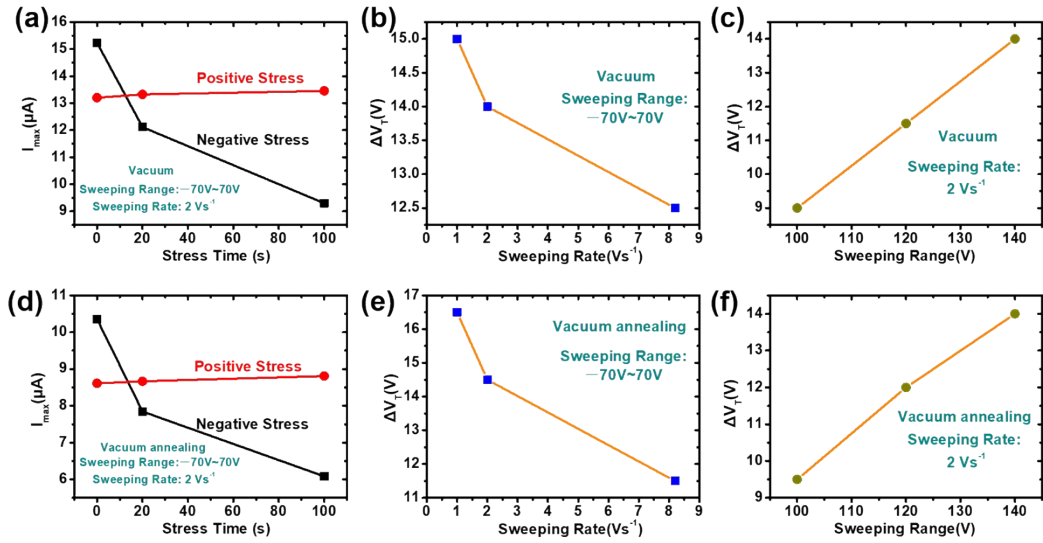
Figure S14. Gate bias instability of the 18-layer WSe$_2$ FETs in different conditions. (a) Maximum output current (I_{max}) as a function of stress time in vacuum (b) Threshold voltage difference as a function of sweeping rate in vacuum. (c) Threshold voltage as a function of the sweeping range in vacuum. (d) Maximum output current (I_{max}) as a function of stress time after in-situ annealing in vacuum (e) Threshold voltage difference as a function of sweeping rate after in-situ annealing in vacuum. (f) Threshold voltage as a function of the sweeping range after in-situ annealing in vacuum.
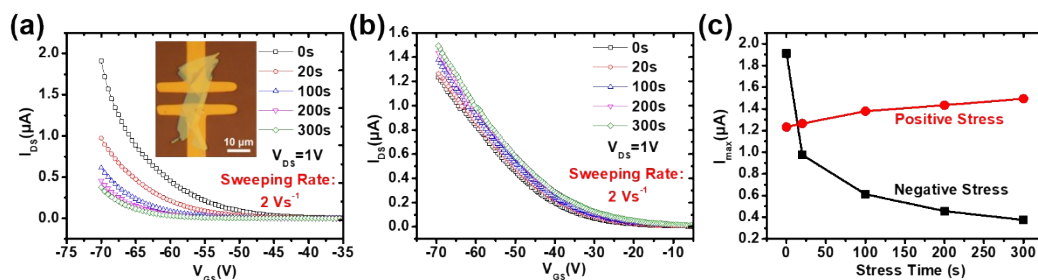

Figure S15. Effect of gate bias stress on the electrical properties of 24-layer WSe$_2$ FETs.

(a) Negative stress under different stress time. (b) Positive stress under different stress time. (c) Maximum output current (I_{max}) as a function of stress time. During the measurement of these transfer curves under atmosphere, the source-drain voltage is fixed at 1 V, while the voltage sweeping rate is controlled to 2 V·s^{-1}.
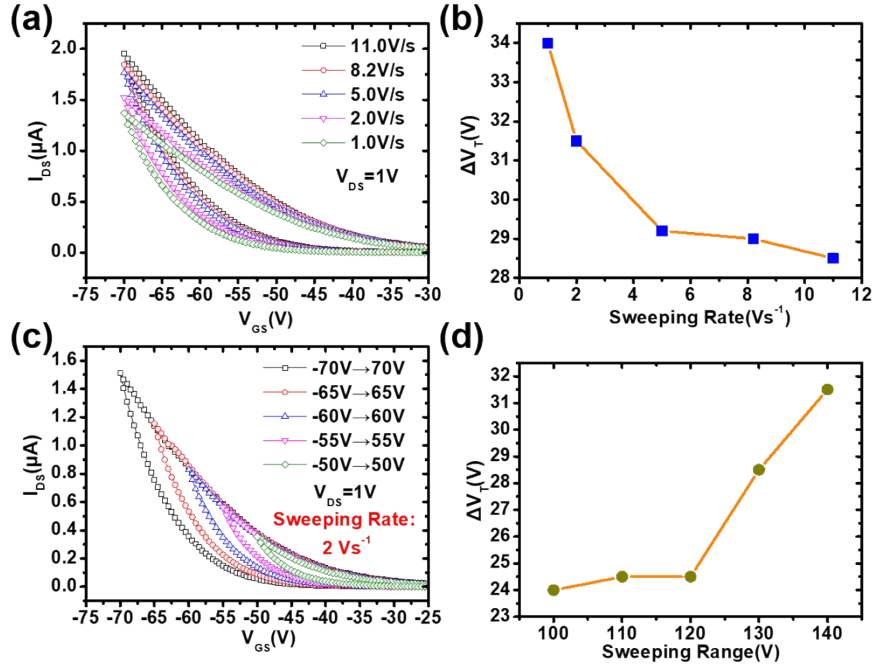
Figure S16. Hysteresis characteristics of the 24-layer WSe$_2$ FETs. (a) Double sweeping transfer curves with different sweeping rates. (b) Change of threshold voltage as a function of the voltage-sweeping rate. (c) Double sweeping transfer curves with different gate sweeping ranges, where the sweeping rate is 2 V·s^{-1}. (d) Threshold voltage difference as a function of the sweeping range. The source-drain voltage is 1 V.
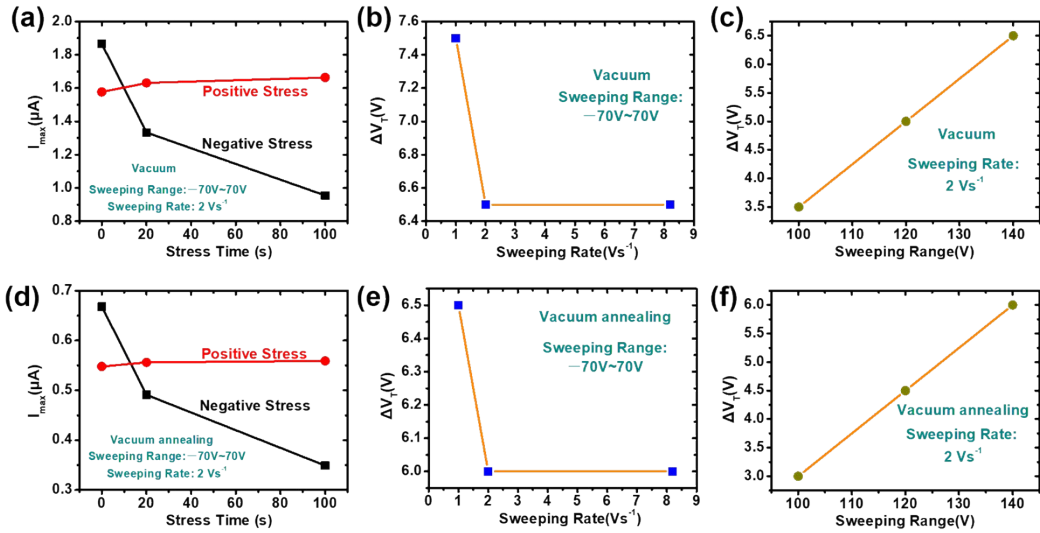

Figure S17. Gate bias instability of the 24-layer WSe$_2$ FETs in different conditions. (a) Maximum output current (I_{max}) as a function of stress time in vacuum (b) Threshold voltage difference as a function of sweeping rate in vacuum. (c) Threshold voltage as a

function of the sweeping range in vacuum. (d) Maximum output current (I_{max}) as a function of stress time after in-situ annealing in vacuum (e) Threshold voltage difference as a function of sweeping rate after in-situ annealing in vacuum. (f) Threshold voltage as a function of the sweeping range after in-situ annealing in vacuum.
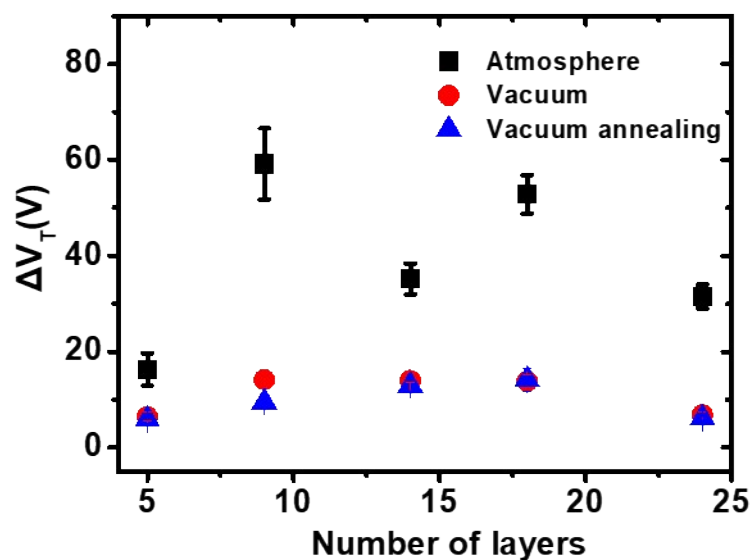

Figure S18. Threshold voltage difference (ΔV_T) of WSe$_2$ with different layer in different environments. The hysteresis of all devices drastically reduces in vacuum and further decreases after in-situ annealing in vacuum compared with that in air.

References

1. P. Tonndorf, R. Schmidt, P. Böttger, X. Zhang, J. Börner, A. Liebig, M. Albrecht,

    C. Kloc, O. Gordan, D. R. T. Zahn, S. M. de Vasconcellos and R. Bratschitsch,

Optics Express, 2013, **21**, 4908-4916.

2. S. Wang, W. Zhao, F. Giustiniano and G. Eda, *Phys. Chem. Chem. Phys.*, 2016, **18**, 4304-4309.

3. W. Zhao, Z. Ghorannevis, L. Chu, M. Toh, C. Kloc, P.-H. Tan and G. Eda, *ACS Nano*, 2013, **7**, 791-797.