Electronic Supplementary Material (ESI) for Journal of Materials Chemistry A.

Supporting information

Using Hysteresis to Predict charge Recombination Properties of Perovskite Solar Cells

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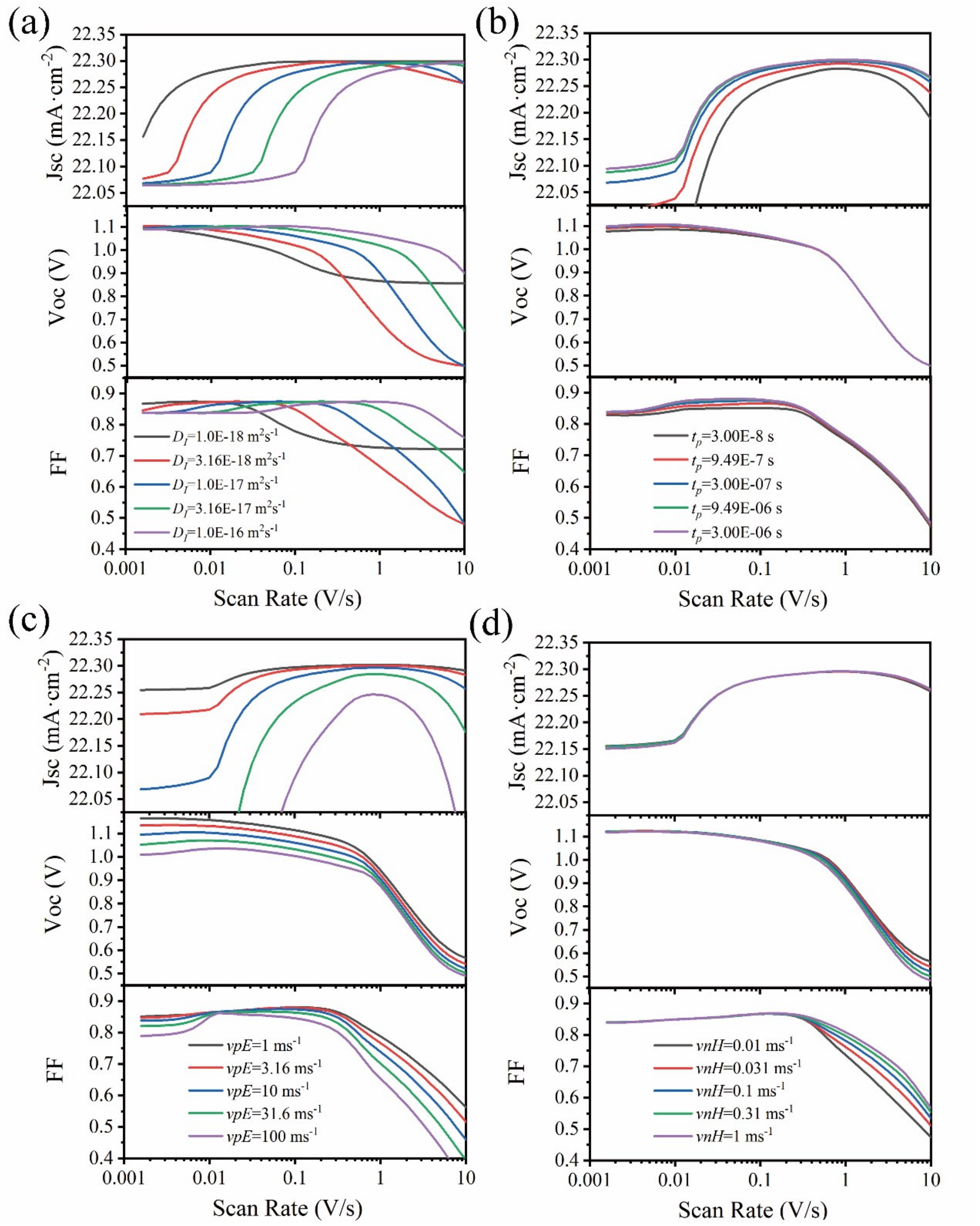

Figure S1 Simulated PSC performance under different scanning rates with different characteristics (a) D_I values (b) t_p values (c) *vpE* values (d) *vnH* values.

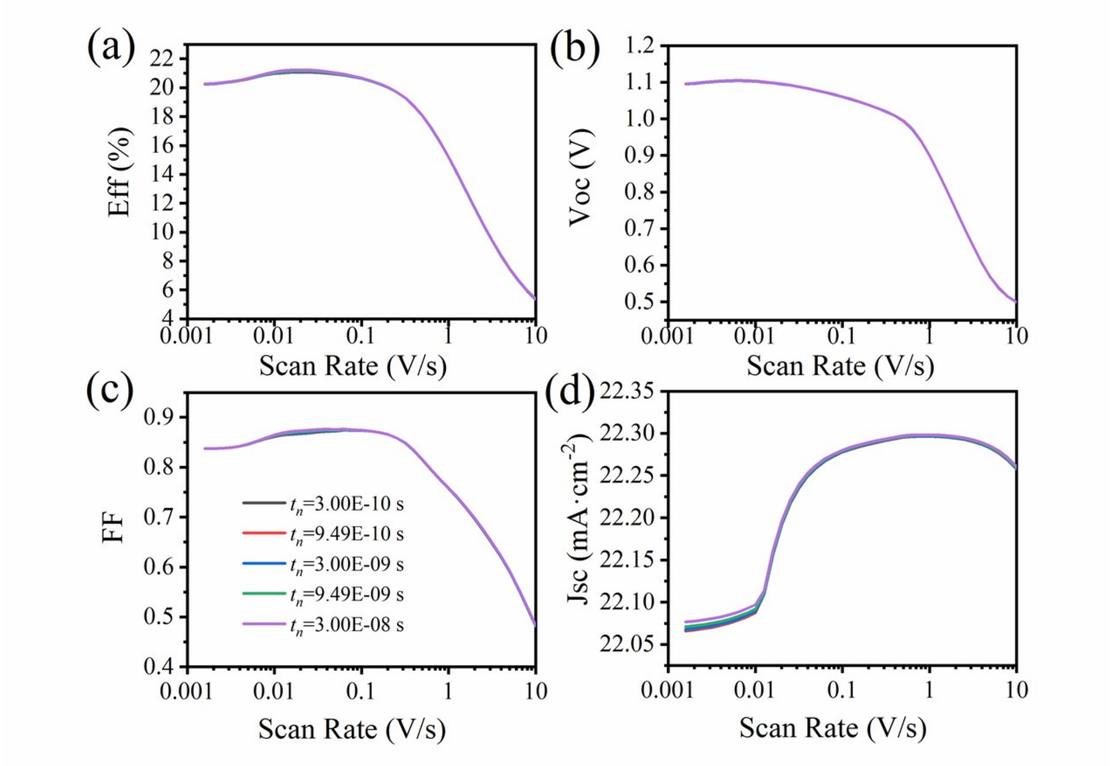

Figure S2. Simulated PSC performance under different scanning rates with different tn values (a) efficiency (b) Voc (c) FF (d) Jsc

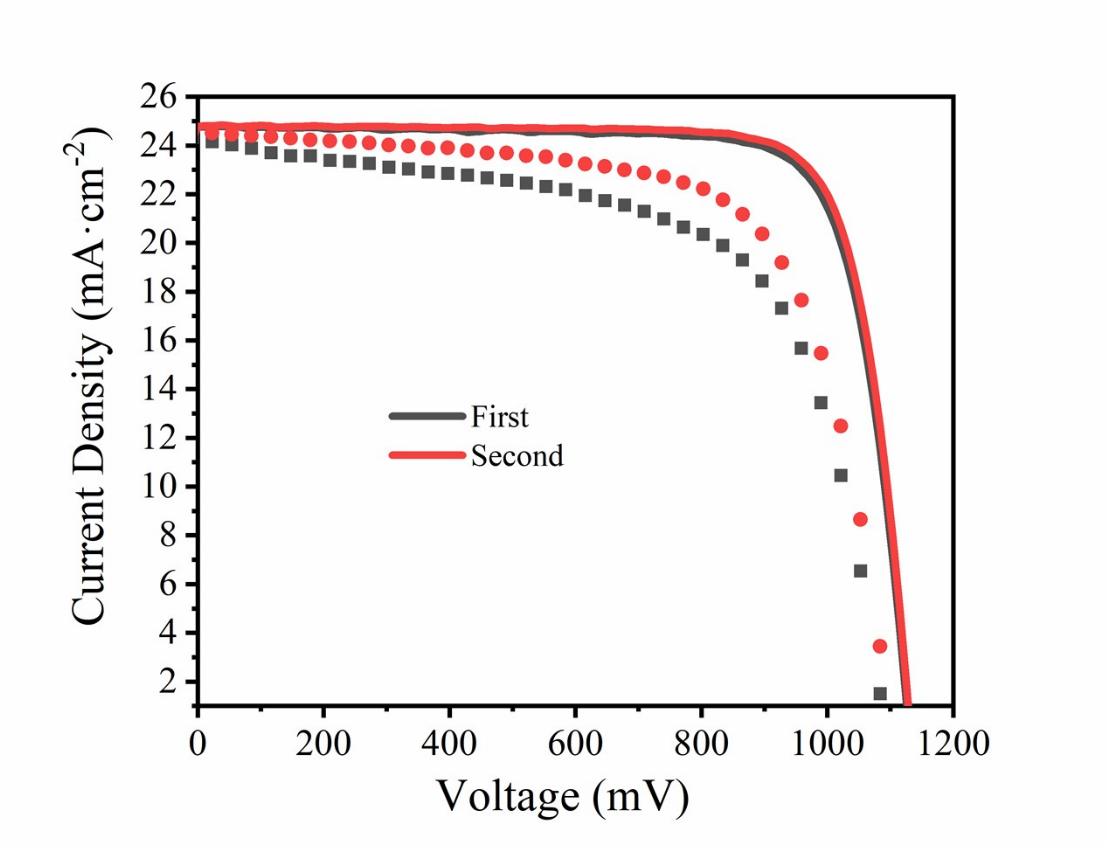

Figure S3. Two consecutive IV test results of the same PSC.

Table S1. Two consecutive IV test results of the same PSC.

	J_{sc} (mA cm^{-2})	**V_{oc}** (V)	**FF**	**B-PCE** (%)	**F-PCE** (%)
First	24.76	1.13	0.79	22.10	16.69
Second	24.75	1.13	0.80	22.37	14.48

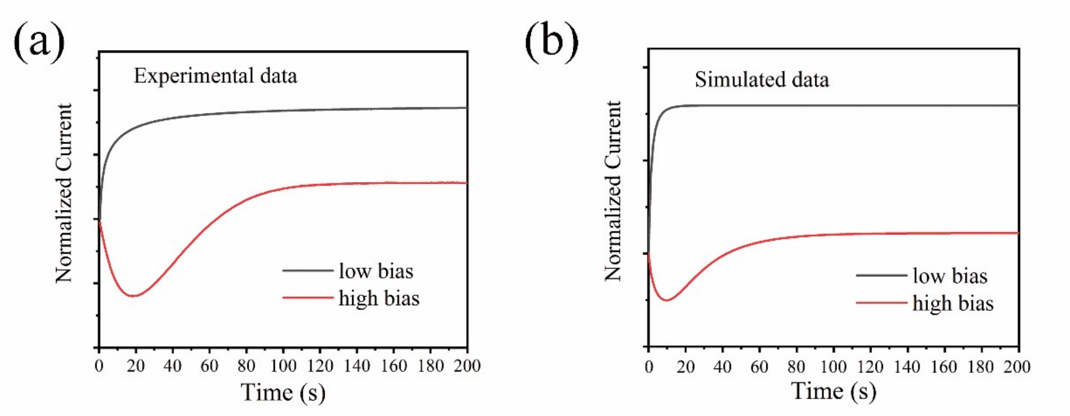

Figure S4. Unique IT curves of PSCs (a) experimental date. (b) Simulated data.

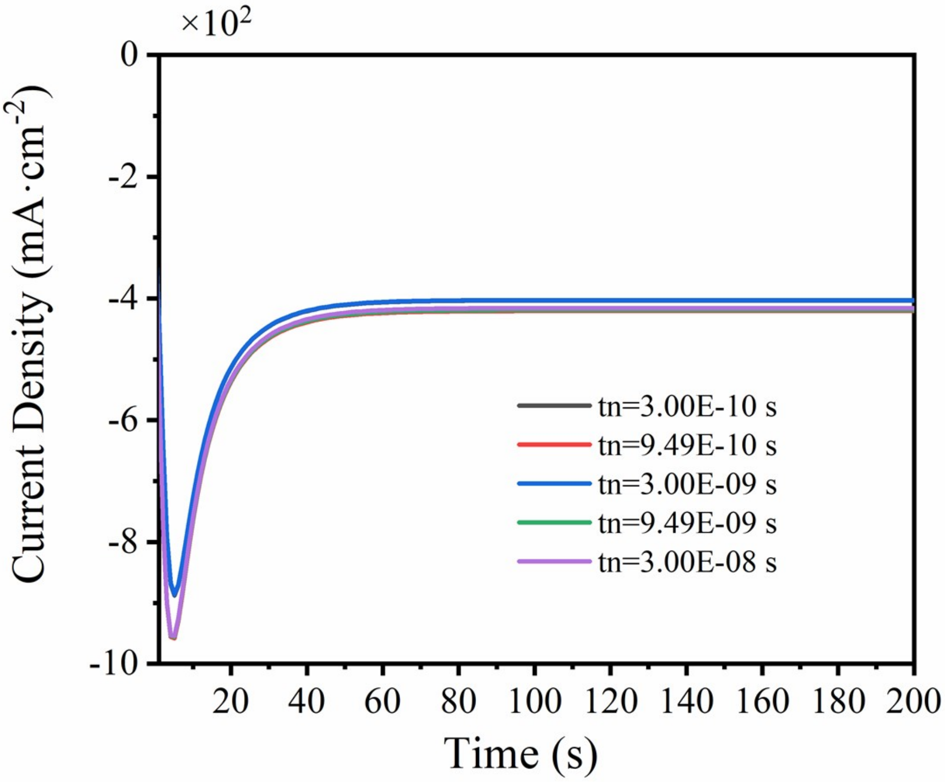

Figure S5. Simulated IT curve with different tn values.

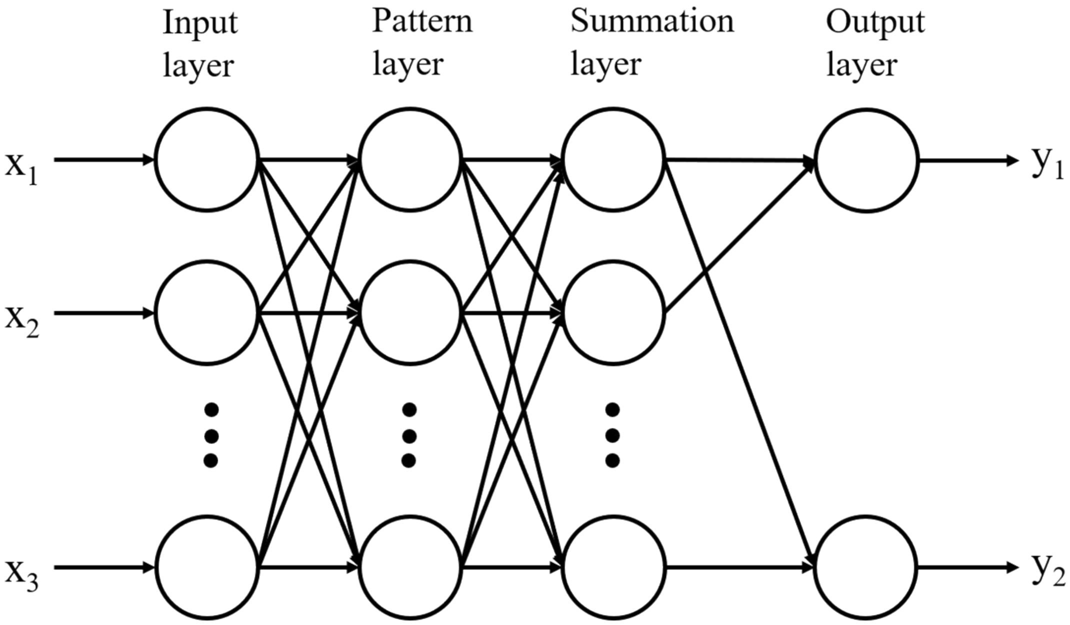

Figure S6. Structure diagram of generalized regression neural network

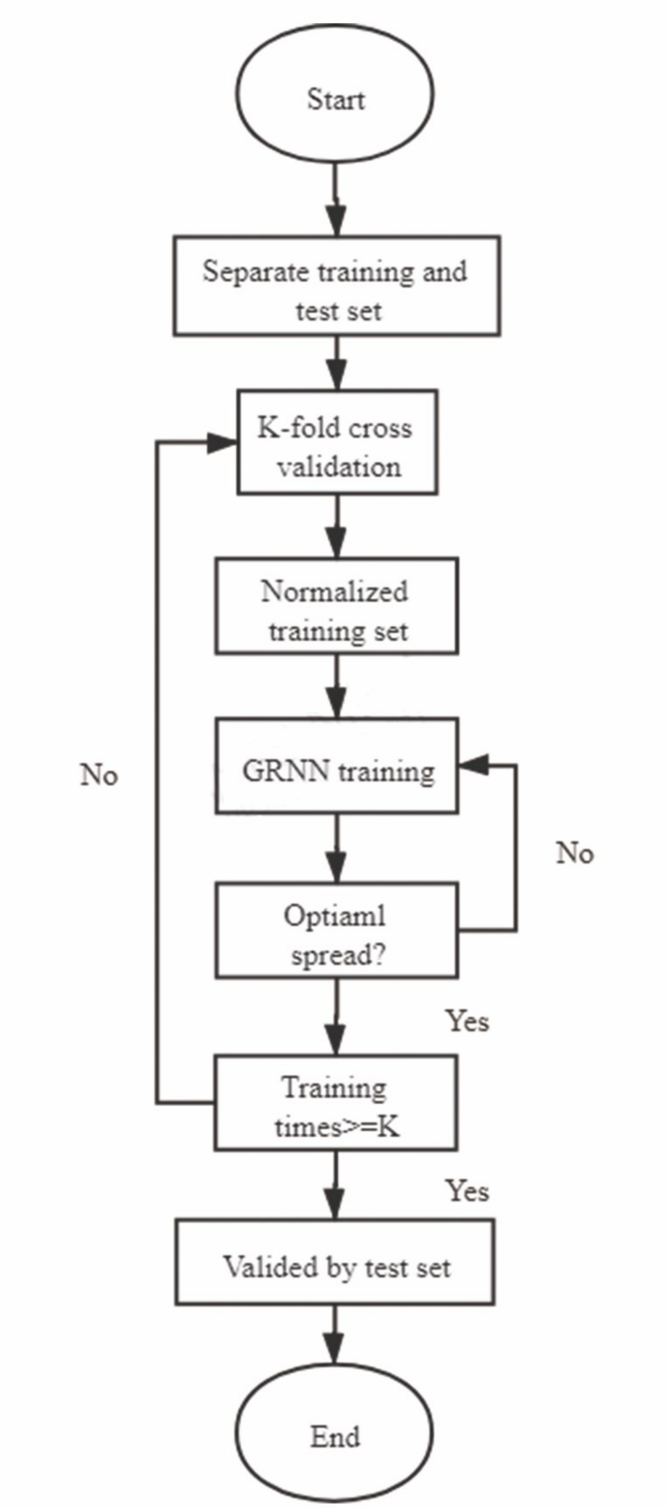

Figure S7. Flow diagram of the GRNN training.

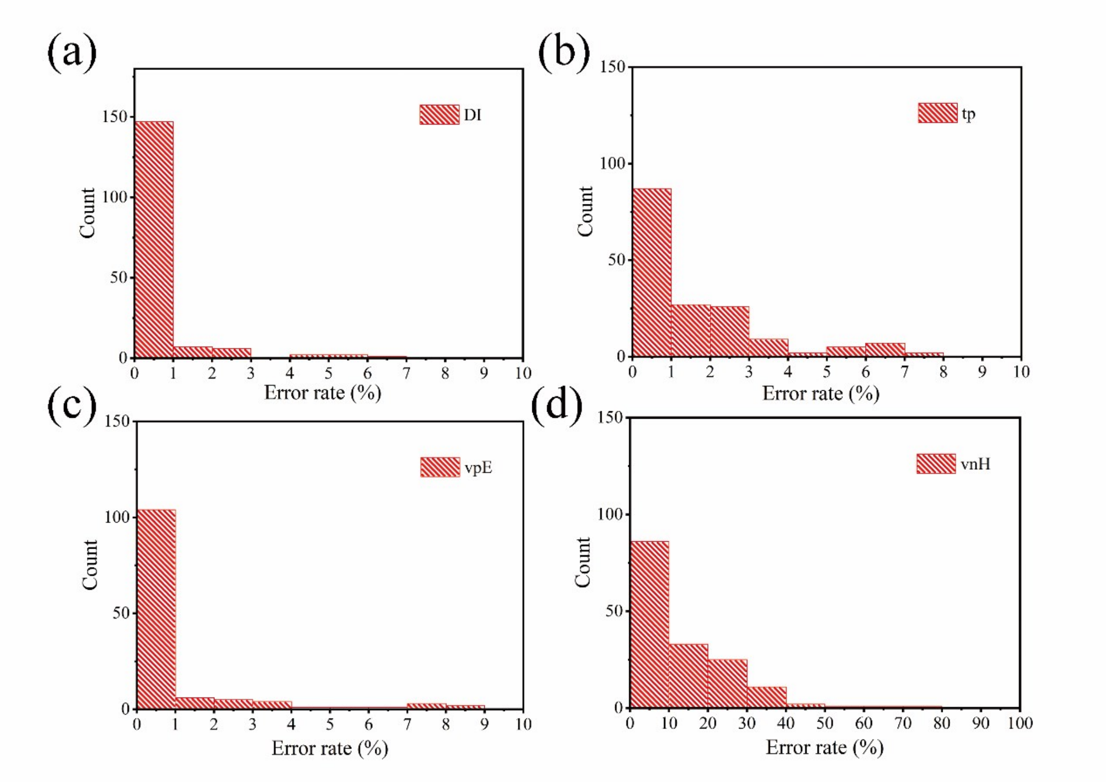

Figure S8. Error rate statistical data and distributions of validation results of different IT curves predicting device values through GNRR (a) D_I. (b) t_p. (c) vpE. (d) vnH.

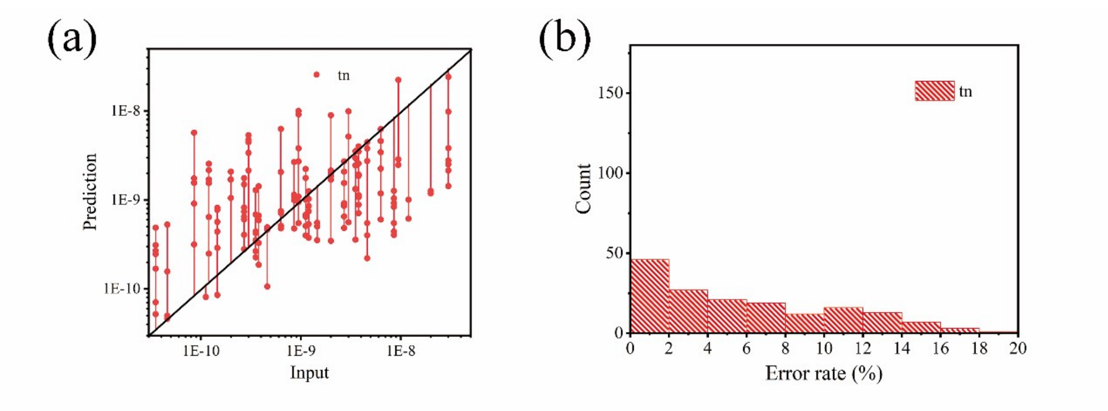

Figure S9. GRNN validation result and error rate of t_n.

Table S2. Device IV performance of four really PSCs.

	Jsc(mA/cm^2)	Voc(V)	FF	B-PCE(%)	F-PCE(%)
Device A	24.506	1073.148	0.787	20.691	15.403
Device B	24.351	1121.122	0.794	21.687	18.331
Device C	24.495	1079.548	0.787	20.816	16.943
Device D	24.291	1102.309	0.788	21.088	14.735

Method of defect state separation

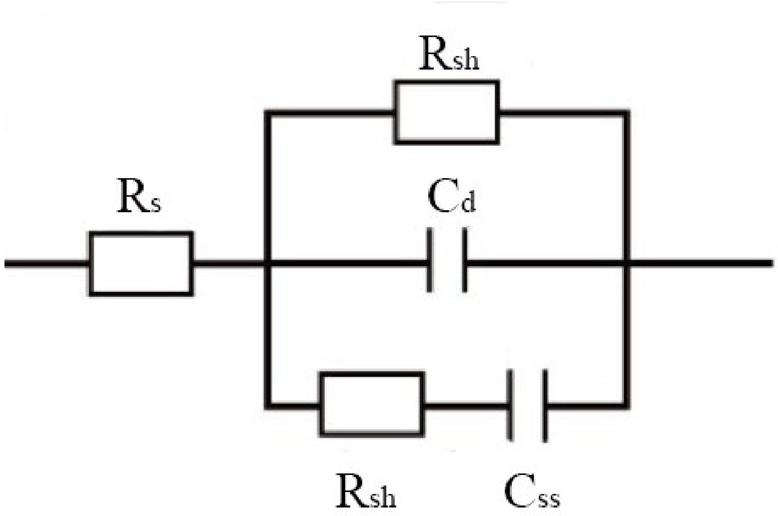

Figure S10. An expanded equivalent circuit model describing the charge transfer and recombination properties of the cell. The bulk and interface defects are reflected by the capacitance C_d and C_{SS}, respectively

Figure S10 shows an expanded equivalent circuit model separating interface-related capacitance bulk-related capacitance of the PSCs. This model is simplified from a much more complicated strategy that was initially utilized for a metal–insulator–semiconductor structure. [1,2]. In a common equivalent circuit model, charge transfer resistance (R_{sh}) and bulk junction capacitance (C_d) are paralleled element. The bulk defect density (N_b) can be gotten as follow:

$$N_b = -A\frac{\omega C_d(\omega)}{\omega}$$

where ω is the angular frequency and A is the constant related to the PSCs. Besides a widely used paralleled element consisting of R_{sh} and C_d, another capacitance (C_{SS}) is used to reflect the interface defect response in the expanded equivalent circuit model. The R_{SS} is the resistance that a charge needs before being captured by the interface defect.[3] There is a quantitative relationship between C_{SS} and the interface defect density (N_{SS}), that is [4]

$C_{ss}=qSN_{ss}$

where q is the electron charge and S is the device area. The C_{SS} can be gotten from following equation

$$\frac{1}{\omega}\left(G-\frac{1}{R_{sh}}\right)=\frac{\omega R_{ss}C_{ss}^2}{1+(\omega R_{ss}C_{ss})^2}$$

where G is the admittance and ω is the angular frequency. The left term of Equation can be obtained from experimental admittance measurements. The C_{SS} as well as the N_{SS} can then be computed from the admittance spectra.

Reference:

[1] E. H. Nicollian, A. Goetzberger, *Bell Syst. Tech. J.* **1967**, *46*, 1055.

[2] V. V. Brus, *Semicond. Sci. Technol.* **2012**, *27*, 035024.

[3] K. Lehovec, A. Slobodskoy, *Solid-State Electron.* **1964**, *7*, 59.

[4] S. M. Sze, K. N. G. Kwok, *Physics of Semiconductor Devices*, 3rd ed.,Wiley, Hoboken **2007**.