

Supporting Information

The Role of Hybrid Dielectric Interface in Improving the Performance of Multilayer InSe Transistors

Shichao Zhang^{†,§}, *Yunfeng Qiu*^{†,§}, *Huihui Yang*[‡], *Dao Wang*[†], *Yunxia Hu*[‡], *Xubing Lu*[†],
Zhonghua Li^{*†,§}, and *PingAn Hu*^{*†,‡,§}

[†]School of Chemistry and Chemical Engineering, Harbin Institute of Technology,
Harbin, 150001, P. R. China

[‡]School of Materials Science and Engineering, Harbin Institute of Technology, Harbin
150001, P. R. China

[§]Key Laboratory of Micro-systems and Micro-structures Manufacturing of Ministry of
Education, Harbin Institute of Technology, Harbin 150080, P. R. China

[†]Institute for Advanced Materials, South China Academy of Advanced Optoelectronics,
South China Normal University, Guangzhou, 51000, P. R. China

E-mail: hupa@hit.edu.cn, lizh@hit.edu.cn

KEYWORDS: β -InSe, Coulomb scattering, surface optical phonon scattering,
interfacial traps, hybrid dielectric

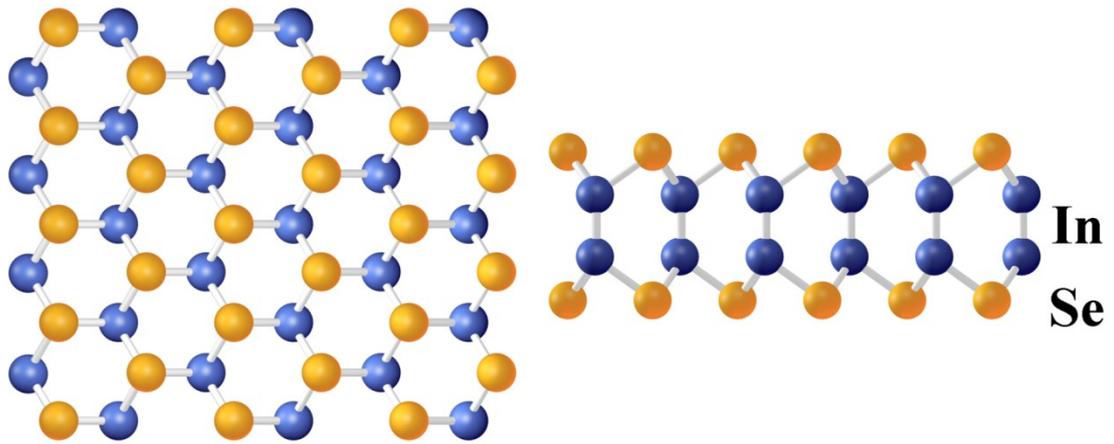


Figure S1. Schematic of β -InSe crystal structure. Left panel shows a top view of the InSe crystal structure and right panel displays a side view

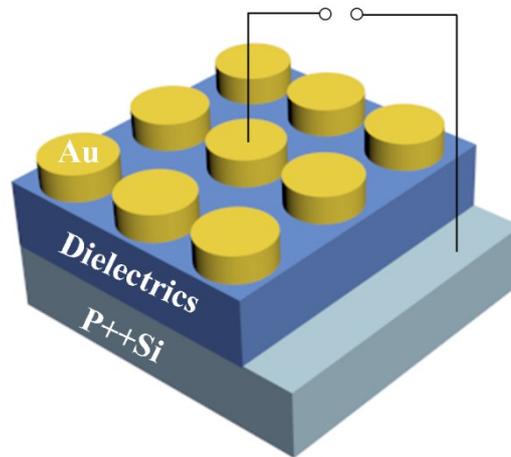


Figure S2. Schematic diagram of a MIM capacitor

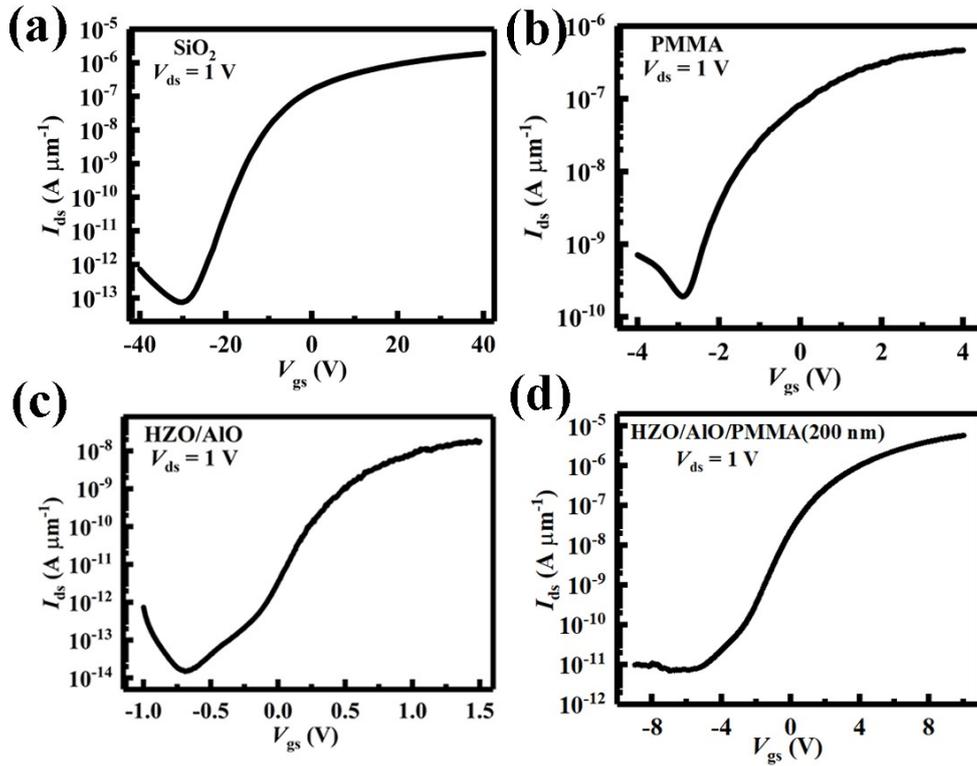


Figure S3. Typical transfer characteristics of InSe transistors using various gate dielectric layers using (a) SiO₂ (300 nm), the channel length and width are 27 μm and 24 μm , respectively, (b) PMMA (200 nm), the channel length and width are 28 μm and 26 μm , respectively, (c) HZO (20 nm)/AIO (4 nm), the channel length and width are 30 μm and 25 μm , respectively, (d) HZO (20 nm)/AIO (4 nm)/PMMA (200 nm) hybrid dielectric device, the channel length and width are 28 μm and 24 μm , respectively.

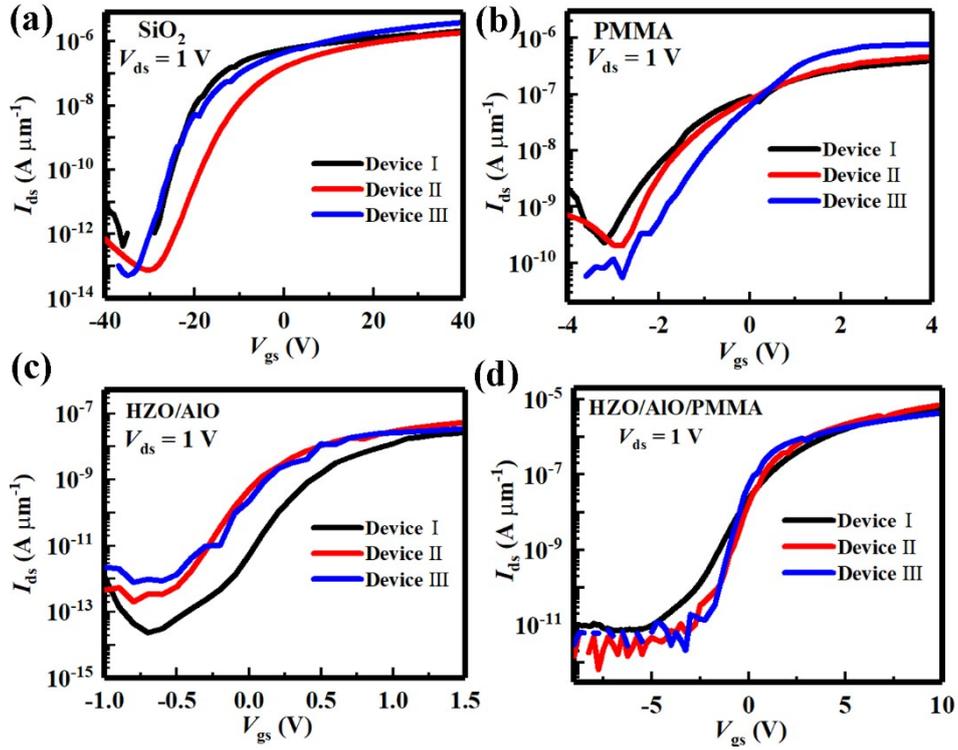


Figure S4. Transfer characteristics of multiple InSe transistors using various gate dielectric layers

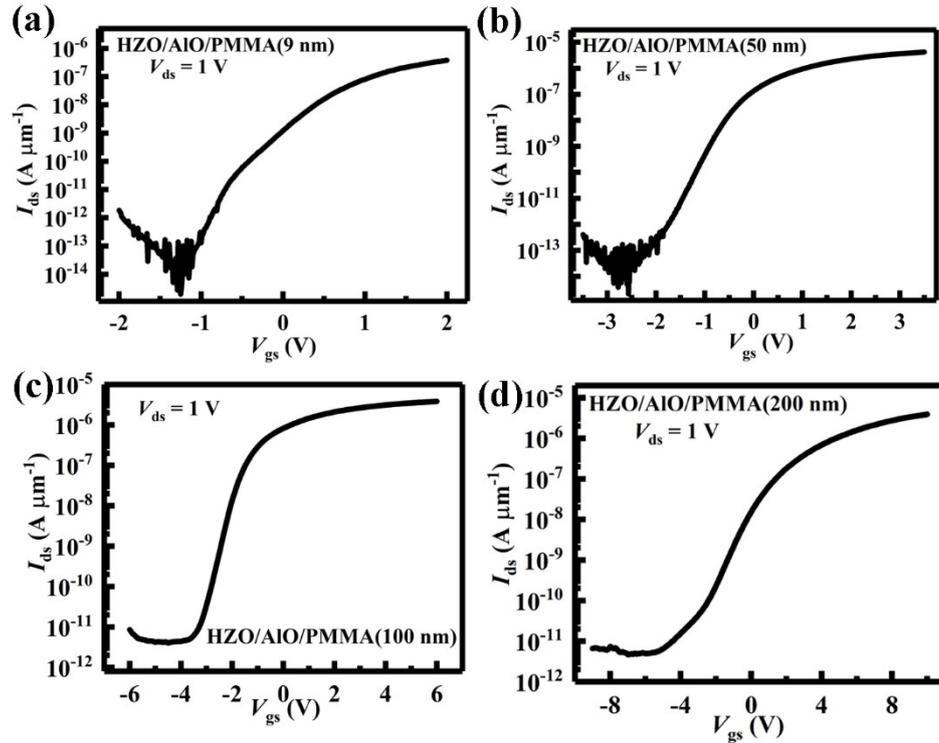


Figure S5. Transfer characteristics of InSe transistors using HZO (20 nm)/AIO (4 nm)/PMMA (9 ~ 200 nm) trilayer device

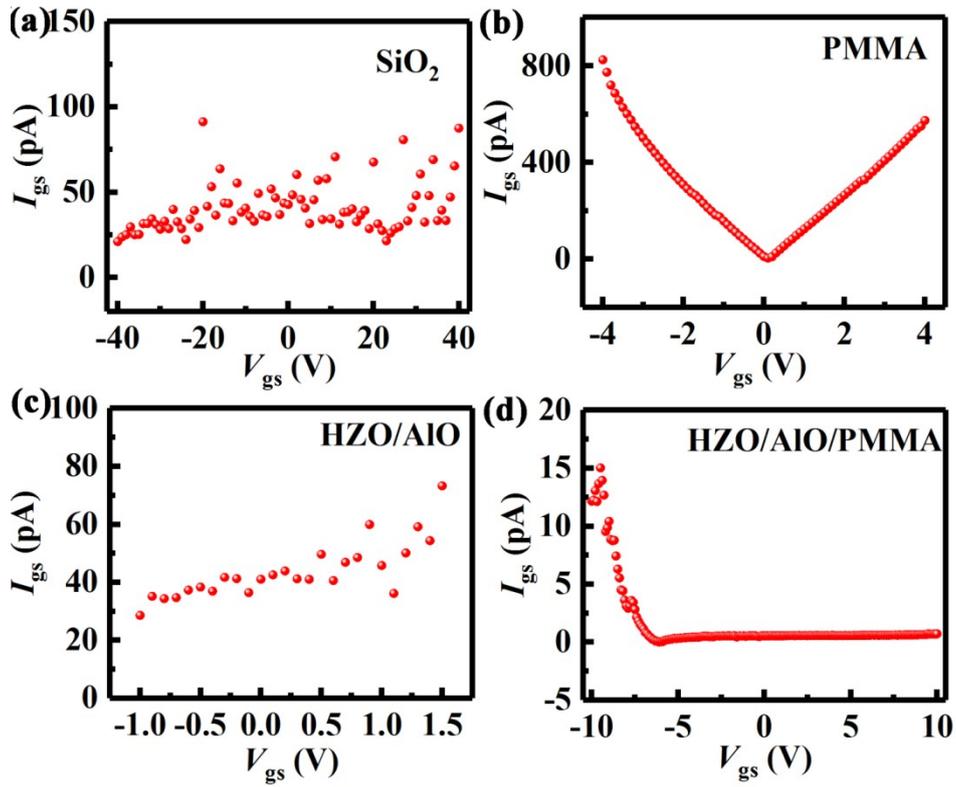


Figure S6. I_{gs} versus V_{gs} of InSe transistors using various gate dielectric layers

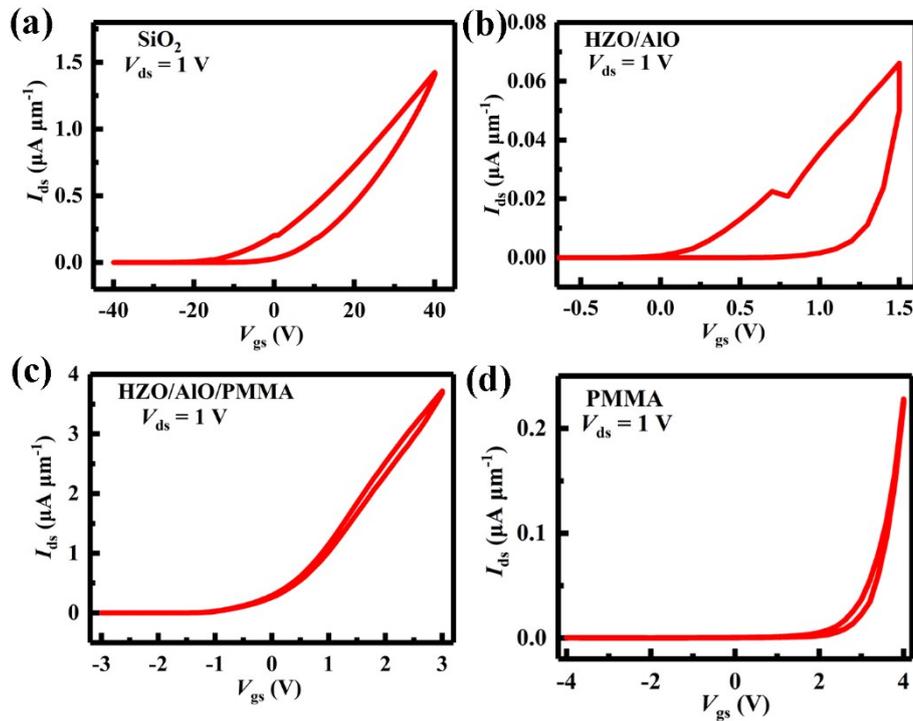


Figure S7. Transfer characteristics of InSe transistors using various gate dielectric layers with forward and backward scans of the gate voltage.

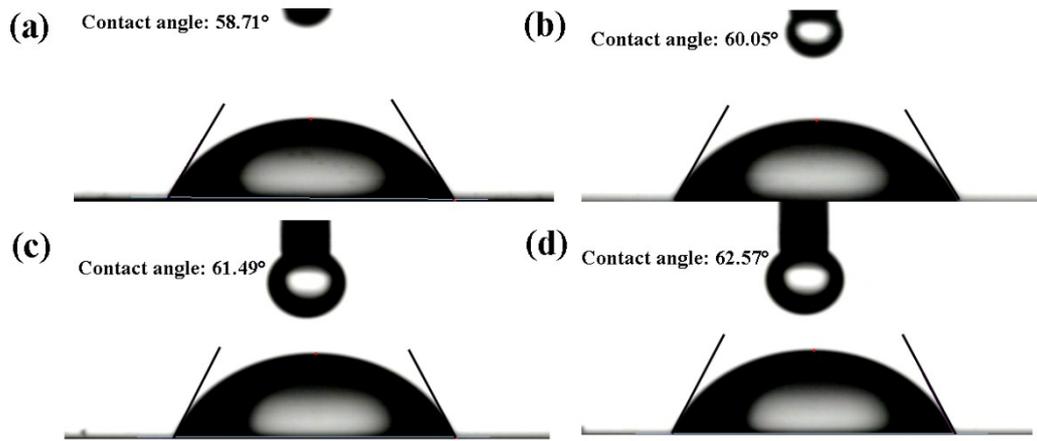


Figure S8. Images of water drops on hybrid dielectric layers for contact angle measurement: (a) HZO/AlO₃/PMMA (20 nm/4 nm/9 nm), (b) HZO/AlO₃/PMMA (20 nm/4 nm/50 nm), (c) HZO/AlO₃/PMMA (20 nm/4 nm/100 nm), (d) HZO/AlO₃/PMMA (20 nm/4 nm/200 nm).