

## *Supporting Information*

### **Memristors Mimicking the Regulation of Synaptic Plasticity and the Refractory Period in Phenomenological Model**

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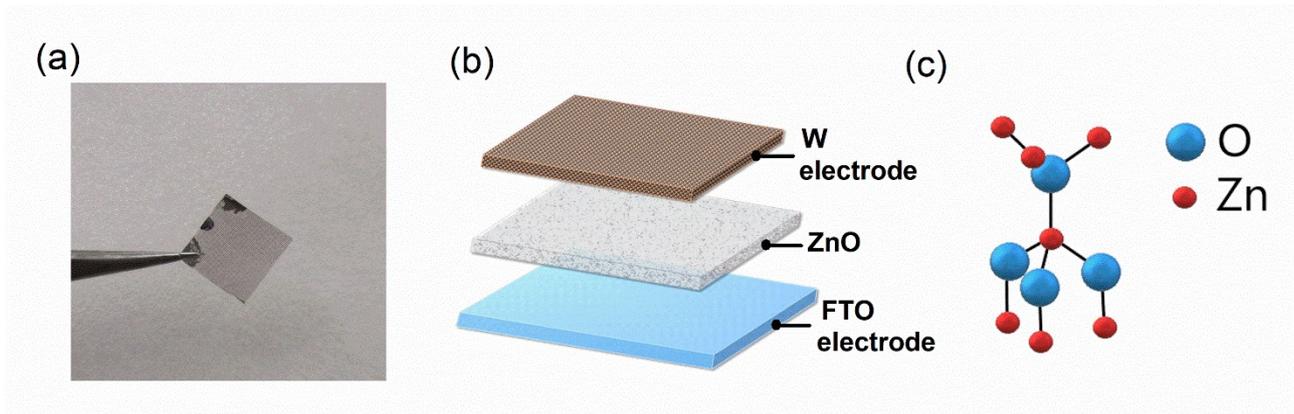
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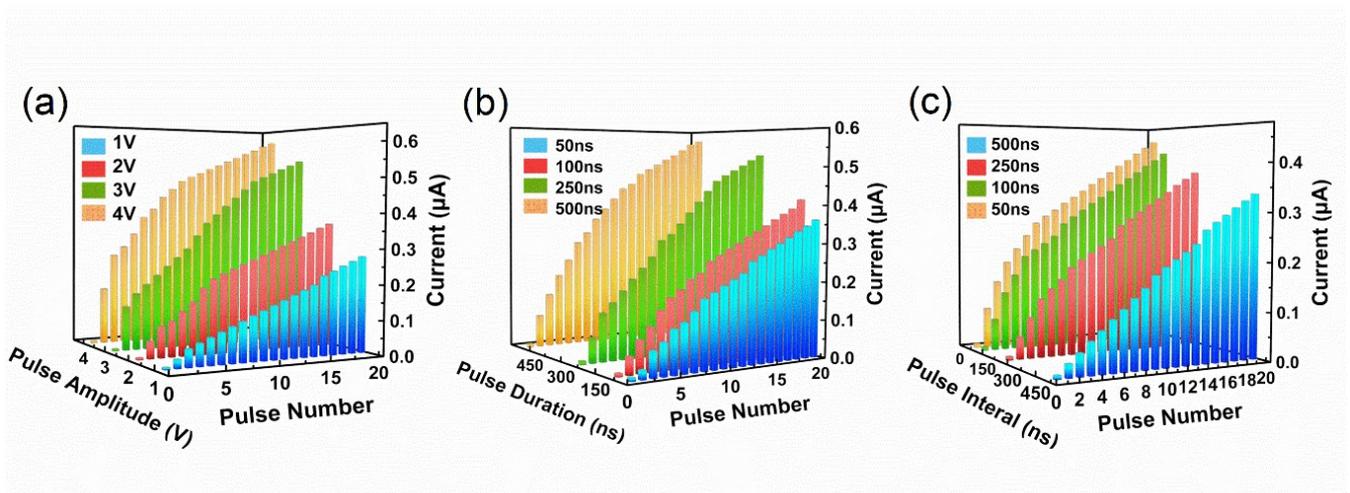
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**Figure S1.** The modeling of the memristor. **a,b)** The image of W/ZnO/FTO devices and schematic structure. **c)** A solid sphere model of ZnO in wurtzite structure.

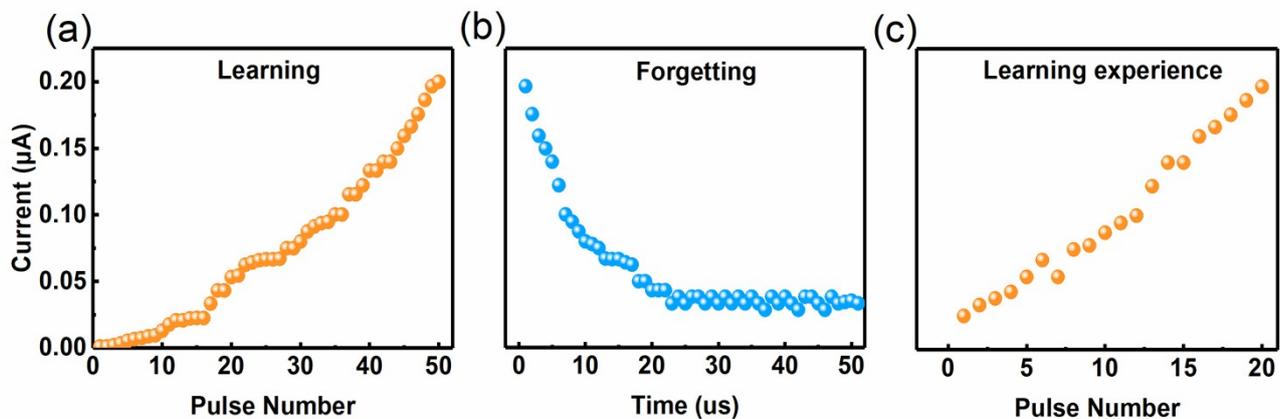
A schematic memristor device configuration is depicted in Figure S1. The basic RRAM structure should consist of two opposing electrodes and a memory material, as shown in Figure S1b. For fabrication, FTO was used as a substrate. The device has a tungsten (W) top electrode, a zinc oxide (ZnO) switching layer, and a fluorine-doped tin oxide (FTO) bottom electrode. The 3-D schematic illustrations matched with the atomic image: the ZnO in a wurtzite structure.



**Figure S2.** Unidirectional pulse train for exciting the synapse with different parameters. **a,b,c)** Impact of positive pulse train amplitude/duration/interval on the conductance modulation.

Synergistic effects of presynaptic and postsynaptic synapses can affect synaptic body weight. Changing the amount of change in synaptic weight by using electrical pulses of different amplitudes, pulse durations, pulse interval and pulse numbers to change the effective flux determined by the spike parameters. We further studied the effect of different pulse parameters on the variation of the counterpart wave peak on the device.

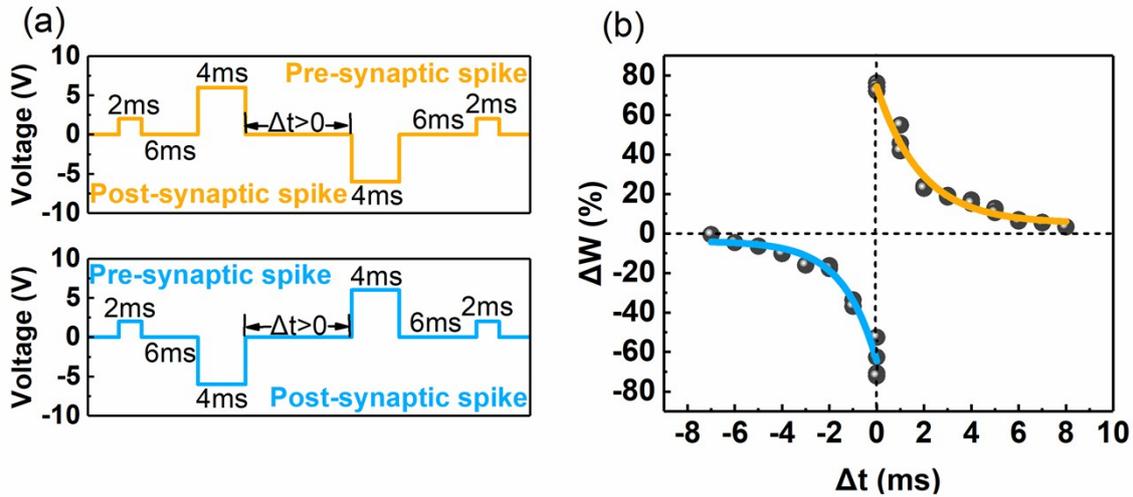
As the spikes in the pulse sequence continue to act on our memristive devices, we first investigated the effects of adjusting the amplitude, pulse duration, and spacing of the pulse train with positive polarity on conduction changes. Figure S2a shows the relationship between device current and pulse amplitude, with 20 pulses applied to the device. The pulse duration and interval are fixed at 100ns. To determine the successful modulation of conduction in the device, the dependence of the device current on the positive pulse amplitude is shown in Figure S2a. The current changes rapidly as the pulse amplitude increases. Next, Figure S2b shows the device current vs. pulse duration, with pulse amplitude and spacing fixed at 5V and 100ns. The dependence of the device current on the pulse duration is shown in Figure S2b. The conduction of the device changes rapidly with the increase of the pulse durations for both potentiating processes. Finally, Figure S2c shows the relationship between device current and pulse interval. Pulse amplitude and duration are fixed at 5V and 100ns. The dependence of the device conductance on the pulse interval is shown in Figure S2c. The increase in pulse spacing results in less conduction changes in the enhancement and suppression processes. These results confirm that successfully pass device adjusted by nanosecond pulses of different parameters, and all of the current memristor eventually reaches saturation. The conduction value in the saturated state increases as the pulse amplitude and duration increase or the pulse interval decreases.



**Figure S3.** The “learning-experience” behaviors, and the dynamic model of device operation. **a)** Nearly linear increase of the synaptic weight with consecutive stimuli. **b)** The spontaneous decay of the conductivity, that is, which is very similar to the human-memory “forgetting curve”. **c)** Re-stimulation process from the mid-state. The pulses, far fewer than the number of stimuli required in the first learning process, can make the device recover its memory, which bears striking resemblance to the learning process based on experience for biological systems.

Figure S3a shows the results of a test in which the synaptic device was stimulated sequentially with 50

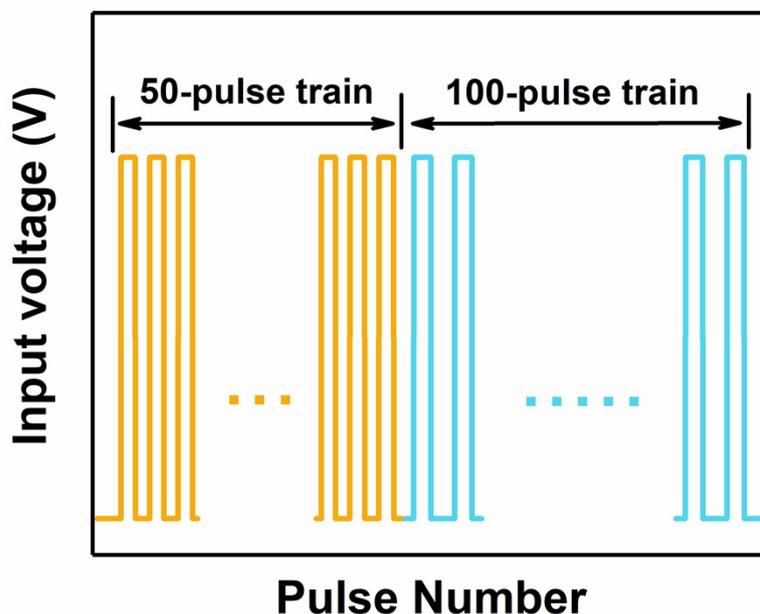
positive pulses; the synaptic weight is gradually increased with the number of pulses. It is worth noting that when the applied voltage is removed, a spontaneous decay of synaptic weight occurs in the case of no external inputs (Figure S3b). The decay rate is very fast at the initial stage and then gradually slows down. This trend is consistent with the human-memory “forgetting (or retention) curve” in psychology.



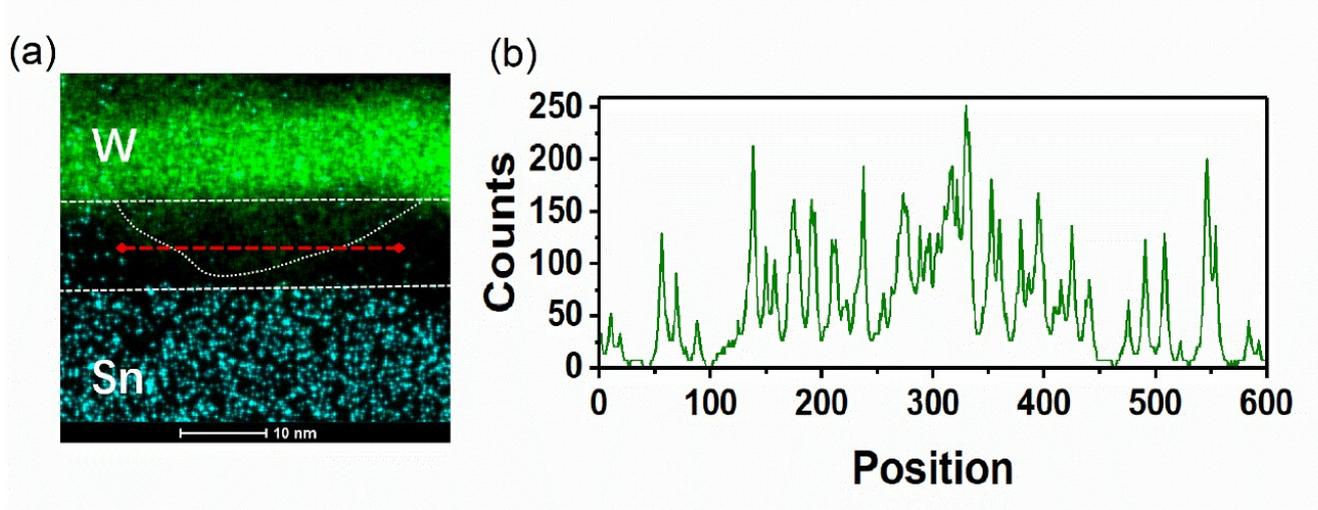
**Figure S4.** Demonstration of spike-timing-dependent plasticity (STDP) in the memristor synapse. **a)** In order to implement STDP, a pair of pre- and postsynaptic spikes were designed. **b)** The variation of the memristor synaptic weight ( $\Delta W$ ) with the relative spike timing ( $\Delta t$ ). The solid lines show the exponential fitting result of the experimental data.

The temporal sequence of presynaptic and postsynaptic spikes determines the polarity of synaptic weight changes. The observed spike-rate-dependent characteristic is similar to the STDP rule of biological synapses. To implement STDP, a pair of pulses with amplitude  $V^+ / V^- = 6 \text{ V} / -6 \text{ V}$  are applied to the top and bottom electrodes as the pre- and postsynaptic spikes, as illustrated in Figure S4 a, b. The relative timing  $\Delta t < 0$  ( $\Delta t > 0$ ) is defined as the interval from the end of the presynaptic (postsynaptic) spike to the beginning of the postsynaptic (presynaptic) spike. The postsynaptic currents were measured before (I1) and after (I2) the spike-pair application. The postsynaptic currents were measured before (I1) and after (I2) the spike-pair application. Figure S6b shows the variation of  $\Delta W$  with  $\Delta t$ . We can see that (1) when the presynaptic neuron spikes before (after) the postsynaptic neuron, the synaptic weight increases (decreases); (2) the smaller the time interval  $\Delta t$ , the larger the absolute value of  $\Delta W$ ; and, (3) the experimental data can be well fitted to an exponential function. These are typical STDP characteristics of biological synapses. In fact, the temporal

characteristic is identical between spike-rate dependent plasticity and STDP behaviors, and frequent stimulation can increase the synaptic weight.



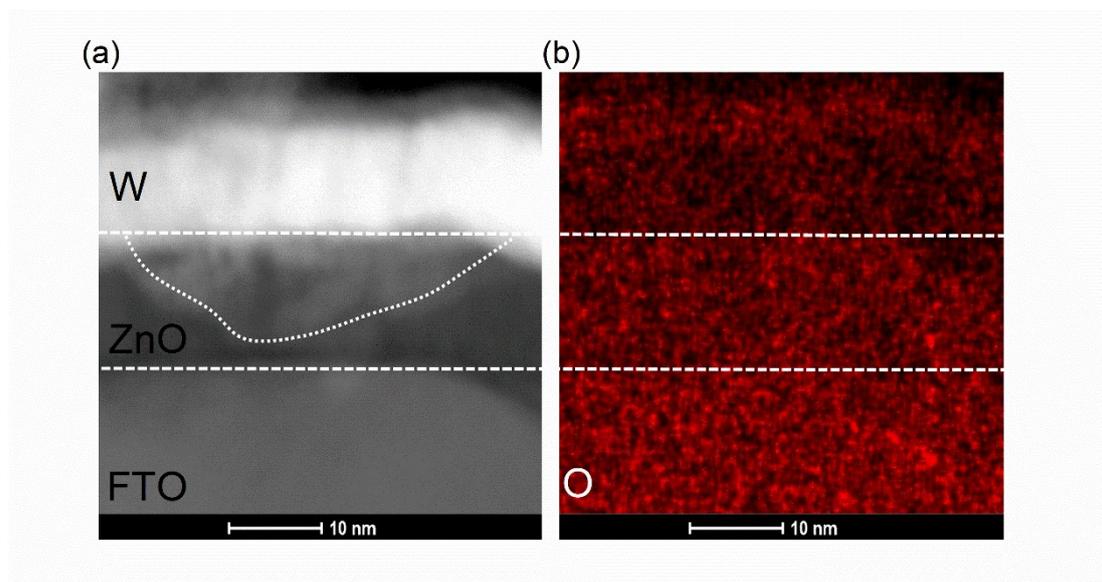
**Figure S5.** Schematic diagram of two different pulse sequences applied to the device.



**Figure S6.a)** The elemental mapping images of W and Sn. **b)** The line scan parts of elements W filaments corresponding to (a).

To further corroborate the formation of W protrusion-like region structure, Figure S6a shows the EDS elemental analysis of the W/ZnO/FTO memristor. It is obvious found that the conductive protrusion-like region between top and bottom electrodes across the ZnO layer are clearly observed in STEM. Moreover, the

W protrusion-like region structure is confirmed by the line scan profiles shown in Figure S6b.



**Figure S7.**The elemental mapping images of O.

Figure S7b shows the elemental mappings of O, which corresponds to the results shown in Figure S7a. We found that the oxygen atoms were evenly distributed in the ZnO layer with no oxygen vacancies between the two electrodes, as shown in Figure S7b. Therefore, we believe that the mechanisms of the device does not support the migration of O vacancies.