# Electronic Supplementary Information (ESI)

# Nanoscale surface engineering of a high-*k* $ZrO_2/SiO_2$ gate insulator for high performance ITZO TFT via plasma-enhanced atomic layer deposition

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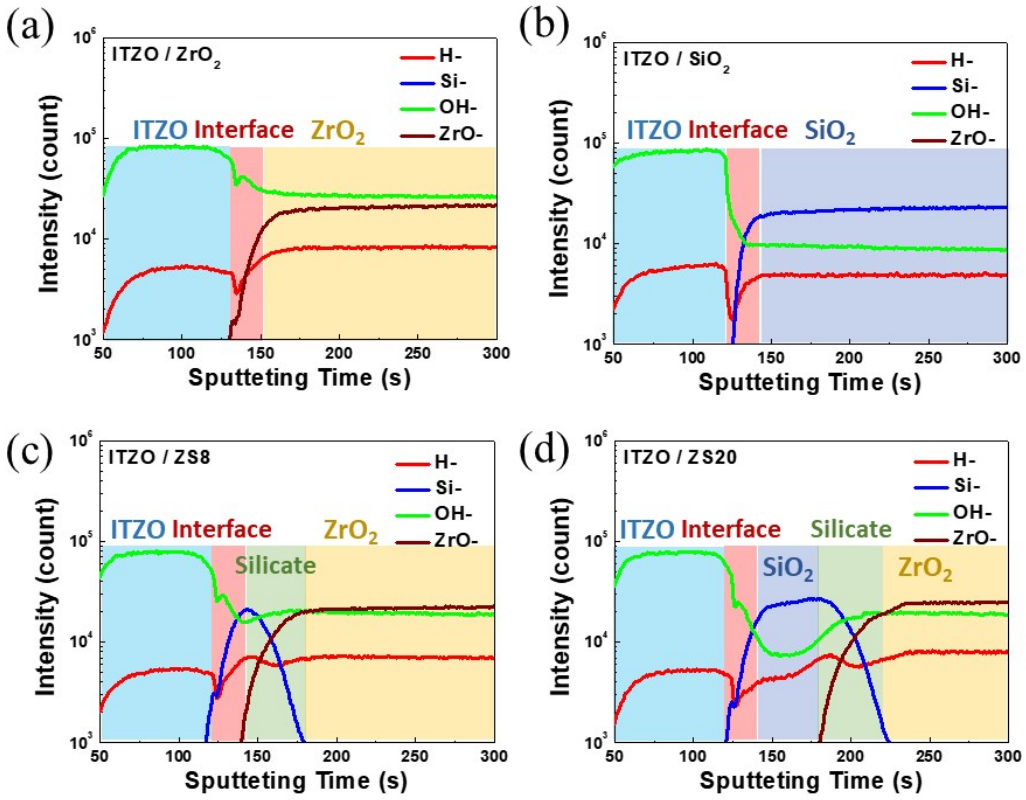


**Figure S1.** SIMS depth profile of TFT structure with (a)$ZrO_2$, (b)$SiO_2$, (c)ZS8 and (d)ZS20.