Supporting Information

Partial substitution of CdS buffer layer with interplay of fullerenes in kesterite solar cells

David Payno[a], Yudania Sánchez[c], Oriol Blázquez[c], Sergio Giraldo[c], Manuel Salado[a], Samrana Kazim[a,b], Edgardo Saucedo [c,d] and Shahzada Ahmad[a,b]

[a]BCMaterials, Basque Center for Materials, Applications and Nanostructures, Bld. Martina Casiano, UPV/EHU Science Park, Barrio Sarriena s/n, 48940 Leioa, Spain
Email:shahzada.ahmad@bcmaterials.net
[b]IKERBASQUE, Basque Foundation for Science, Bilbao, 48013, Spain
[c]Catalonia Institute for Energy Research (IREC), Jardin de les Dones de Negre 1, 08930 Sant Adrià de Besòs, Barcelona, Spain
[d]Department of Electronic Engineering, Polytechnic University of Catalonia (UPC), Sor Eulàlia d'Anzizu 6, 08034 Barcelona, Spain

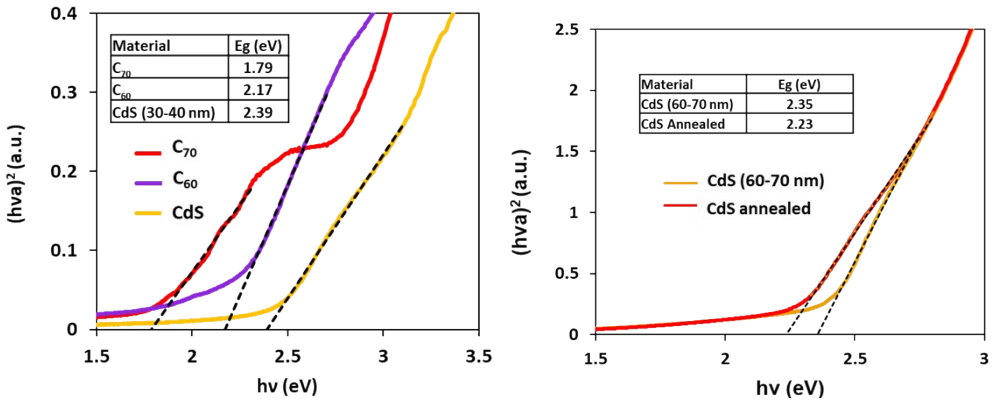

Figure S1*:* Tauc plot and band-gaps derived from the absorption spectra for a) C_{60}, C_{70} and 30-40nm of CdS and b) for CdS (60-70nm) before and after annealing in air at 230 °C for 20mins.

Influence of post annealing treatment in CZTSe based solar cells:

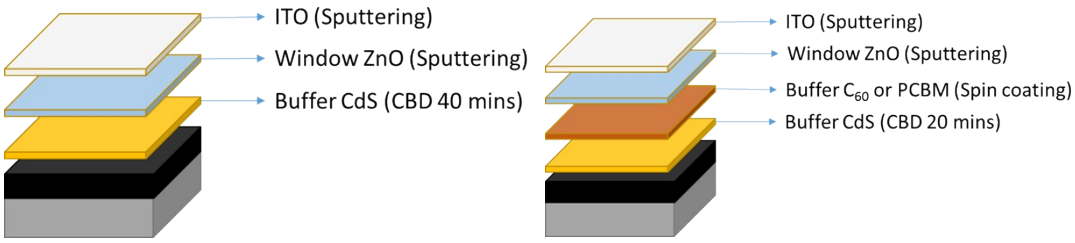

Figure S2. Schematic of the fabricated devices with CZTSe as absorber layer.

Devices were fabricated with the standard composition of CZTSe. The reference device has a standard CdS deposition (chemical bath deposition, produces 60nm-70nm thickness). The effects of C_{60} and PCBM where explored by dividing the buffer layer in two parts, a first one of 30nm of CdS, followed by a second one of 30nm C_{60} or PCBM, following the scheme of the *Fig.S2*. Devices with only C_{60} or PCBM where also fabricated to explore its influence as buffer layer.

For this, the final devices were characterized and subject to successive post heat treatment, at 200, 225 and 250 °C for 20 minutes on a hot plate. The results are showed in the *Table S1*, where a similar trend can be noted in all the

devices. In all the cases, they present an increase in the V_{oc} at higher temperatures treatments. The optimized efficiency was noted at 225°C, where the fill factor is maximum. This effect is less pronounced in the case of PCBM, probably due to its lower stability under high temperatures. Treatment at higher temperature starts to degrade the current and the fill factor, resulting in a lower power conversion efficiency. In the case of using only C_{60} or PCBM, the optimized condition was found at 200 °C. We speculate that this is due to a better redistribution of Na in the absorber, rather than changes in the interface or in the buffer material. Samples that only use 30nm of C_{60} or PCBM show a reduction in photovoltaics parameters. In all like hood insufficient thickness or un-aligned band energy can be responsible of this. With further optimization of the process and the use of appropriate charge selective contact as buffer layer can push the performance.

The current-voltage of the best cells are represented in the *Figure S3a.* The device statistics suggests that the partial substitution of the CdS can be an attractive option. The spectra response where measured by external quantum efficiency (EQE) in the *Figure S3b*. Both the samples with C_{60} and PCBM exhibits similar PCE, however devices based on C_{60} was found to have a higher voltage after the heat treatment.

Table S1: Devices parameters using CZTSe as absorber, extracted from J-V characterization under 1 sun ilumination (average values over 8 cells).

Condition	Post Heat Treatment (°C)	J_{sc} (mA/cm²)	V_{oc} (mV)	FF (%)	PCE (%)
Reference CdS 40 min	As prepared	22.87	321.29	42.71	3.21
	200	27.17	366.38	53.22	5.49
	225	**25,35**	**422,99**	**65,82**	**7.08**
	250	23.84	451.03	60.89	6.55
CdS/PCBM	As prepared	22.79	399.07	52.71	4.80
	200	25.85	396.49	64.27	6.59
	225	**24.97**	**409.29**	**69.39**	**7.09**
	250	24.28	411.55	59.63	5.99
CdS/C_{60}	As prepared	23.83	400.32	54.66	5.20
	200	26.62	406.09	65.50	7.03
	225	**24.49**	**423.15**	**67.83**	**7.03**
	250	23.52	440.89	61.20	6.35
PCBM	As prepared	0.10	112.34	24.60	0.00
	200	**9.98**	**164.95**	**20.62**	**0.34**
	225	7.68	143.43	20.09	0.22
	250	4.19	141.90	15.14	0.09
C_{60}	As prepared	0.13	54.38	28.79	0.00
	200	**14.21**	**194.13**	**26.96**	**0.74**
	225	8.68	142.06	28.75	0.35
	250	7.44	113.08	30.67	0.26

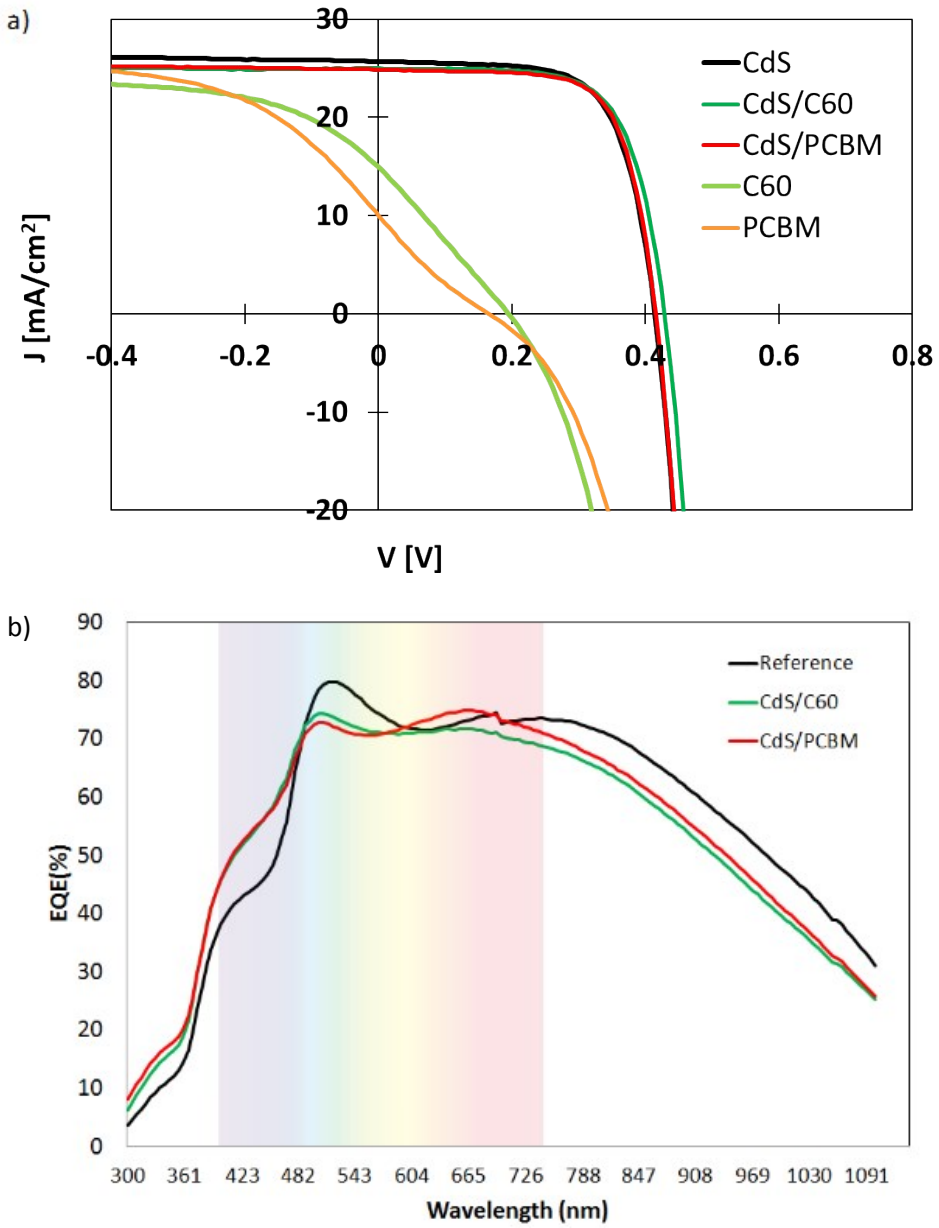

Figure S3: **a)** Current-Voltage (*J-V*) characteristic of and b) external quantum efficiency spectra of the fabricated devices.

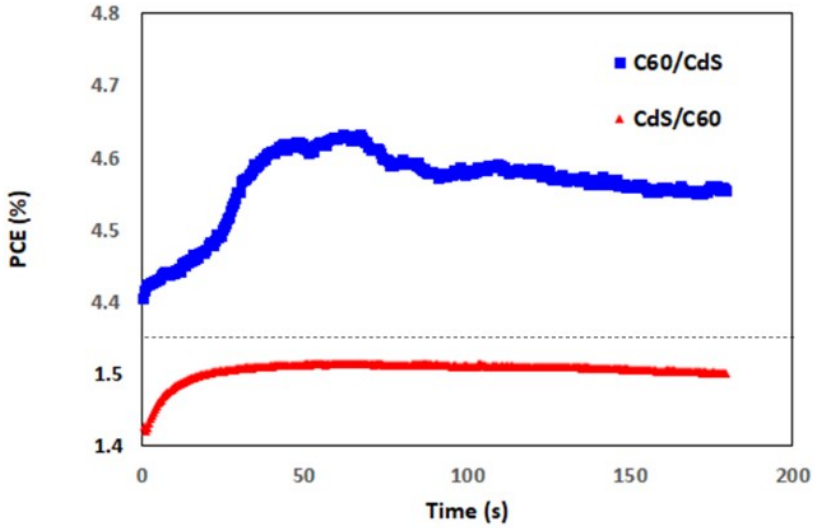

***Figure S4**:* Power conversion efficiencies evolution with time under 1 sun for the CZTS/C_{60}/CdS and CZTS/CdS/C_{60} samples. Maximum power point was tracked every 0.5 s.