Electronic Supplementary Information

Unusual Phase-Pure Zinc blende and Highly-Crystalline As-rich $InAs_{1-x}Sb_x$ Nanowires for High-Mobility Transistors

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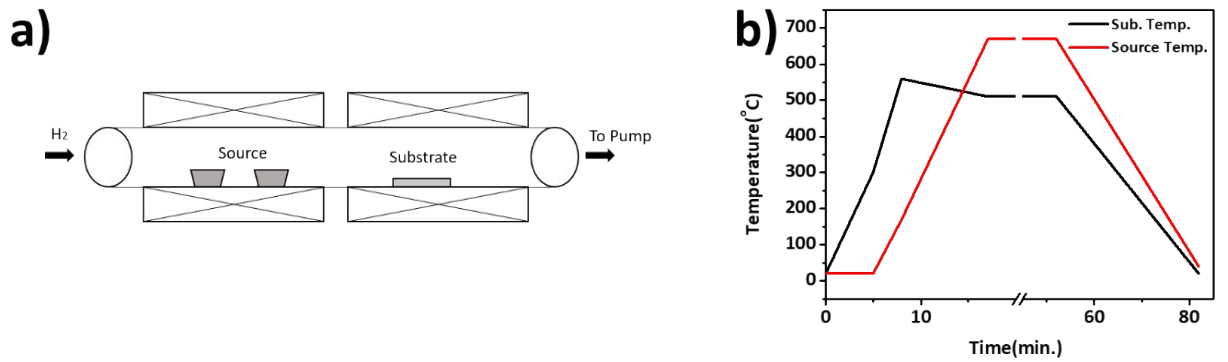

Figure S1. Experimental setup: (a) configuration of the chemical vapor deposition system and (b) temperature profiles of the source zone and substrate zone.

The experimental steps are listed in the main text of the manuscript. In specific, the two boron nitride crucibles are placed in the source zone with the distance of 6 cm and 9 cm away from the middle of the center isolation (i.e. the center positon between the two zones), while the substrate is positioned in the substrate zone 4 cm away from the center isolation. The reason of using two crucibles is to keep the source vapor flow for a longer duration. The position of the substrate is also important as the nanowires nucleate only when the substrate is close enough to the center isolation.

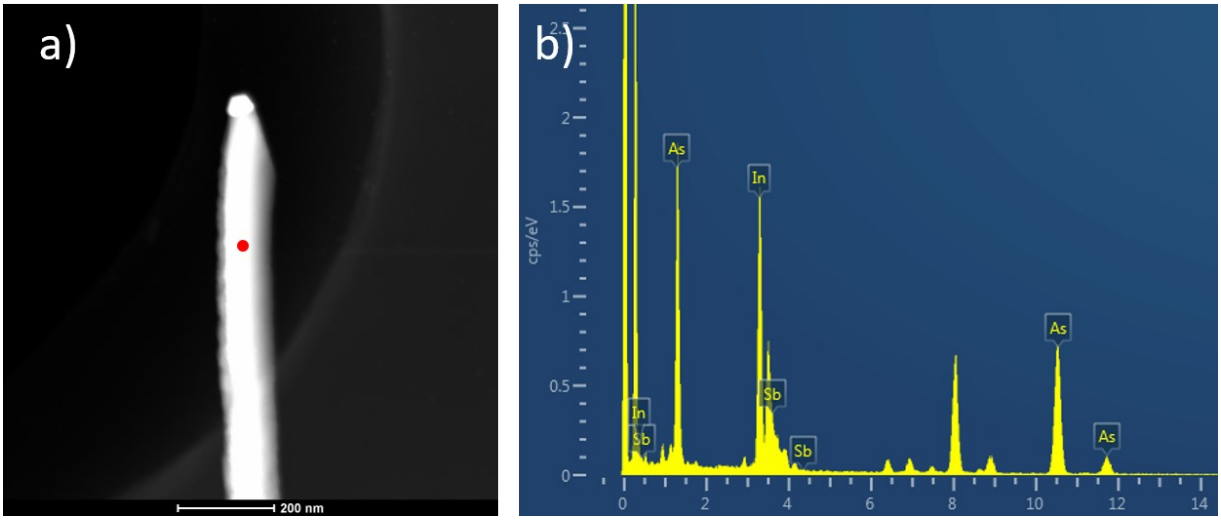

Figure S2. (a) The STEM HADAF image of a typical $InAs_{0.908}Sb_{0.092}$ NW and (b) its corresponding energy dispersive X-ray spectroscopy spectrum taken at the red dot shown in the panel a.

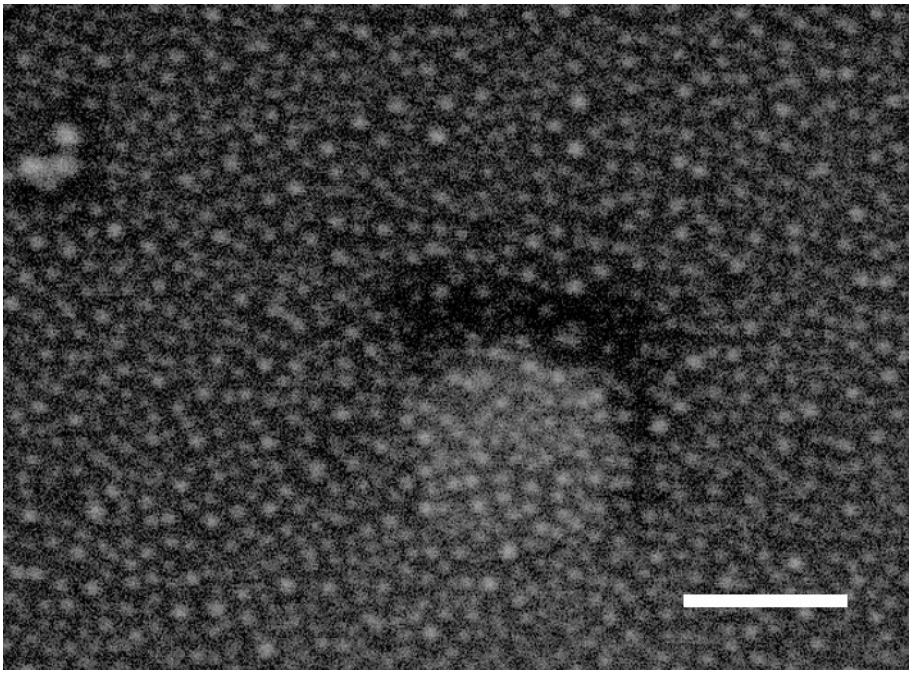

Figure S3. SEM image of the Au catalytic particles formed by annealing the 0.5-nm-thick Au layer without supplying precursor source. Scale bar is 100 nm.

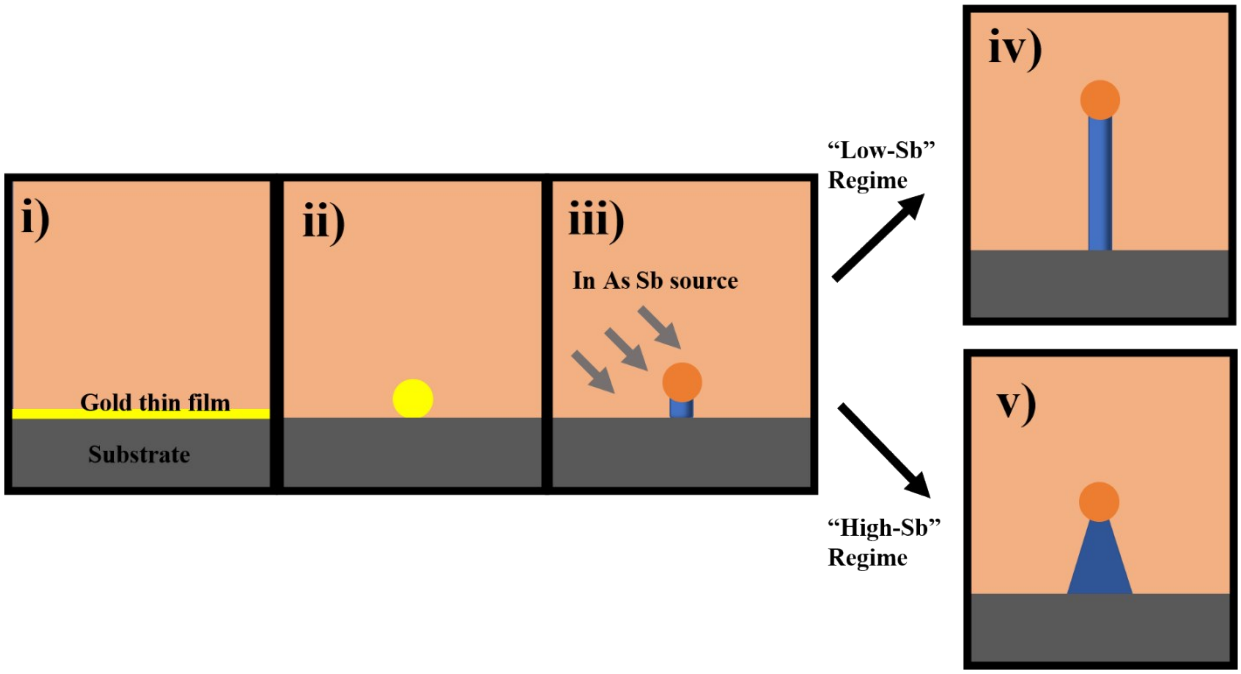

Figure S4. Schematic description of the growth process of $InAs_{1-x}Sb_x$ NWs at different stages. They are (i) initial stage, (ii) gold nanoparticle formation, (iii) NWs nucleation and NWs grown under (iv) "low-Sb" regime and (v) "high-Sb" regime. The drawing is not in scale.

Proposed growth mechanism of $InAs_{1-x}Sb_x$ NWs: The growth of $InAs_{1-x}Sb_x$ NWs is divided in several stages. At first, as shown in step i, the gold film with 0.5 nm nominal thickness is deposited on the SiO_2/Si substrate. Followed by the annealing process in step ii, the high density of gold nanoparticles are formed. These nanoparticles are experimentally witnessed as shown in Fig. S3. During the NW growth, as the powder source is heated up, the elemental In, Sb and As are released and carried to the downstream by the carrier gas. When these precursor vapors meet the Au nanoparticles, the vapors would get absorbed into the nanoparticles to form alloy nanoparticles. Once the supersaturation is reached, the NWs are then nucleated at the nanoparticle/substrate interface as depicted in step iii. It is evident that the catalytic tips are existed in the hemispherical shape, which contains the composition of Au, In and Sb (Figure 3 in the main text). The presence of these hemispherical catalytic tips suggests that the $InAs_{1-x}Sb_x$ NWs follow the vapor-liquid-

solid (VLS) growth mechanism here. Although a very small amount of As vapor may also get absorbed and diffused into the catalyst tip, the incorporation amount of As in the tip is insignificant. Notably, the obtained morphology of NWs is highly dependent on the concentration of Sb in the reaction reservoir. Under "low-Sb" regime, such as using the precursor powder weight ratio of InAs : InSb = 30:1 and 20:1 (Figure 1b and c in the main text), the obtained NWs are smooth and long as illustrated in step iv. In contrast, the obtained NWs are short and tapered when then are grown under "high-Sb" regime in step v, such as using the precursor powder weight ratio of InAs : InSb = 1:1 and 1:4 (Figure 1e and f in the main text). According to the EDS mapping (Figure 3 in the main text), the composition of the NWs is uniform along the NW length.

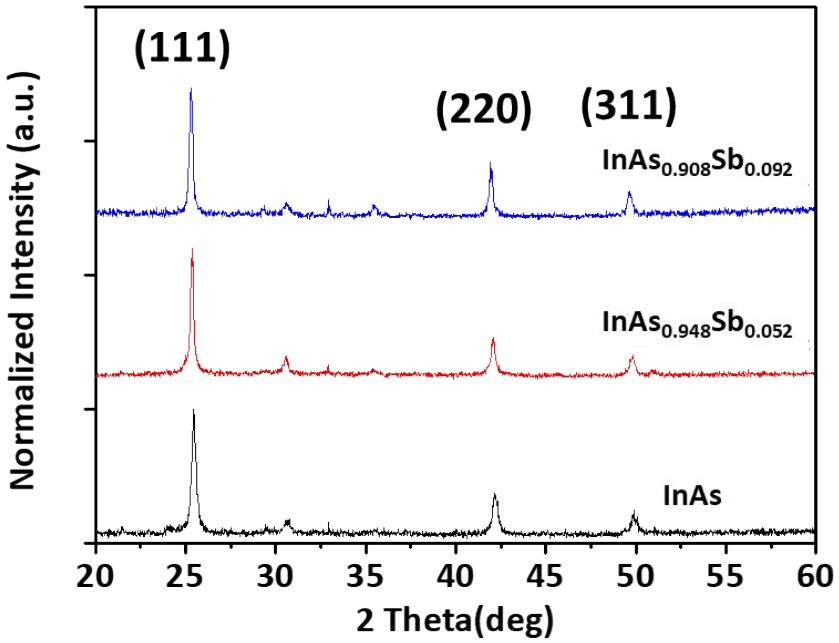

Figure S5. XRD spectra of the InAs, $InAs_{0.948}Sb_{0.052}$ and $InAs_{0.908}Sb_{0.092}$ NWs.

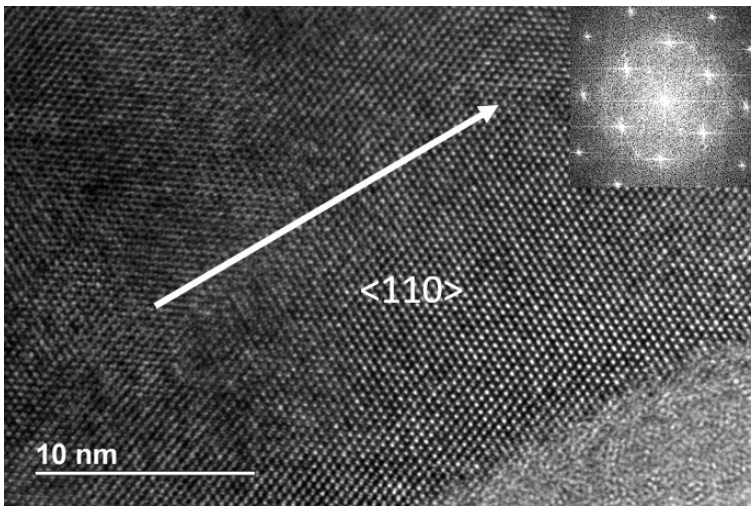

Figure S6. HRTEM image of a typical $InAs_{0.948}Sb_{0.052}$ NW grown in the <110> direction. The inset shows the corresponding FFT pattern of the NW.

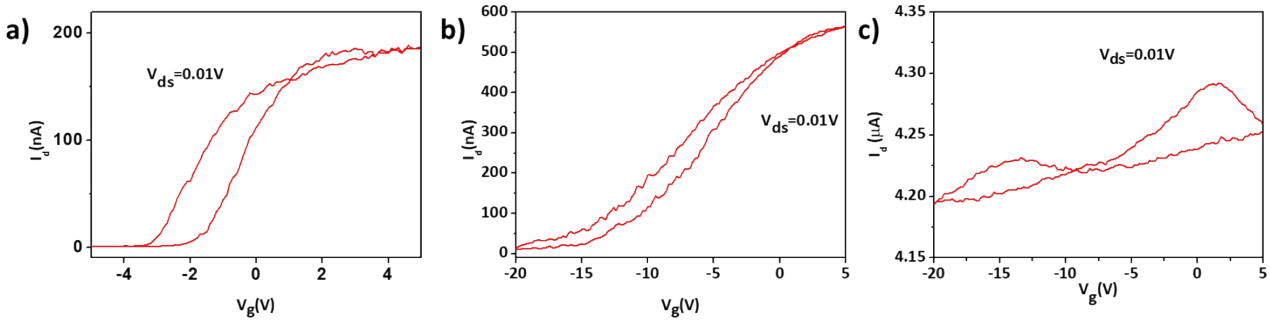

Figure S7. Transfer characteristics of the typical (a) $InAs_{0.964}Sb_{0.036}$, (b) $InAs_{0.92}Sb_{0.08}$ and (c) $InAs_{0.908}Sb_{0.092}$ NWFETs.

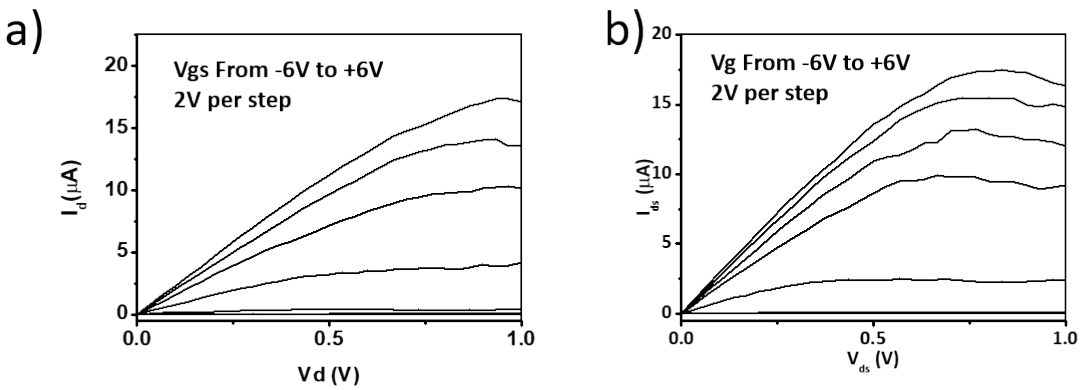

Figure S8. Output characteristics of the typical (a) InAs NWFET and (b) $InAs_{0.948}Sb_{0.052}$ NWFET.

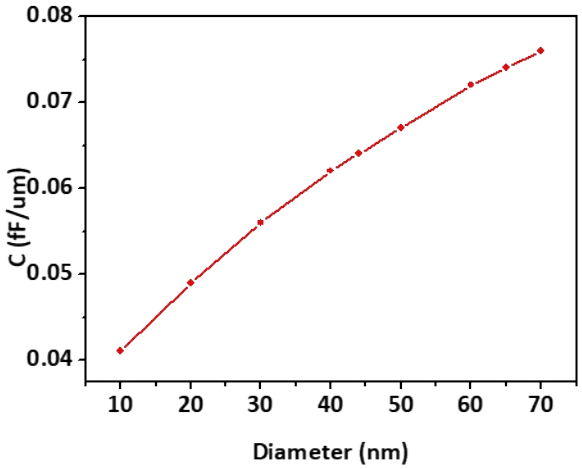

Figure S9. Gate capacitance per unit length as a function of the nanowire diameter.

The gate capacitance per unit length of nanowire is estimated by finite element method using COMSOL Multiphysics. Here, the NW is treated as a metal cylinder lies on a layer of a 50nm thick silicon oxide. The dielectric constant of silicon oxide is taken as 3.9. The calculated result is shown in Fig. S9.

Table S1. The change of the transconductance (g_m) of different $InAs_{0.948}Sb_{0.052}$ NWFETs measured in air and in vacuum.

Sample number	g_m in air (nS)	g_m in vacuum (nS)	$\Delta g_m/g_{m,\ air}$ (%)
1	141	100	29%
2	109	75.1	31%
3	96.4	88.9	8%
4	111	83.8	25%
5	115	54.5	53%
6	117	72.7	38%
7	53.3	41.1	23%