Supplementary information for

Anisotropic ionic transport-controlled synaptic weight update by protonation in VO_2 transistor

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Figure S1

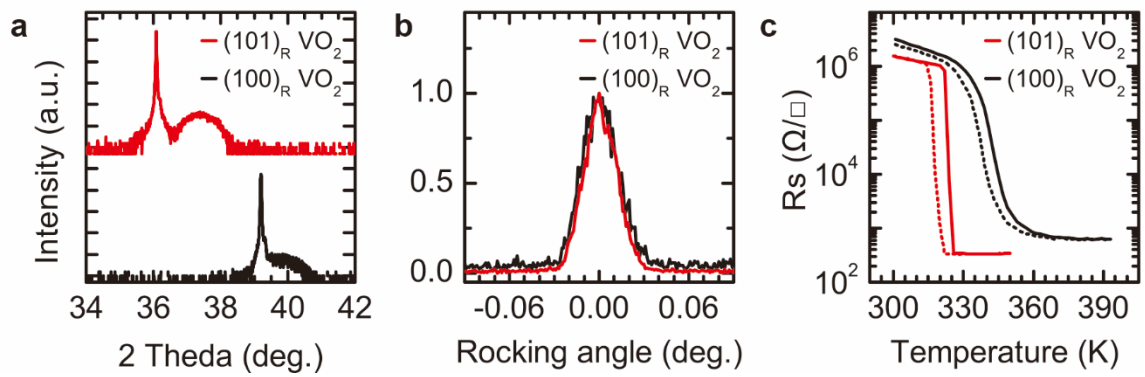


Figure S1 | Epitaxial growth of $(101)_R$ and $(100)_R$ VO_2 thin films. a. Structural analysis of epitaxial $(101)_R$ and $(100)_R$ VO_2 films on (101) and (100) TiO_2 substrates. **b.** The rocking curves of both VO_2 diffraction peaks were shown, and they show similar FWHM value as 0.025°. **c.** Sheet resistance (R_S) – Temperature (K) measurements from 300 K to 395 K during heating and cooling process of both VO_2 films. They show similar R_S change during their intrinsic metal-insulator transition (MIT) phenomena.

Figure S2

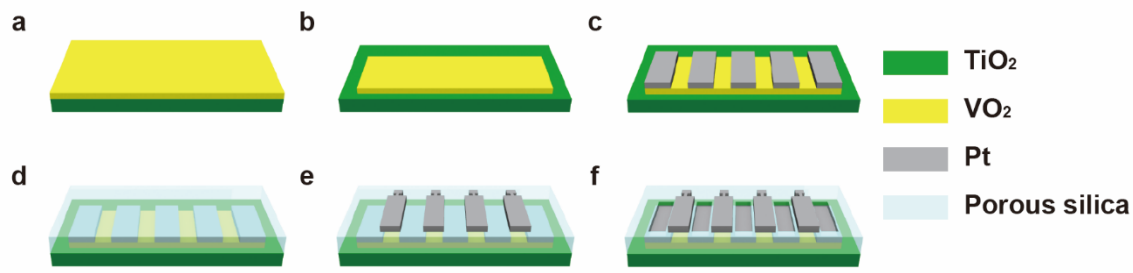


Figure S2 | Device fabrication process. a. Epitaxial 10-nm-thick $(101)_R$ and $(100)_R$ VO_2 thin films were prepared by PLD methods. **b.** VO_2 channel were defined by photolithography followed by wet HNO_3 etching process. **c.** 30-nm-thick Pt source and drain electrodes were deposited by RF sputtering. **d.** 300-nm-thick porous silica layer were spin-coated followed by curing process. **e.** 30-nm-thick Pt gate electrode were deposited by RF sputtering. **f.** The porous silica layer on the area of source and drain electrode were wet etched with oxide etchant for contact.

Figure S3

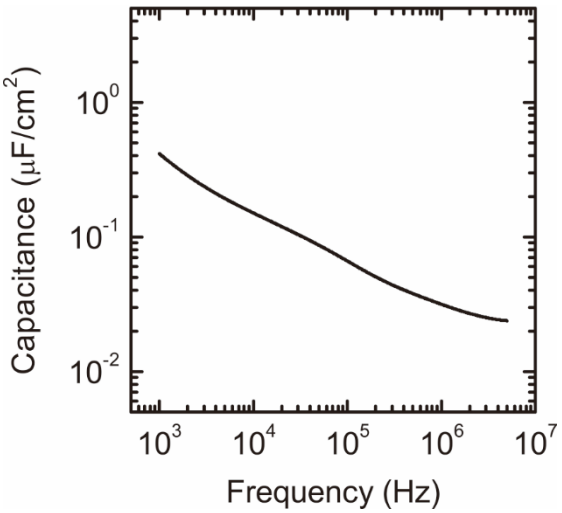


Figure S3 | Specific capacitance as a function of frequencies. The frequency-dependent capacitance measurements (*C*-*f*, 1 kHz ≤ *f* ≤ 5 MHz) were performed on the Pt (gate)/electrolyte/VO_2 stack. the specific capacitance decreased with *f* (~ 0.4 μF/cm^2 at 1 kHz → ~ 0.02 μF/cm^2 at 5 MHz) due to the slow response of mobile protons in porous silica with respect to high-*f* V_G.

Figure S4

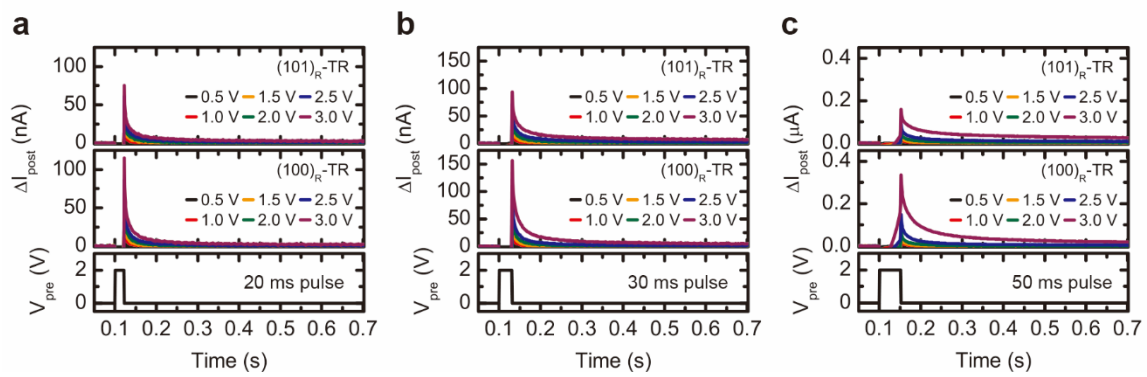


Figure S4 | Excitatory postsynaptic current (EPSC) triggered by D_P (= 20, 30, and 50 ms) of V_{pre} pulse as a function of A_P of V_{pre} in $(101)_R$ and $(100)_R$-VO_2 synaptic transistors.

Figure S5

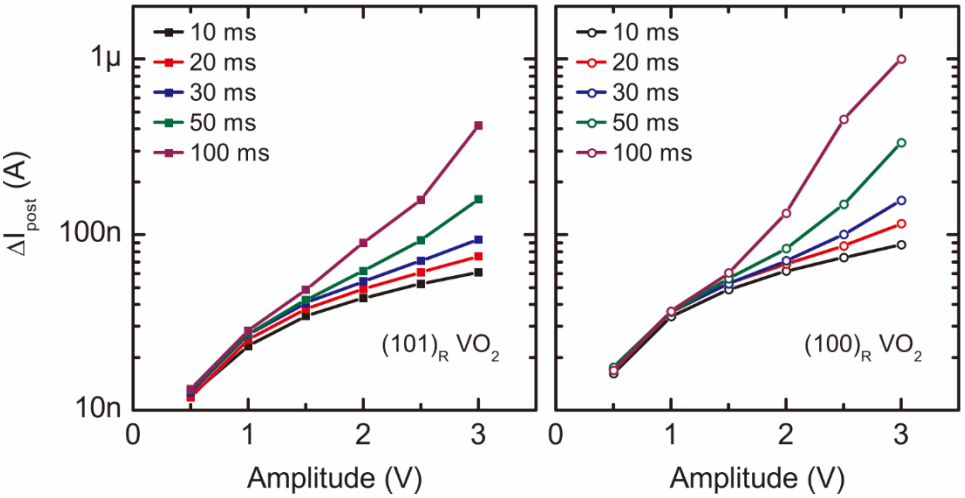
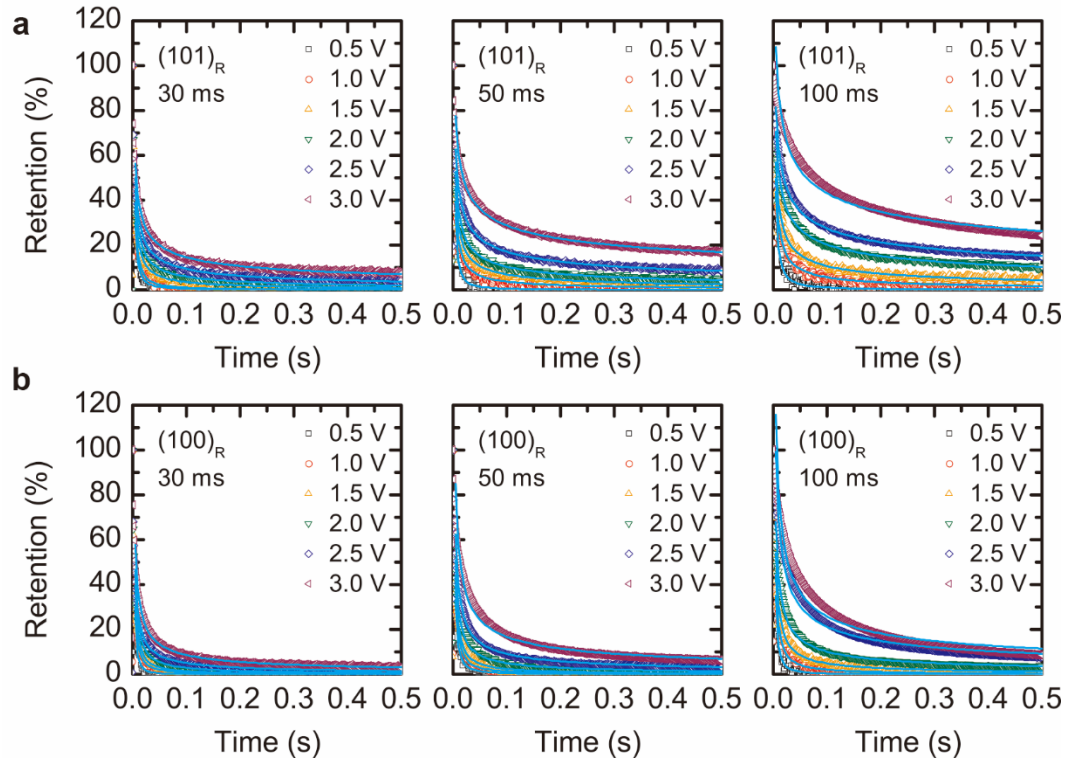


Figure S5 | EPSC peak of single V_{pre} pulse as a function of D_P and A_P $(101)_R$ and $(100)_R$-VO_2 synaptic transistors. The similar value of EPSC with short D_P (= 10 ms) and long D_P (=100 ms) at small A_P (= 0.5 V) means that there is no additional H^+ incorporation with long D_P. However, the EPSC with short D_P (= 10 ms) and long D_P (=100 ms) at large A_P (= 3.0 V) shows significant differences due to the large amount of H^+ incorporation in VO_2 lattices.

Figure S6



Pulse width	100 ms		50 ms		30 ms	
V_{pre} (V)	$(101)_R$	$(100)_R$	$(101)_R$	$(100)_R$	$(101)_R$	$(100)_R$
3.0 V	0.31	0.50	0.33	0.54	0.45	0.64
2.5 V	0.37	0.52	0.44	0.64	0.56	0.75
2.0 V	0.42	0.64	0.54	0.78	0.68	0.91
1.5 V	0.56	0.81	0.63	0.97	0.80	1.12
1.0 V	0.73	1.02	0.79	1.14	1.19	1.16
0.5 V	1.24	1.48	1.38	1.38	1.35	1.74

Figure S6 | The memory retention in the both VO_2 synaptic transistors with A_P (= 0.5 - 3.0 V) and D_P (= 30, 50, and 100 ms). The power function $\gamma = b \times t^{-m}$, where γ is the memory retention, b is the initial value, t is time, and m is the decay rate. Retention time increases as m decreases. By quantitative evaluation, in the same transistor, m decreased with increase in A_P and D_P.

Figure S7

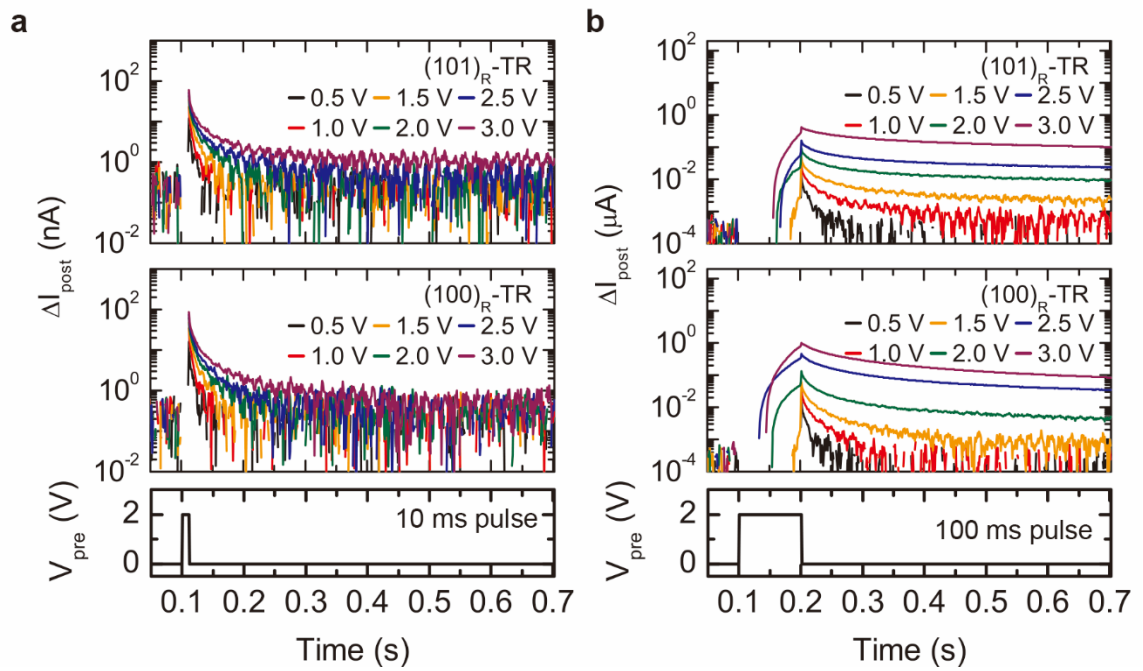


Figure S7 | a. a short D_P of V_{pre} pulse (= 10 ms) and **b.** a long D_P of V_{pre} pulse (= 100 ms) as a function of the A_P of V_{pre} in $(101)_R$ and $(100)_R$-VO_2 synaptic transistors in logarithmic scale.

Figure S8

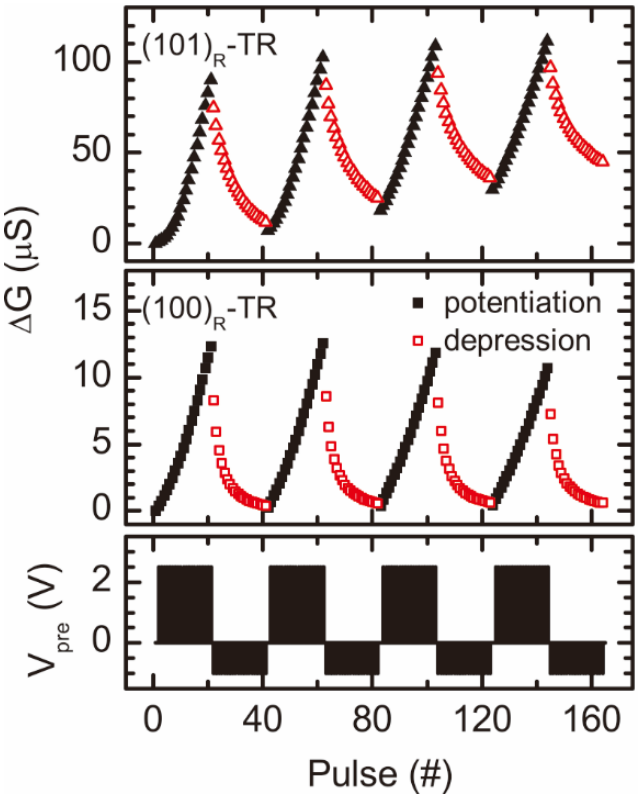


Figure S8 | Potentiation and Depression of $(101)_R$ and $(100)_R$ VO_2 synaptic transistors

Figure S9

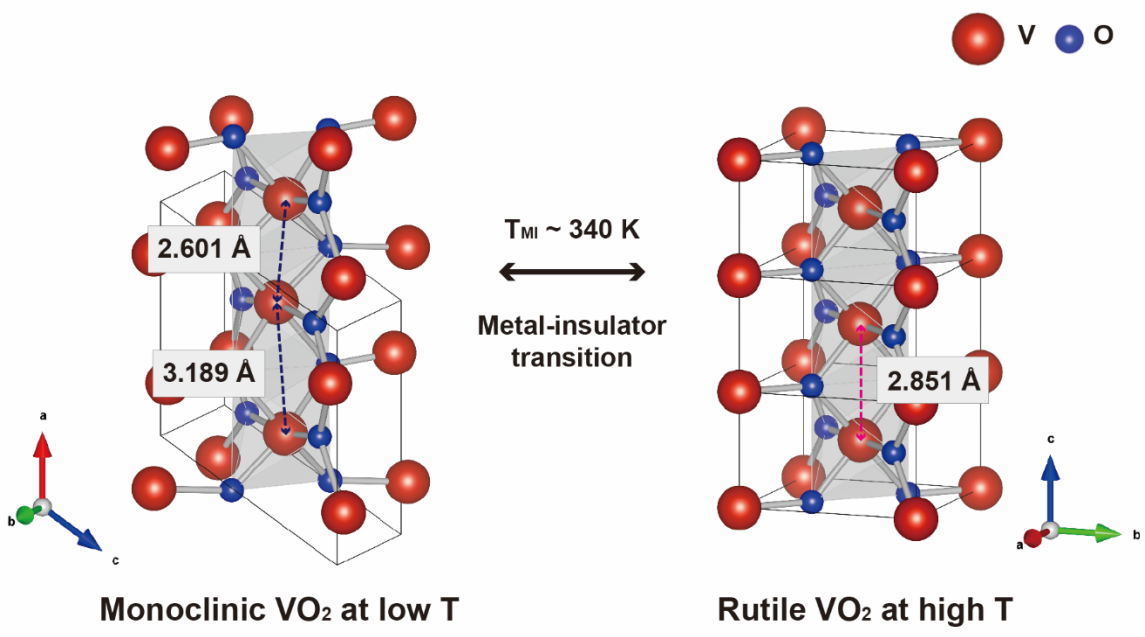


Figure S9 | the crystallographic axes of monoclinic VO_2 and rutile VO_2 phases