Electronic Supplementary Information

for

Thermal conductivity and electrical resistivity of single copper nanowires

*Wei-Tsu Peng,[a] Fu-Ren Chen,[a] and Ming-Chang Lu[b]**

[a]*Department of Mechanical Engineering, National Yang Ming Chiao Tung University, Hsinchu, 300, Taiwan*

[b]*Department of Mechanical Engineering, National Taiwan University, Taipei, 106, Taiwan*

*: Author to whom correspondence should be addressed

E-mail: mingchanglu@ntu.edu.tw

1. Fabrication Process of the Measurement Microdevices.

The fabrication process of the microdevices is schematically illustrated in Fig. S1, and is described as follows: (a) A thin layer of low-stress silicon nitride is grown on the silicon substrate; (b) a photoresist (PR) layer is coated on the silicon nitride, (c) the PR layer is patterned using photolithography, (d) electron-beam evaporation is employed for successively depositing Cr and Pt, (e) the lift-off process is applied to remove the excess Pt layer; (f) another PR layer is coated on the surface, (g) the PR layer is patterned using photolithography, (h) the reactive ion etching of silicon nitride is applied to pattern the silicon nitride layer, (i) the remaining PR layer is removed after cleaning the wafer, (j) the microdevice with two suspended membranes can be obtained by aqueous potassium hydroxide ($KOH_{(aq)}$) etching the silicon substrate beneath the two membranes.

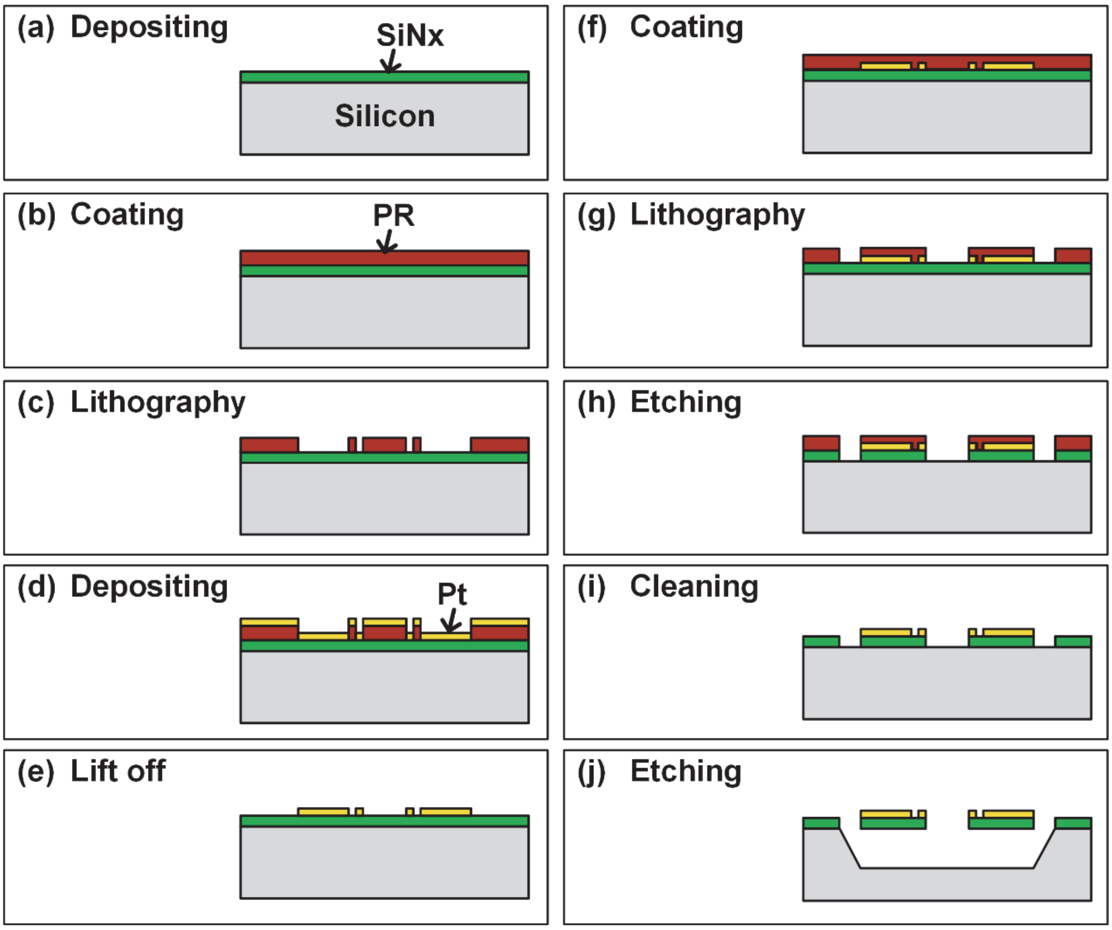

Fig. S1. Schematic diagram of the fabrication process.

2. Scanning Electron Microscopy (SEM) Images of the CuNWs.

The microdevice consists of two suspended membranes that are identical and parallel aligned to each other as shown in Fig. S2. The CuNWs are picked up onto the microdevice, bridging the two suspended membranes for measurements. Figs. S2(a)−(c) show the SEM images of the CuNWD195, CuNWD243, CuNWD255, respectively. The inserts are the magnified SEM images at the contact regions. The diameter of the CuNW is the averaged width of the nanowire, and the length of the CuNW is taken as the suspended length of the CuNW. The CuNWD195, CuNWD243, and CuNWD255 have 195.3, 243.1, and 255.3 nm in diameter, respectively, and the corresponding lengths are 6.50, 6.03, and 7.62 μm, respectively.

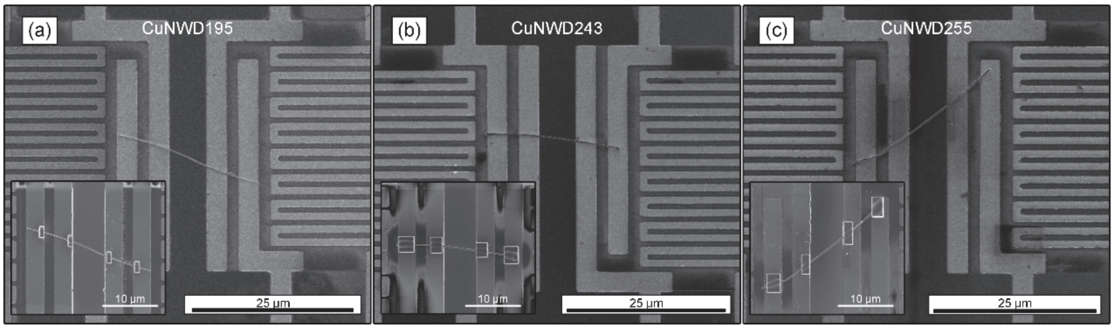

Fig. S2. The SEM images of (a) CuNWD195, (b) CuNWD243, and (c) CuNWD255.

3. Thermal Conductivity Measurement Method.

For the thermal conductivity (κ) measurement, a DC current is applied to heat up the left membrane (denoted as the heating membrane) of the microdevice shown in Fig. S2 by Joule heating. The heat flows to the right membrane (denoted as the sensing membrane) through the CuNW and raises its temperature. According to the literature[1-3], the thermal conductance (G) of a nanowire is derived from energy conservation and is determined by Fourier's law with the temperature difference between the two ends of the nanowire. The temperature difference is obtained from the measured resistances of the platinum coils on the heating and sensing membranes, and their temperature coefficient of resistances ($TCR= 1/R(\mathrm{d}R/\mathrm{d}T)$). Owing to the small temperature difference between the heating and sensing membranes for the high thermal conductance sample ($G \sim 10^{-7}$ W/K), the Wheatstone bridge circuit is applied to both of the heating and sensing membranes, as shown in the electric circuit diagram in Fig. S3.[3] The advantages of the Wheatstone bridge circuit in the κ measurement are (1) minimizing the temperature fluctuation of the sample stage, and (2) reducing the amplifier noise caused by the large dynamic range.[3] In Fig. S3, V_h and V_s are the measured voltages before entering the Wheatstone bridge circuits at the heating and sensing membranes, respectively. A DC voltage (V_{DC}) is applied to generate Joule heat on the heating membrane. The two external variable resistors, R_{ex1} and R_{ex2}, are used to adjust the AC current (i_{AC}) and the heating current (i_{DC}), respectively. The electric resistances on the heating and sensing membranes are[3]:

$$R_h = \frac{R_{h2}}{\left(\frac{V_{gh}}{V_h}\right)+\left(\frac{R_{h3}}{R_{h1}+R_{h3}}\right)} - R_{h2} \tag{1}$$

$$R_s = \frac{R_{s2}}{\left(\frac{V_{gs}}{V_s}\right)+\left(\frac{R_{s3}}{R_{s1}+R_{s3}}\right)} - R_{s2} \tag{2}$$

where R and V represent the resistance and voltage, respectively, and the subscripts h and s denote the heating and sensing membranes, respectively. The Wheatstone bridge circuit at the heating membrane consists of the heating membrane resistor (R_h) and three variable resistors (i.e., R_{h1}, R_{h2}, and R_{h3}). The Wheatstone bridge circuit at the sensing membrane consists of the sensing membrane resistor (R_s), pair resistor (R_{s1}), and two variable resistors (i.e., R_{s2} and R_{s3}). The R_h, R_s, R_{s1}, and CuNW are located inside the cryostat (colored area in Fig. S3). R_{s1} which is the additional on-chip pair Pt resistor has the same resistance value as R_s. The effect of ambient temperature fluctuation in the cryostat on both the R_s and R_{s1} are nominally equal.[3] Therefore, the change in resistance from the ambient fluctuations can be canceled out due to the symmetric configuration of the Wheatstone bridge circuit. During experiments, alternating voltages, V_{AC_h} and V_{AC_s}, are applied, and the gate voltages (V_{gh} and V_{gs}) and the midpoint voltages (V_{Bh} and V_{Bs}) are measured. The midpoint voltages of V_{Bh} and V_{Bs}

are needed to acquire V_h and R_{s1}:

$$V_h = \left(\frac{R_{h1}+R_{h3}}{R_{h3}}\right) V_{Bh} \tag{3}$$

$$R_{s1} = \left(\frac{V_s}{V_{Bs}}\right) R_{s3} - R_{s3} \tag{4}$$

In the measurements, we set V_{AC_s}= V_s= 10 mV and V_{AC_h}= 5 V. Before the κ measurements (i.e., when the temperature of the cryostat is at room temperature), the R_{h1} is adjusted to be close to the value of R_h. In addition, the variable resistors R_{h3} and R_{s3} are tuned to approach the values of R_{h2} and R_{s2}, respectively. Therefore, as $R_{s2} \sim R_{s3}$, $R_{s1} \sim R_s$. Due to the symmetric configuration of the Wheatstone bridge circuit, the fluctuations from the ambient temperature can be wiped out and will not affect the measurement of V_{gs}. Thus, making $R_{s2} \sim R_{s3}$ and $R_{s1} \sim R_s$ increases the precision in measuring the temperature on the sensing membrane.[3] For the heating membrane, although the R_{h1} was not placed inside the cryostat, the symmetric configuration of the Wheatstone bridge circuit is able to minimize the amplifier noise,[3] thereby increasing the accuracy of the temperature measurement on the heating membrane. The i_{AC} and i_{DC} passing through the heating membrane are:

$$i_{AC} = \frac{V_{AC\_h}}{(R_{ex1}+R_{eff})}\left(\frac{R_{h1}+R_{h3}}{R_{h1}+R_{h2}+R_{h3}+R_h}\right) \tag{5}$$

$$i_{DC} = \left(\frac{V_{DC}}{R_{ex2}+R_{eff}}\right)\left(\frac{R_{h1}+R_{h3}}{R_{h1}+R_{h2}+R_{h3}+R_h}\right) \tag{6}$$

where $R_{eff} = \frac{(R_{h1}+R_{h3})(R_{h2}+R_h)}{(R_{h1}+R_{h3})+(R_{h2}+R_h)}$ is the effective resistance of the bridge circuit on the heating membrane. In the heating process, the V_{DC} is ramped from 0 to 9 V for supplying i_{DC} into the heating membrane. Given that i_{DC} is coupled to the i_{AC}, the R_{ex1} and R_{ex2} are set to be 10 MΩ and 500 kΩ, respectively, to ensure that the i_{DC} is at least one order of magnitude larger than the i_{AC}.

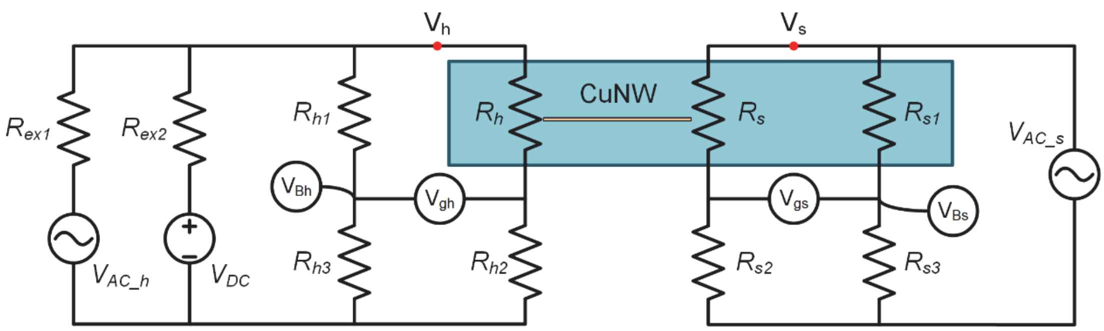

Fig. S3. The Wheatstone bridge circuit diagram.

Fig. S4 gives the R_h and R_S values as a function of the environmental temperature (T_0).

In this figure, the R_h and R_S are obtained without supplying i_{DC}. The measured resistances have contributions from the resistances of the platinum coil on the membranes (R_c) and the two suspended beams ($2R_b$). The temperature on the membrane is uniform but it varies linearly along the beam.[3] To acquire the temperature on the membrane alone, the effective change in the membrane resistance with respect to the temperature ($\Delta R_{\text{effctive}}/\Delta T$) is obtained from:[3]

$$\left(\frac{\Delta R_{effective}}{\Delta T}\right) = \left(\frac{R_c+R_b}{R_c+2R_b}\right)\left(\frac{\Delta R}{\Delta T}\right) \tag{7}$$

From Eq. (7), the temperature rise of the membranes can be obtained during the heating process.

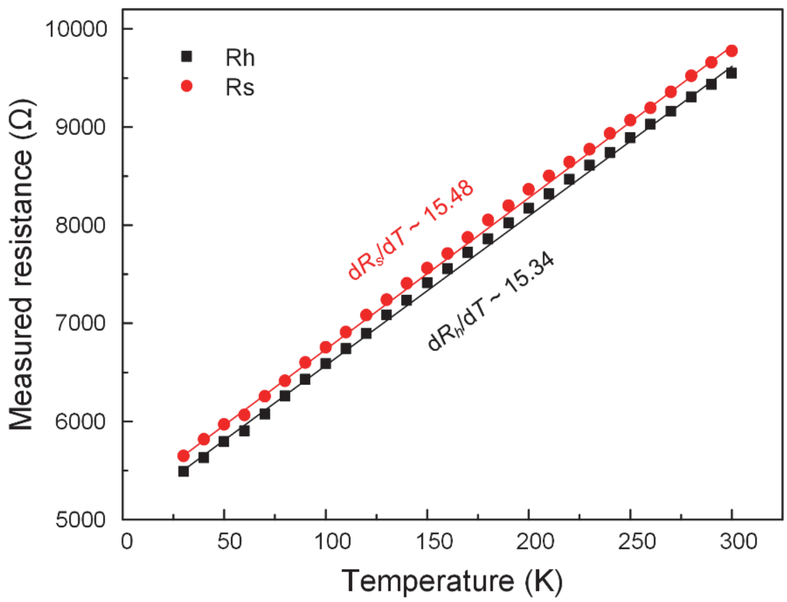

Fig. S4. Electrical resistances of the platinum coils on the heating and sensing membranes as a function of environmental temperature.

The G of the CuNW is derived through $G= Q\Delta T_s/(\Delta T_h^2-\Delta T_s^2)$, where Q is the power generation in the heating membrane and the beam, and ΔT_h ($=T_h-T_0$) and ΔT_S ($= T_s-T_0$) are the temperature rises of the heating membrane and the sensing membrane, respectively.[1] Using Fourier's law, the thermal conductivity of the nanowire is: $\kappa= GL/A$, where L is the suspended length of the CuNW between the heating and sensing membranes, and A ($= \pi D_{nw}^2/4$) is the cross-sectional area of the CuNW, where D_{nw} is the diameter of the CuNW. The power passing through the CuNW is $Q_s= Q\Delta T_s/(\Delta T_h+\Delta T_s)$. Fig. S5 depicts the power passing through the nanowire versus the temperature difference between heating and sensing membranes. The G of the sample was obtained from the slope of the fitting curve in Fig. S5. The error for the κ was the standard errors from the G values at various applied powers.

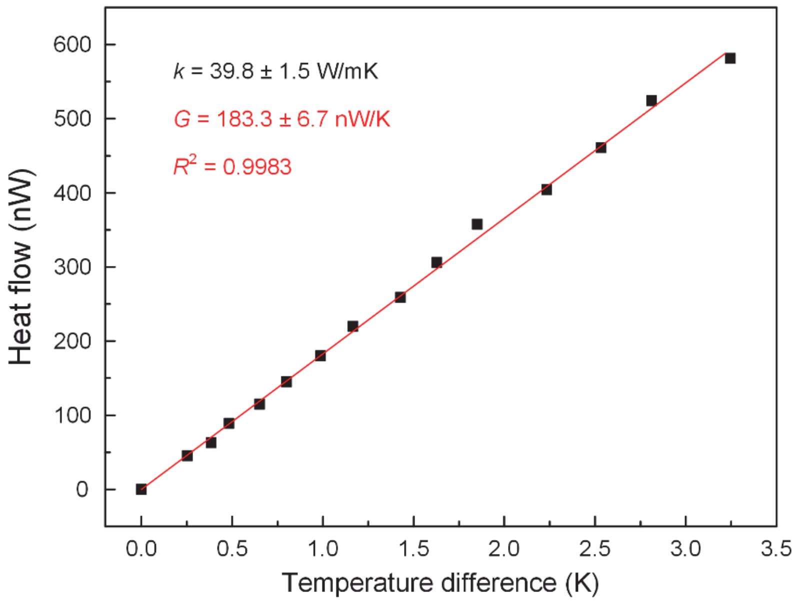

Fig. S5. The power (Q_s) through the CuNWD195 versus the temperature difference (ΔT) between the two membranes. The measured κ is 39.8 ± 1.5 $Wm^{-1}K^{-1}$. The G in the figure was obtained from the slope of the fitting curve. The error for the κ is the standard errors obtained from the G values at various applied powers.

4. Thermal Conductivity of a Single SiO_2 Nanowire.

To validate our measurement method, the thermal conductivity of a single SiO_2 nanowire was measured. The thermal conductivity of the single SiO_2 nanowire is depicted as the open red squares in Fig. S6. Our measurement result agreed well with the literature value of a SiO_2 thin film (solid black circles).[4]

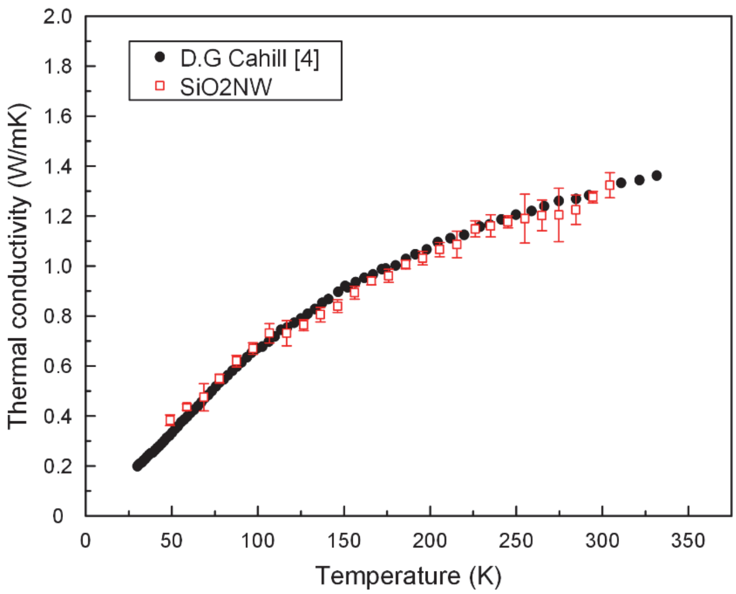

Fig. S6. Thermal conductivity of a single SiO_2 nanowire (red squares) comparing to the literature value (black circles).[4]

5. Electron Mean Free Path (MFP) Limited by the Defects and Grain Boundaries.

From Fig. 3(c), the MFPs limited by the defects (l_d) were evaluated by assuming that each defect takes over the same area of A_{core}/N_d, where A_{core} is the area of copper core. The average defect diameter (D_d) follows the relation: $A_{core}/N_d = \pi D_d^2/4$. Here, it is assumed that $l_d = D_d$. Thus, the l_d values for CuNWD195, CuNWD243, and CuNWD255 were obtained as 19.8, 14.7, and 17.9 nm, respectively.

In addition, the following assumptions were made for evaluating the MFPs limited by the grain boundaries: (1) There are N grains inside a CuNW and each grain has a characteristic length l_{bi} and an area A_i, and (2) the grains having the same axial length (L) as the nanowire are aligned to each other in parallel. The l_{bi} was obtained by means of hydraulic diameter: $l_{bi} = 4A_i/P_i$, where P_i is the periphery of A_i. From the assumptions, the total resistance along the nanowire caused by the multiple grains in the nanowire (R_{GB}) is expressed as:

$$\frac{1}{R_{GB}} = \sum_i^N \frac{1}{R_i} \tag{8}$$

where N is the number of grains counted from the cross-sectional TEM images shown in Fig. 3(a) and R_i is the resistance for the i_{th} grain. Eq. (8) can be rewritten as:

$$\frac{1}{\rho_{GB}\frac{L}{A_{GB}}} = \sum_i^N \frac{1}{\rho_i\frac{L}{A_i}} \tag{9}$$

where ρ_{GB} is the resistivity resulted from the multiple grains, A_{GB} is the total cross-sectional area occupied by the N grains, and ρ_i and A_i are the resistivity and area of the i_{th} grain. Eq. (9) can be re-expressed as:

$$\frac{A_{GB}}{\rho_{GB}} = \sum_i^N \frac{A_i}{\rho_i} \tag{10}$$

From Drude's model, the resistivities are a function of MFP:

$$\rho_{GB} = \frac{m_e v_F}{ne^2 l_b} \tag{11}$$

$$\rho_i = \frac{m_e v_F}{ne^2 l_{bi}} \tag{12}$$

where l_b is the overall effective MFP limited by the multiple grains, m_e and e are the electron mass and electron charge. For copper, the Fermi velocity (v_F) is 1.57×10^6 ms^{-1} and electron concentration (n) is 8.45×10^{28} m^{-3}. From Eq. (10) to Eq. (12), the l_b is:

$$l_b = \frac{1}{A_{GB}} \cdot \sum_i^N A_i l_{bi} \tag{13}$$

Here, A_{GB} was taken as the copper core area. The l_b values obtained from Eq. (13) for CuNWD195, CuNWD243, and CuNWD255 were 56.2, 92.1, and 36.5 nm, respectively.

6. Dislocations in the CuNWs.

The dislocation of the atom arrangement at grain boundary was only found in CuNWD255 as shown in Fig. S7. The area enclosed by red dashed line show the discontinuity of the atoms at the grain boundary, meaning that some of the atoms are missing in these areas.

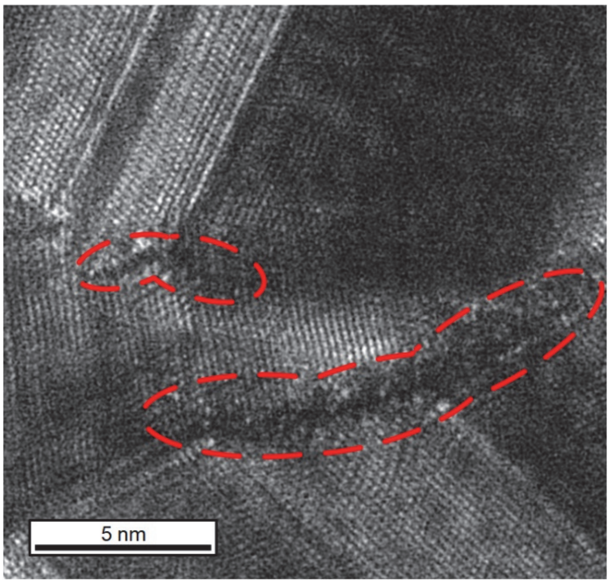

Fig. S7. Dislocation of atom arrangement at grain boundary of CuNWD255 contoured by the red dashed line.

7. Evaluation of the Effective Thermal Conductivity of Copper Core.

Because of the oxide layer, the effective diameter of copper core (D_e) is reduced from the diameter of the CuNWs (D_{nw}): $D_e = D_{nw} - 2\times t$, where t is the thickness of copper oxide. To acquire the contribution of κ from the copper core, we assume a one-dimensional heat transfer model with two parallel thermal resistances of copper core and copper oxide:

$$\frac{1}{R_t} = \frac{1}{R_{Cu}} + \frac{1}{R_{ox}} \tag{14}$$

where R represents as the thermal resistance. The subscripts t, cu, and ox denote the total, copper core, and oxide layer resistances, respectively. The thermal resistance is equal to the suspended length of CuNWs (L) divided by the product of cross-sectional area (A) and κ. Finally, the effective κ of the copper core is derived as:

$$\kappa_{cu} = (\kappa_t - \kappa_{ox})\left(\frac{D_{nw}}{D_e}\right)^2 + \kappa_{ox} \tag{15}$$

In the equation, the κ_{ox} was taken as 7.14 $Wm^{-1}K^{-1}$,[5] and the κ_t were the measured values for CuNWs.

References

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