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Received 00th January 20xx,
Accepted 00th January 20xx

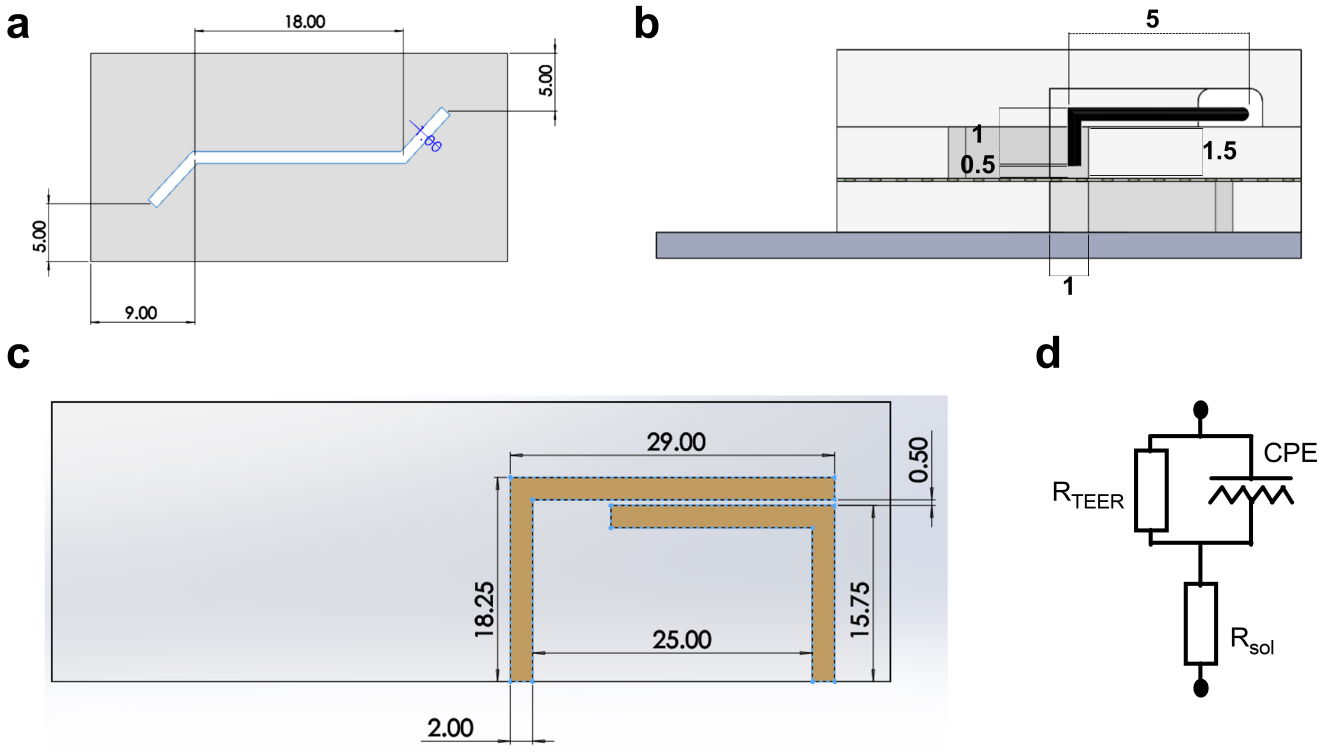
DOI: 10.1039/x0xx00000x

## Supplementary information for:

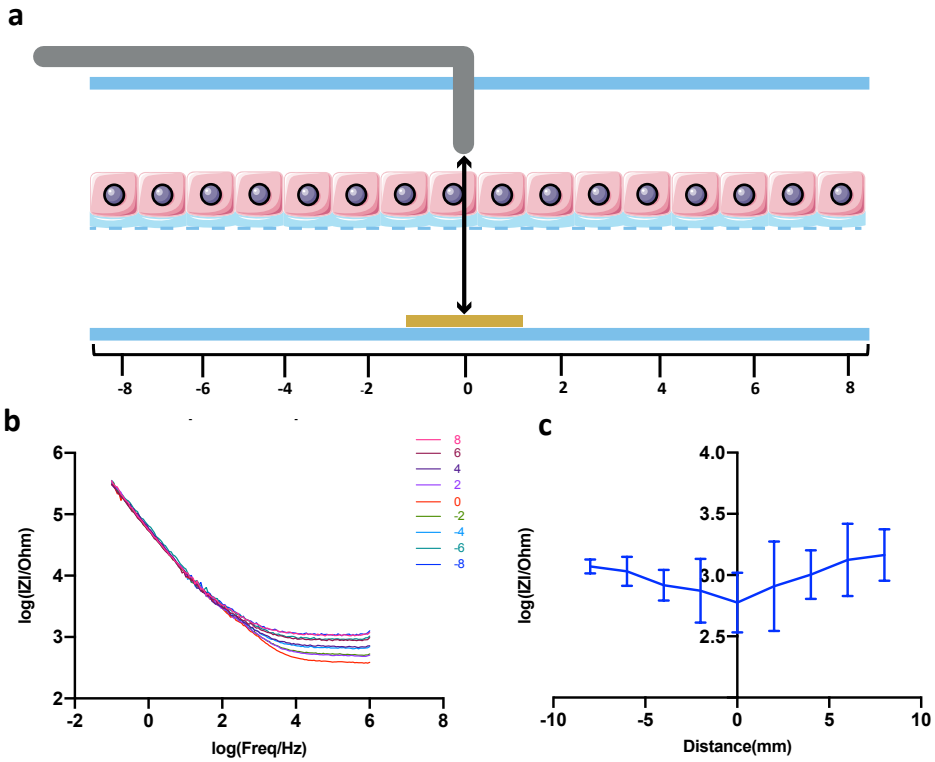
# Spatial Trans-Epithelial Electrical Resistance (S-TEER) Integrated in Organs-on-Chips

Noa Renous [a] , Mark D. Kiri *[a], Ronny A. Barnea [b], Rossana Rauti [a], Yael Leichtmann-Bardoogo [a], and Ben M. Maoz [a, c, d]

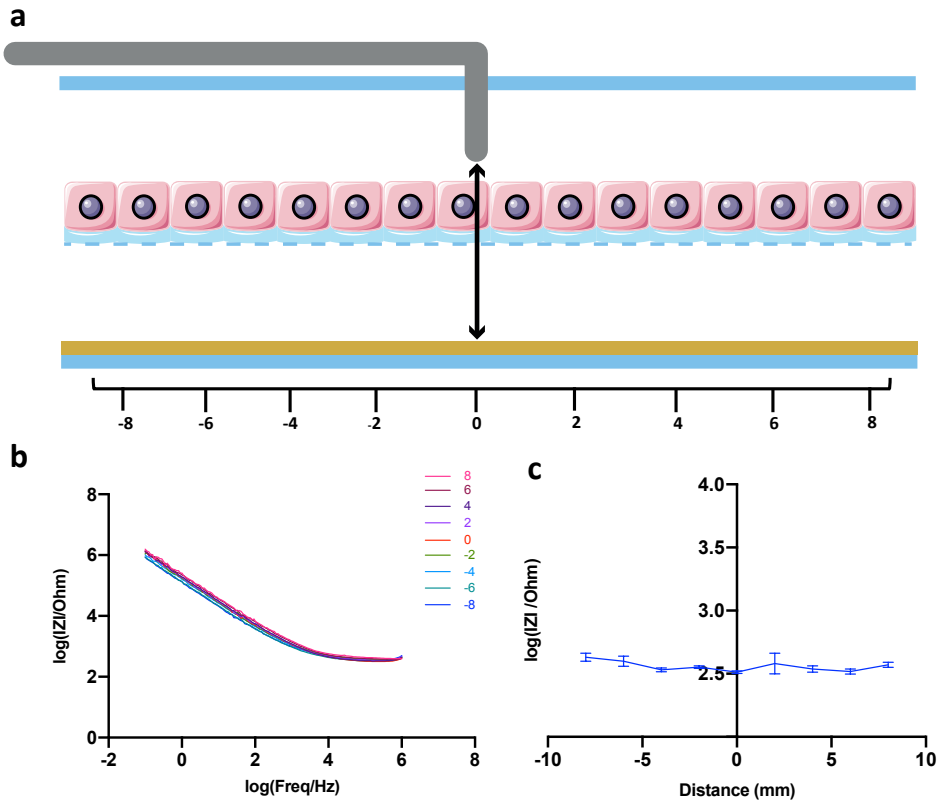
[a.] . *Department of Biomedical Engineering, Tel Aviv University, Tel Aviv 69978, Israel*
[b.] *School of Chemistry, Sackler Faculty of Exact Sciences, Tel Aviv University, Tel Aviv 69978, Israel*
[c.] *Sagol School of Neuroscience, Tel Aviv University, Tel Aviv 69978, Israel*
[d.] *The Center of Nanoscience and Nanotechnology, Tel Aviv University, Tel Aviv 69978, Israel*
**Author are equal contributors*
Electronic Supplementary Information (ESI) available: [details of any supplementary information available should be included here]. See DOI: 10.1039/x0xx00000x



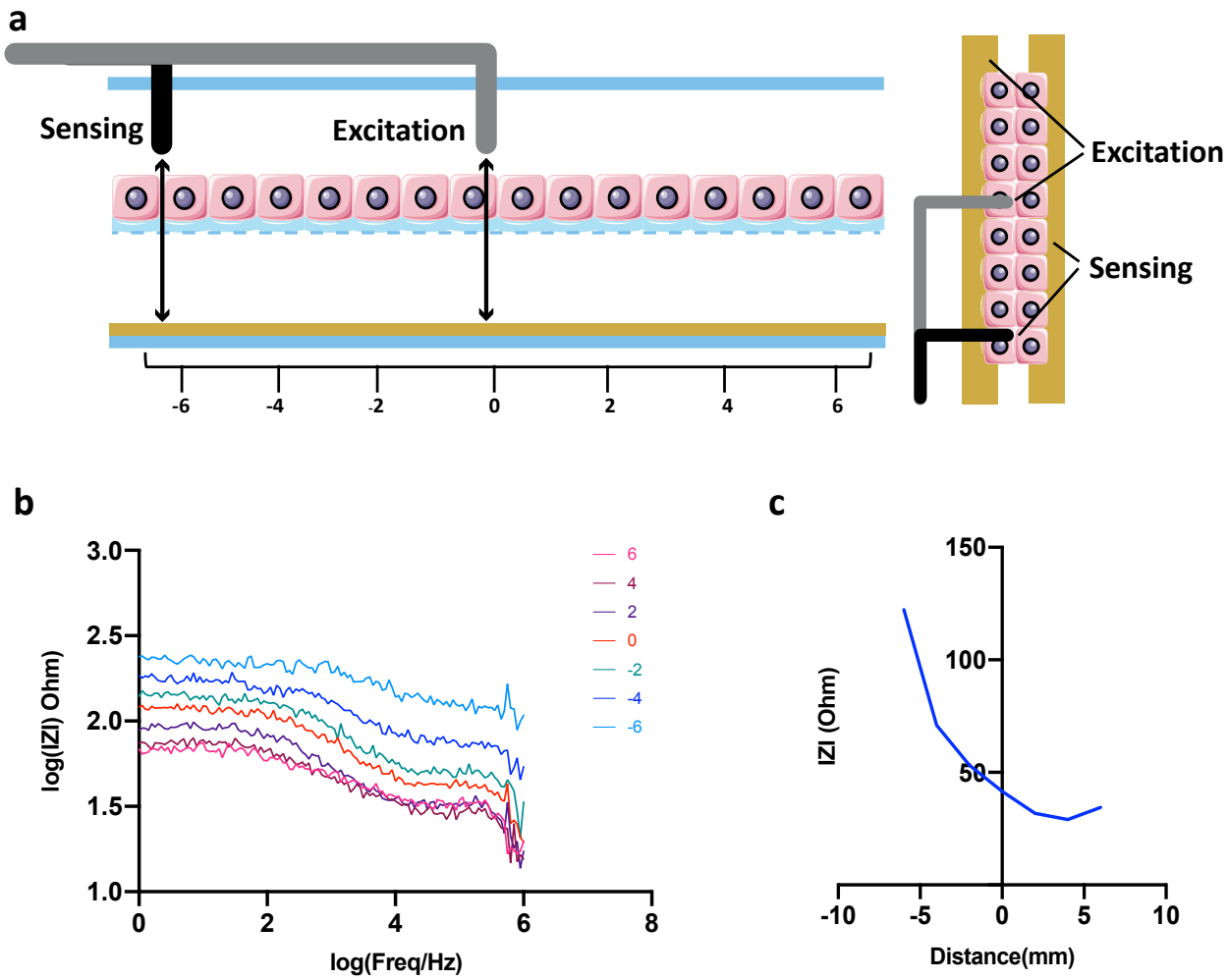

**Supplementary Fig. 1** Dimensions of the S-TEER chip. All dimensions are in mm. a. PDMS channel. b. cross section view of the entire chip. c. Bottom electrodes. d. The equivalent circuit suggested to present the TEER values in the system.



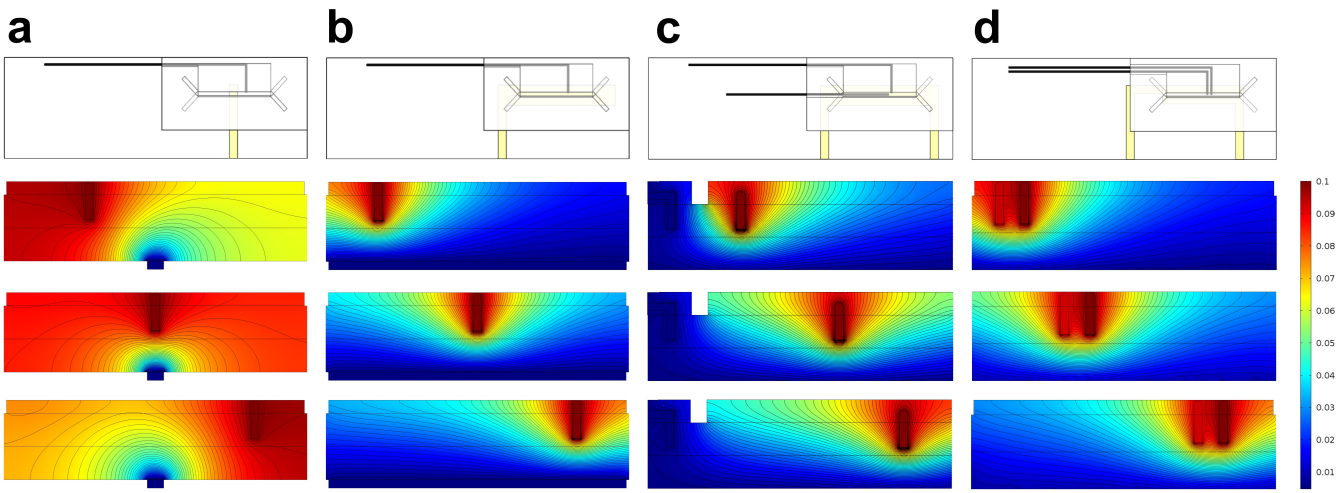

**Supplementary Fig. 2** Two-point electrode system, with a top scanning electrode and a bottom fixed one. a. Illustration of the system. b. Impedance measurements at various frequencies. c. The impedance values (at low frequencies). as a function of the distance from the bottom electrode. Impedance spectroscopy shows that the greater the distance between the electrodes, the greater the impedance.



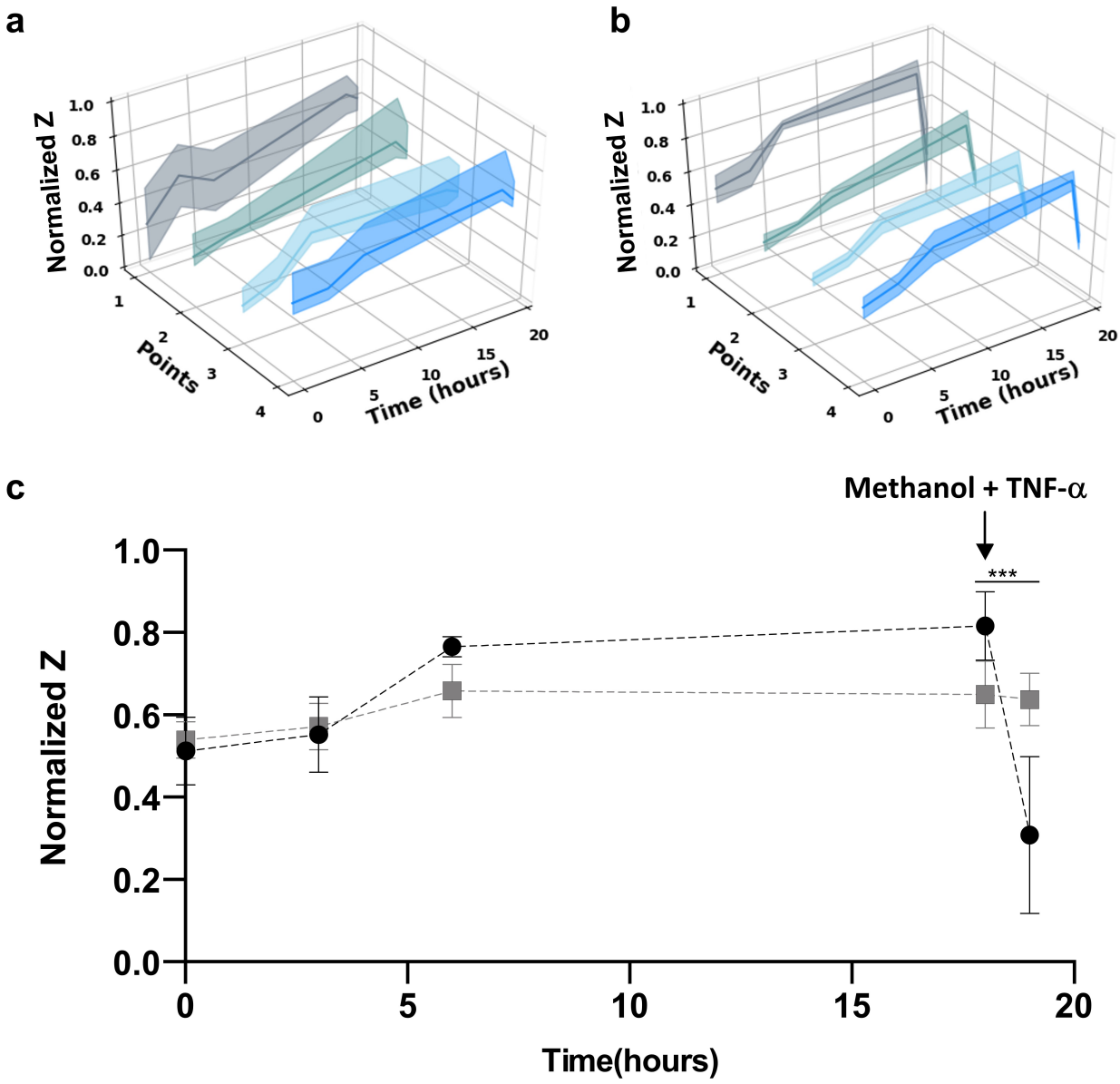

**Supplementary Fig. 3** Two-point electrode system, with a top scanning electrode and a full bottom electrode throughout the whole channel. a. Illustration of the system. b. Impedance measurements at various frequencies. c. Impedance values (at low frequencies) as a function of the distance from the bottom electrode. Impedance spectroscopy shows that all points are equal, without distance dependency.



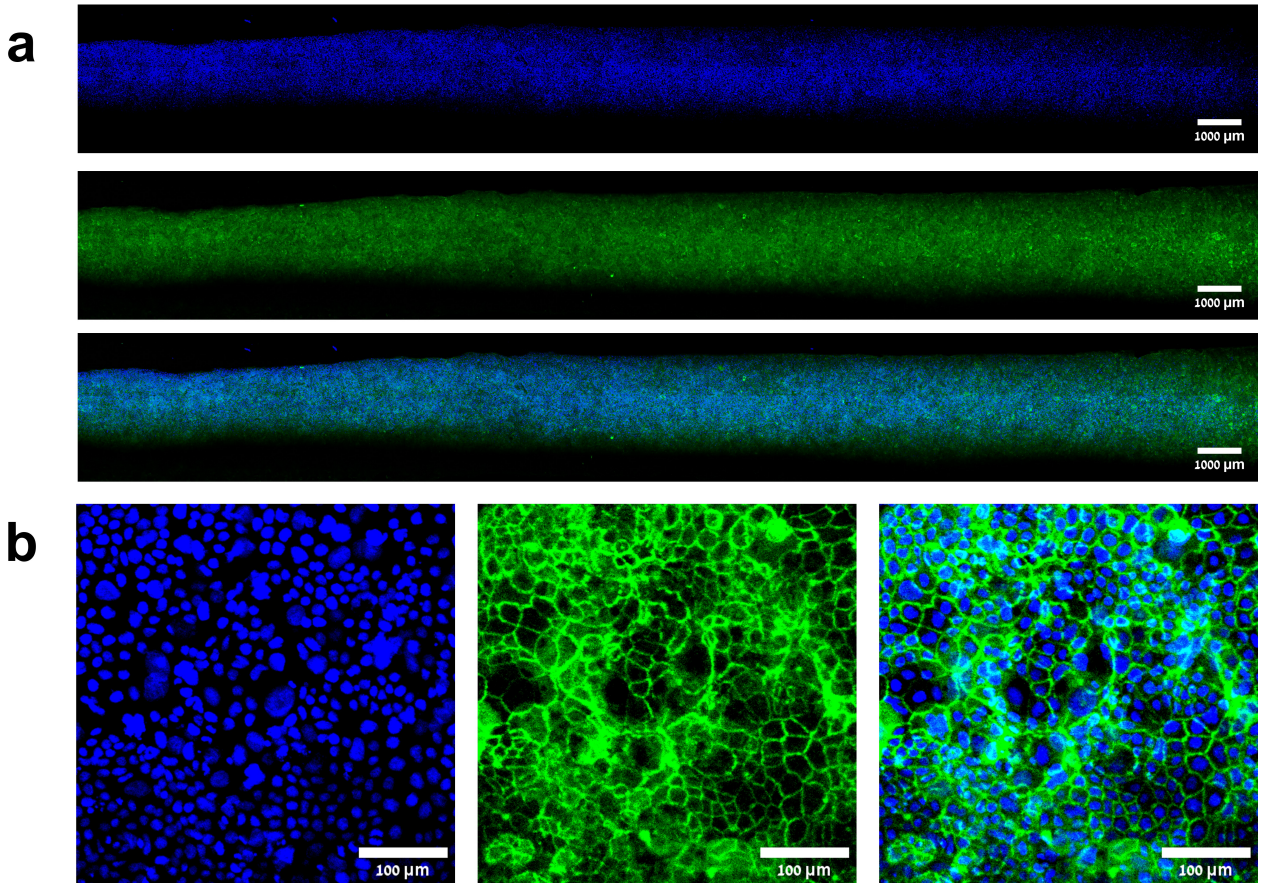

**Supplementary Fig. 4** Four-point electrode system, with one top excitation scanning electrode and the other sensing electrode fixed at the beginning of the channel. The bottom electrodes run throughout the whole channel with 0.5 mm distance between them. a. Illustration of the system. b. Impedance measurements at various frequencies, c. The impedance values (at low frequencies) as a function of the distance from the bottom electrode. Impedance spectroscopy shows that when the distance between the top electrodes increases, the impedance decreases due to lower sensitivity.



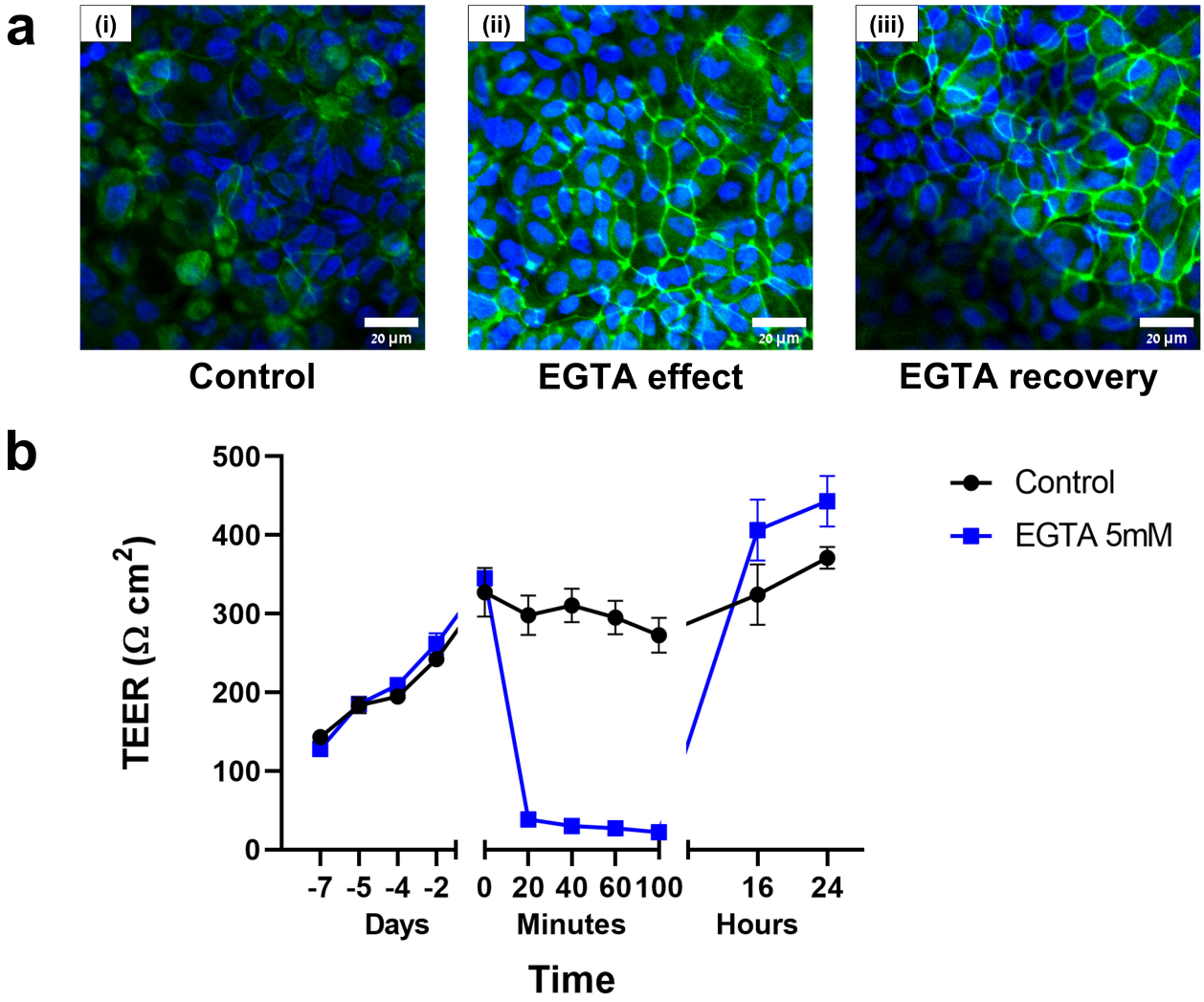

**Supplementary Fig. 5** Simulation of the electric potential of the different versions of the S-TEER-Chip. Top line: Four model versions of the S-TEER-chip: a. Two-electrode S-TEER-Chip. b. Two-electrode S-TEER-Chip with full bottom electrode. c. S-TEER-Chip with one fixed top electrode. d. Final version of the S-TEER-Chip, with two moving electrodes. Simulations: Each simulation presents the electrical potential along the chip, in a cross-section view. The scanning electrodes are positioned at the center (top line of simulation), left of the chip's center (middle line of simulation), and right of the chip's center (bottom line of simulation).




**Supplementary Fig. 6** Tempo-spatial measurements of barrier properties challenged with TNF-α. a. Control: normalized impedance values of spatial points over time. b. Chip with challenged with TNF-α: Normalized impedance values of spatial points over time. c. Normalized impedance values of point 1, developed over time due to cell proliferation forming a confluent layer. TNF-α was added and significantly dropped the measured value ($P < 0.001$).




**Supplementary Fig. 7** Immunofluorescent confocal imaging of a confluent Caco-2 layer on the top channel of a S-TEER chip. a. Whole channel view: (i) DAPI (ii) ZO-1 (iii) Merge. b. Closer look at the cell monolayer: (i) DAPI (ii) ZO-1 (iii) Merge.




**Supplementary Fig. 8** Validation of EGTA effect on Caco-2 barrier functioning on transwells. a. Confocal images of Caco-2 in different stages of the experiment; (i) Control transwell w/o EGTA (ii) Under EGTA effect (iii) After 1 day of recovery. Nuclei stained in blue and ZO-1 in green. b. TEER values over different times point – control over cells treated with 5mM of EGTA solution.

**Supplementary Mov 1.** S-TEER-Chip usage, with manual movement of the scanning electrodes.

**Supplementary Mov 2.** S-TEER chip under flow.

**Supplementary Mov 3.** Spatial accuracy of the moving top electrodes using a caliber.

**Supplementary Mov 4.** Simulation of electrical potential across the channels of the S-TEER-Chip.