Electronic Supplementary Material (ESI) for Materials Horizons.

**Supporting Information**

# CMOS Back-end compatible memristors for in-situ digital and neuromorphic computing application

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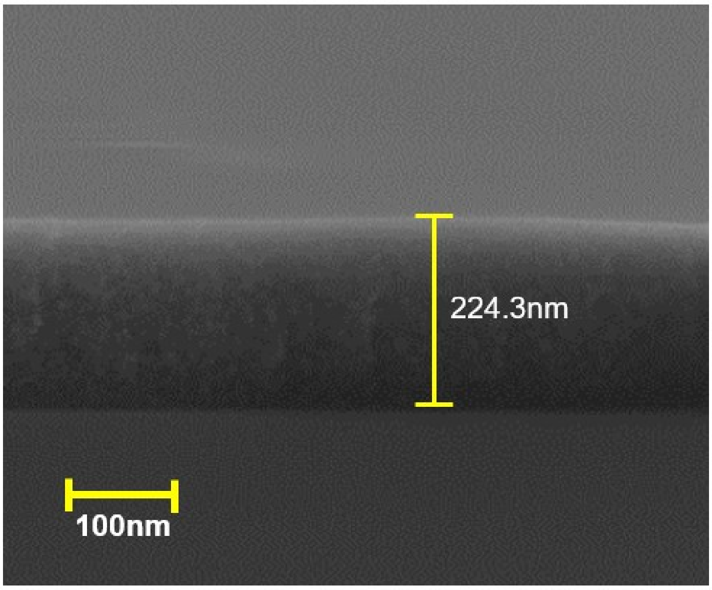


**Figure S1.** The SiCO:H layer grown for 8 minutes was collected by Scanning Electron Microscope (SEM), the thickness obtained by SEM and the thickness measured by SE are more consistent.

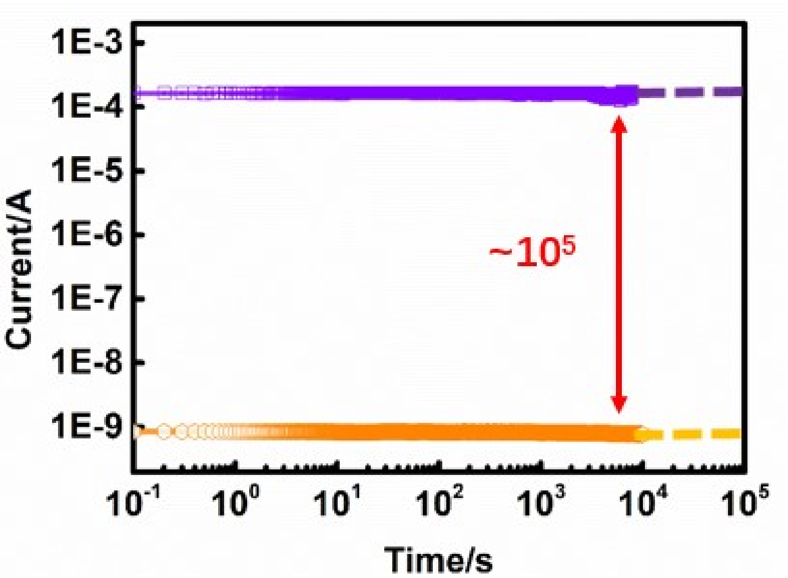


**Fig.S2** The retention characteristics of Ag top electrode memristors were tested at a reading voltage of 50 mV.

**Table S1** Recently reported RRAM material system based on Ag or Cu top electrode. The basic characteristics such as the threshold voltage of the device are displayed. IHRS and ILRS are the corresponding currents in high-resistance and low-resistance states, respectively.

| Material system | /HRS | /LRS | ON/OFF | $V_{th}$ (DC) | Endurance/s | Compatible with CMOS process | Ref. |
|---|---|---|---|---|---|---|---|
| Our work | 30 pA | 500 μA | ~ $10^5$ | ~ 0.3V | > $10^4$ | Y | |
| $Ag/SiO_2/Pt$ | ~ 1 pA | 100 nA | ~ $10^5$ | ~ 6 V | | Y | [1] |
| $Ag/SiO_x/C$ | ~ 1 pA | 50 uA | ~ $5*10^7$ | ~ 2 V | | Y | [2] |
| $Ag/TiO_2/Pt$ | | 1 nA | | ~ 40 V | | Y | [3] |
| $Cu/SiO_2/Pt$ | ~10 pA | 500 μA | ~ $5*10^7$ | ~ 0.6 V | > 50 | Y | [4] |
| Cu/a-C/Pt | ~ 10 uA | 50 μA | 5 | ~ 0.55V | | Y | [5] |
| $Cu/TiO_x/Pt$ | ~ 100 pA | 1 μA | ~ $10^4$ | ~ 0.4 V | > 150 | Y | [6] |
| $TaN/GeO_x/HfON/Ni$ | ~ 300 pA | 100 nA | ~ $9*10^2$ | ~ 3 V | > $10^6$ | Y | [7] |
| $Ag/AlO_x/Pt$ | ~ 100 pA | 100 μA | ~ 104 | ~ 1 V | | Y | [8] |
| $Ag/a\text{-}La_{0.3}Mn_{0.7}SrO_3/Pt$ | ~ 1 nA | 10 μA | ~ $10^4$ | ~ 0.4 V | > 100 | N | [9] |
| Pt/Ag2S/Ag/Ag2S/Pt | ~ 300 nA | 10 μA | 33 | 0.2 V | | N | [10] |
| Cu/Cu-MoOx/Pt | | 100 mA | ~ 20 | ~ 2 V | > $10^6$ | N | [11] |
| Pt/PCMO/Pt | ~ 100 uA | 1 mA | ~ 100 | ~ 4 V | > $10^4$ | N | [12] |
| $Ag/Ge_xS_y/W$ | ~ 100 pA | 10 μA | ~ $10^5$ | ~ 1.5 V | > $10^5$ | N | [13] |
| $Ag/Ta_2O_5/Fe_3O_4/Pt$ | ~ 500 nA | 5 mA | ~ $10^5$ | ~ 0.4 V | > $10^4$ | N | [14] |
| $Ag/MXene/SiO_2/Pt$ | ~ 1 uA | 500 μA | ~ 500 | ~ 0.2 V | > $10^3$ | N | [15] |
| Ag/a-IGZO/ITO | ~ 100 uA | 10 mA | ~ 100 | ~ 1.3 V | > $10^6$ | N | [16] |
| $Ag/ZnMn_2O_4/p\text{-}Si$ | ~ 1 m | 1 A | ~ $10^3$ | ~ 2 | > $10^4$ | N | [17] |
| Pt/Ag/LZO/Pt | ~ 1 uA | 1 mA | ~ $10^3$ | ~ 0.4 V | > $10^4$ | N | [18] |
| $Ag/Er_2O_3/ITO$ | | | ~ 7 | ~ 2 V | | N | [19] |
| $Ag/ZrO_2$:Cu/Pt | ~ 1 nA | 100 μA | ~ $10^5$ | ~ 0.7 V | | N | [20] |

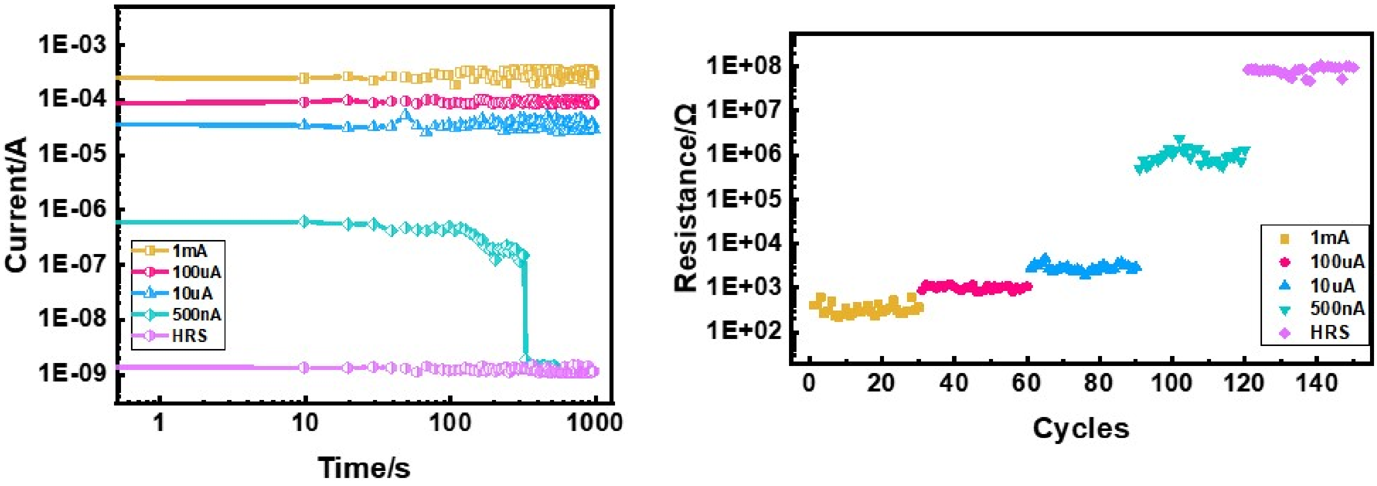


**Fig.S3** **(a)** The retention characteristics of the Ag / SiCO:H / Pt device at different compliance levels (HRS, 500nA, 10uA, 100uA, 1mA). **(b)** The low resistance value of Ag / SiCO:H / Pt device changes under different compliance levels, showing the characteristics of the multi-resistance state. (HRS, 500nA, 10uA, 100uA, 1mA).

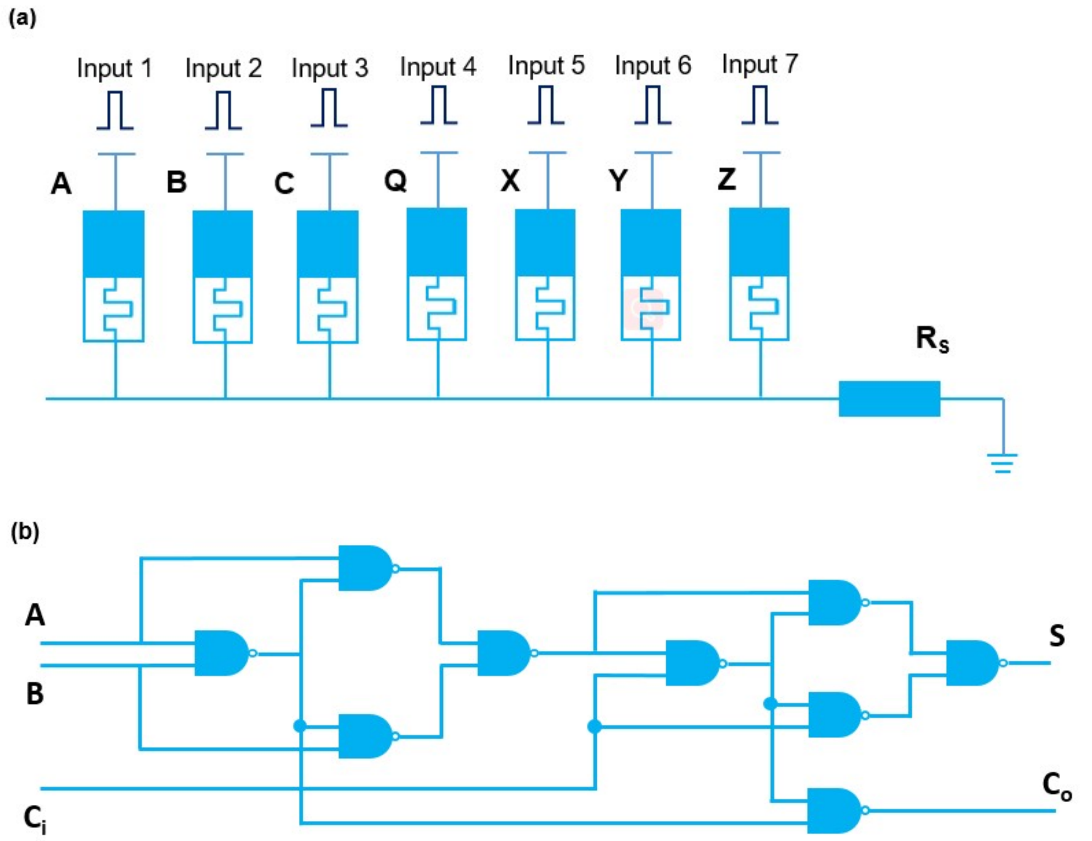
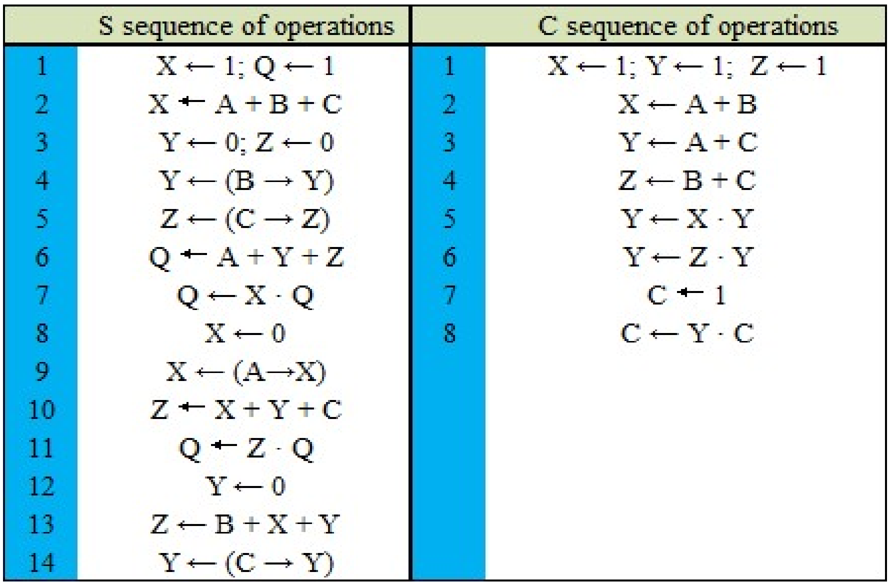
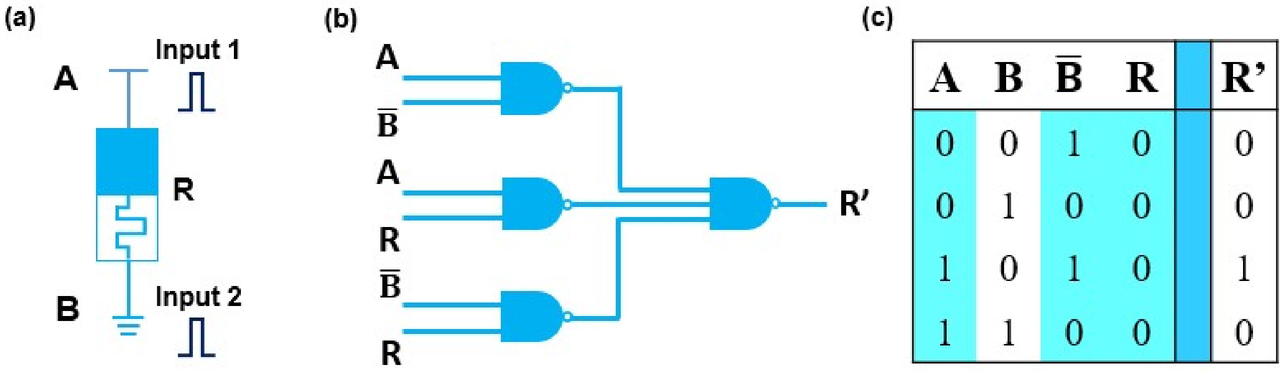


**Fig.S4 (a)** The circuit diagram of a one-bit full adder based on the basic logic of "IMP" based on the memristor. The circuit requires seven memristors. **(b)** The realization of a one-bit full adder logic circuit based on a traditional CMOS circuit requires 8 NAND logic to build, and each NAND logic requires 4 MOS transistors

**Table S2** shows the calculation sequence of the summation S and the carry C to the higher order.



| | S sequence of operations | | C sequence of operations |
|---|---|---|---|
| 1 | $X \leftarrow 1; Q \leftarrow 1$ | 1 | $X \leftarrow 1; Y \leftarrow 1; \ Z \leftarrow 1$ |
| 2 | $X \leftarrow A + B + C$ | 2 | $X \leftarrow A + B$ |
| 3 | $Y \leftarrow 0; Z \leftarrow 0$ | 3 | $Y \leftarrow A + C$ |
| 4 | $Y \leftarrow (B \rightarrow Y)$ | 4 | $Z \leftarrow B + C$ |
| 5 | $Z \leftarrow (C \rightarrow Z)$ | 5 | $Y \leftarrow X \cdot Y$ |
| 6 | $Q \leftarrow A + Y + Z$ | 6 | $Y \leftarrow Z \cdot Y$ |
| 7 | $Q \leftarrow X \cdot Q$ | 7 | $C \leftarrow 1$ |
| 8 | $X \leftarrow 0$ | 8 | $C \leftarrow Y \cdot C$ |
| 9 | $X \leftarrow (A \rightarrow X)$ | | |
| 10 | $Z \leftarrow X + Y + C$ | | |
| 11 | $Q \leftarrow Z \cdot Q$ | | |
| 12 | $Y \leftarrow 0$ | | |
| 13 | $Z \leftarrow B + X + Y$ | | |
| 14 | $Y \leftarrow (C \rightarrow Y)$ | | |



| A | B | $\overline{B}$ | R | | R' |
|---|---|---|---|---|---|
| 0 | 0 | 1 | 0 | | 0 |
| 0 | 1 | 0 | 0 | | 0 |
| 1 | 0 | 1 | 0 | | 1 |
| 1 | 1 | 0 | 0 | | 0 |

**Fig.S5. (a)** One memristor can realize "MIG" logic. **(b)** A circuit that implements a multi-bit voter based on a traditional CMOS circuit requires a total of four NAND logic, and each NAND logic requires four MOS transistors. **(c)** Supplement to the truth table of MIG logic in the original text.

## Reference

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