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Supporting Information

Progressive p-channel vertical transistors using electrodeposited copper oxide designed with grain boundary tunability

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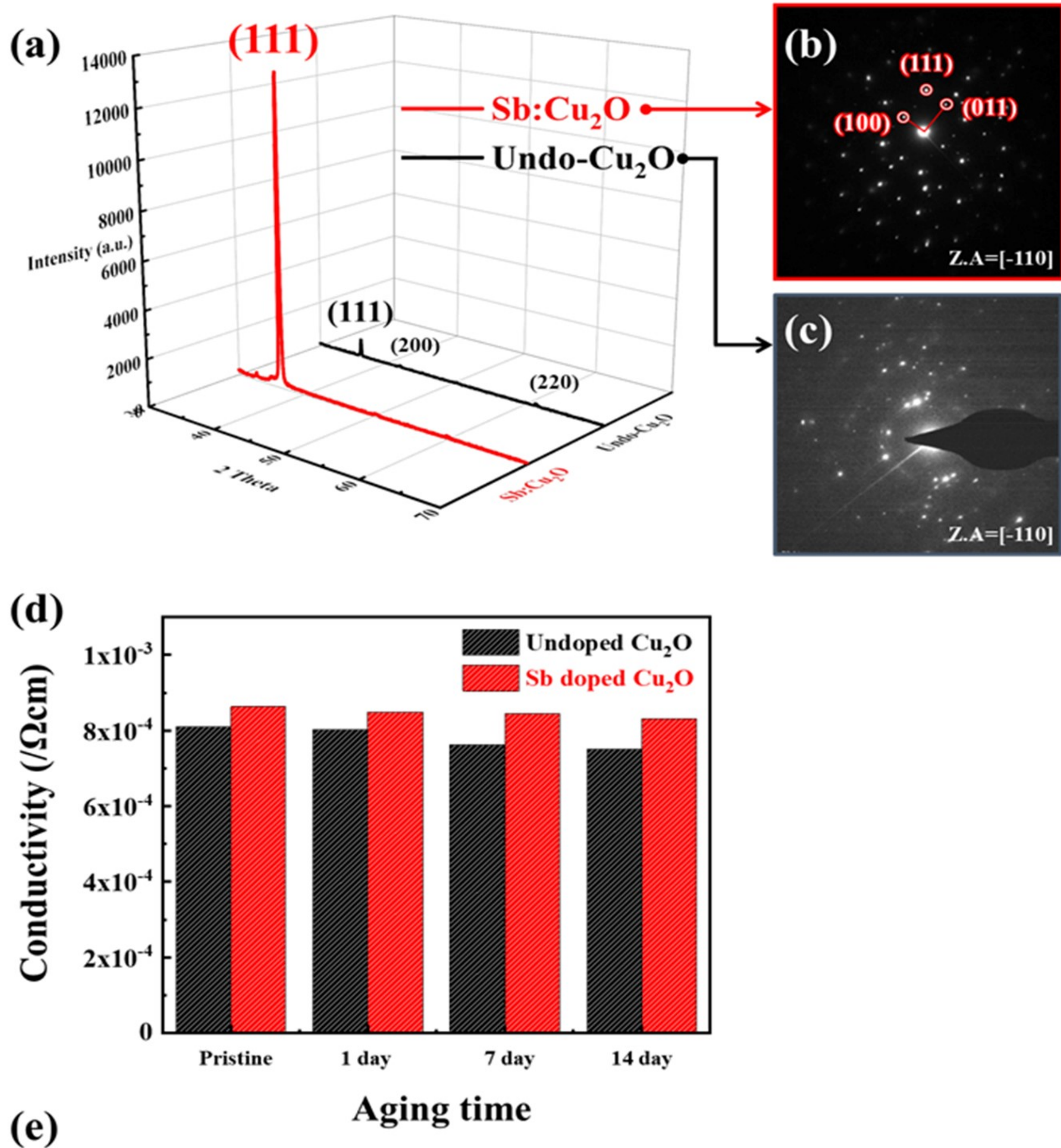
Table S1 Comparative electrical properties of thin film transistor using *p*-type oxide semiconductors



(e)

	Carrier concentration (cm^{-3})	Mobility (cm^2/Vs)
Undoped Cu_2O	1.9×10^{13}	2.7
Sb:Cu_2O (1 µm)	1.7×10^{13}	29.1
Sb:Cu_2O (0.5 µm)	1.62×10^{13}	28.8

Figure S1. (a) XRD pattern of undoped Cu_2O lower intensity random oriented grains and Sb: Cu_2O strong intensity along [111] preferred orientation, (b),(c) Selected area diffraction patterns obtained from Sb:Cu_2O and undoped Cu_2O films, respectively, (d) shows comparative aging time histogram of undoped Cu_2O and Sb:Cu_2O for 14 days' time duration, and (e) hall-effect measurements.

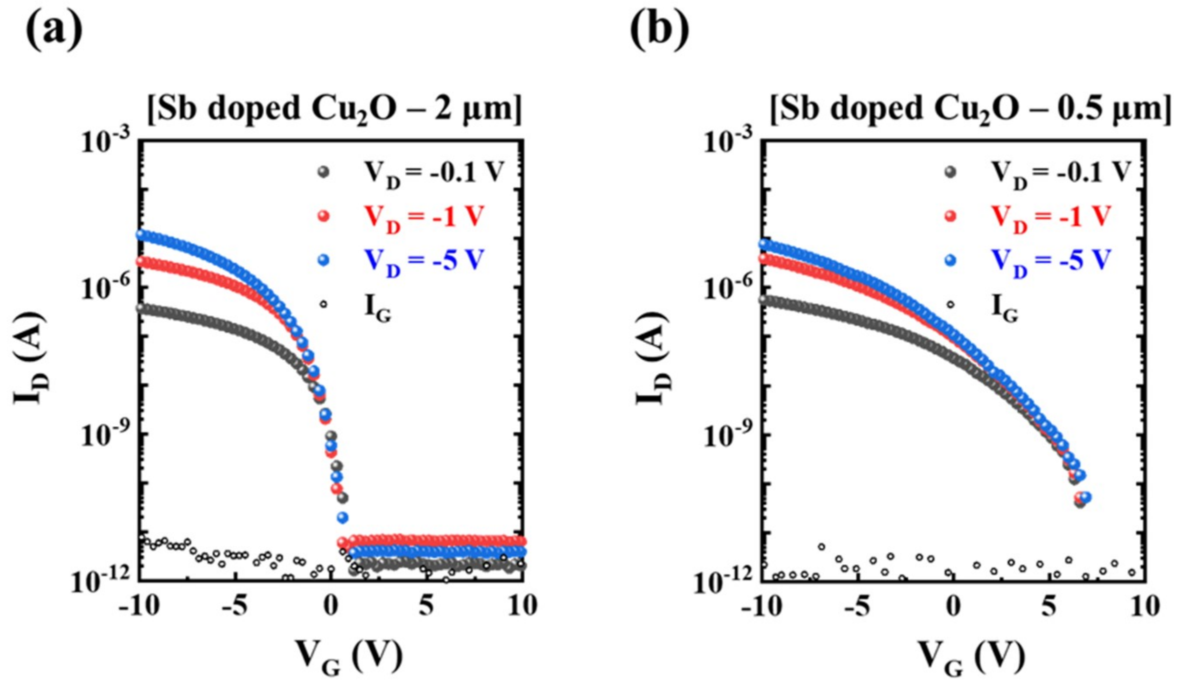


Figure S2. Shows transfer curve and the performance of the transistor based on channel thickness, (a) transfer curve of Sb doped Cu_2O for 2 µm thickness, and (b) transfer curve of Sb doped Cu_2O for 0.5 µm thickness.

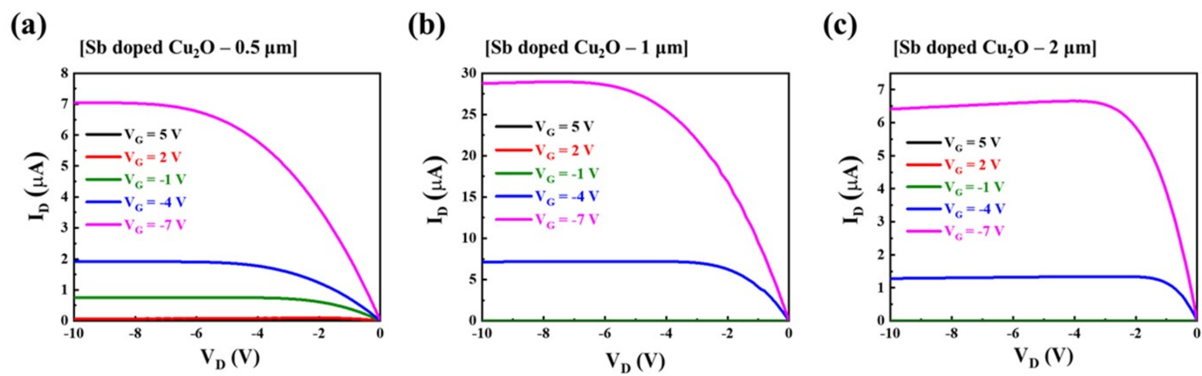


Figure S3. Output curves of *p*-type Cu_2O vertical transistors with different channel thicknesses: (a) 0.5 μm, (b) 1 μm, and (c) 2 μm.

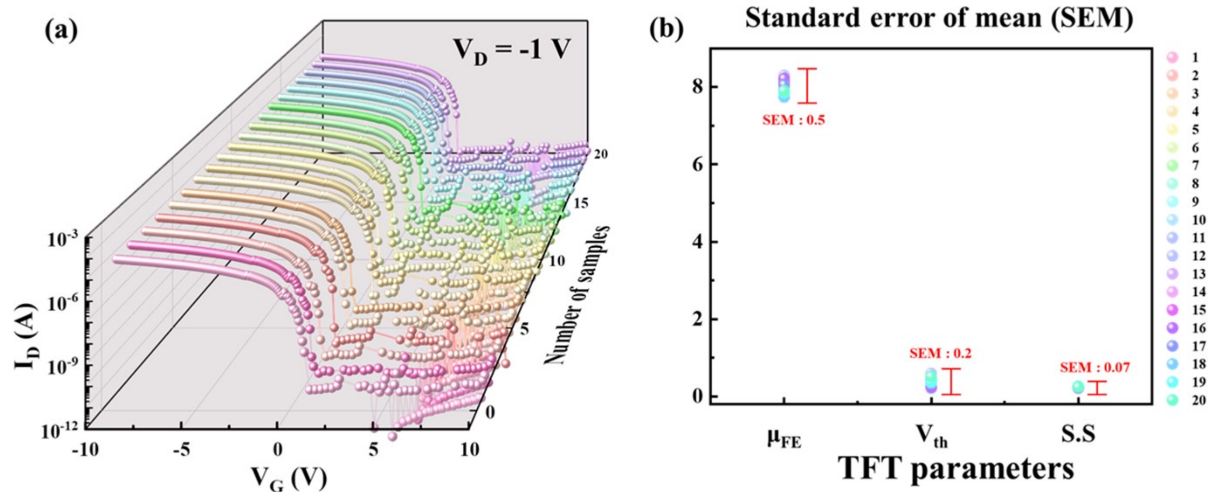


Figure S4. Reproducibility and reliability of p-Cu_2O vertical transistors from 20 devices (a) transfer curve, and (b) Standard error of mean and variance of transistor parameters.

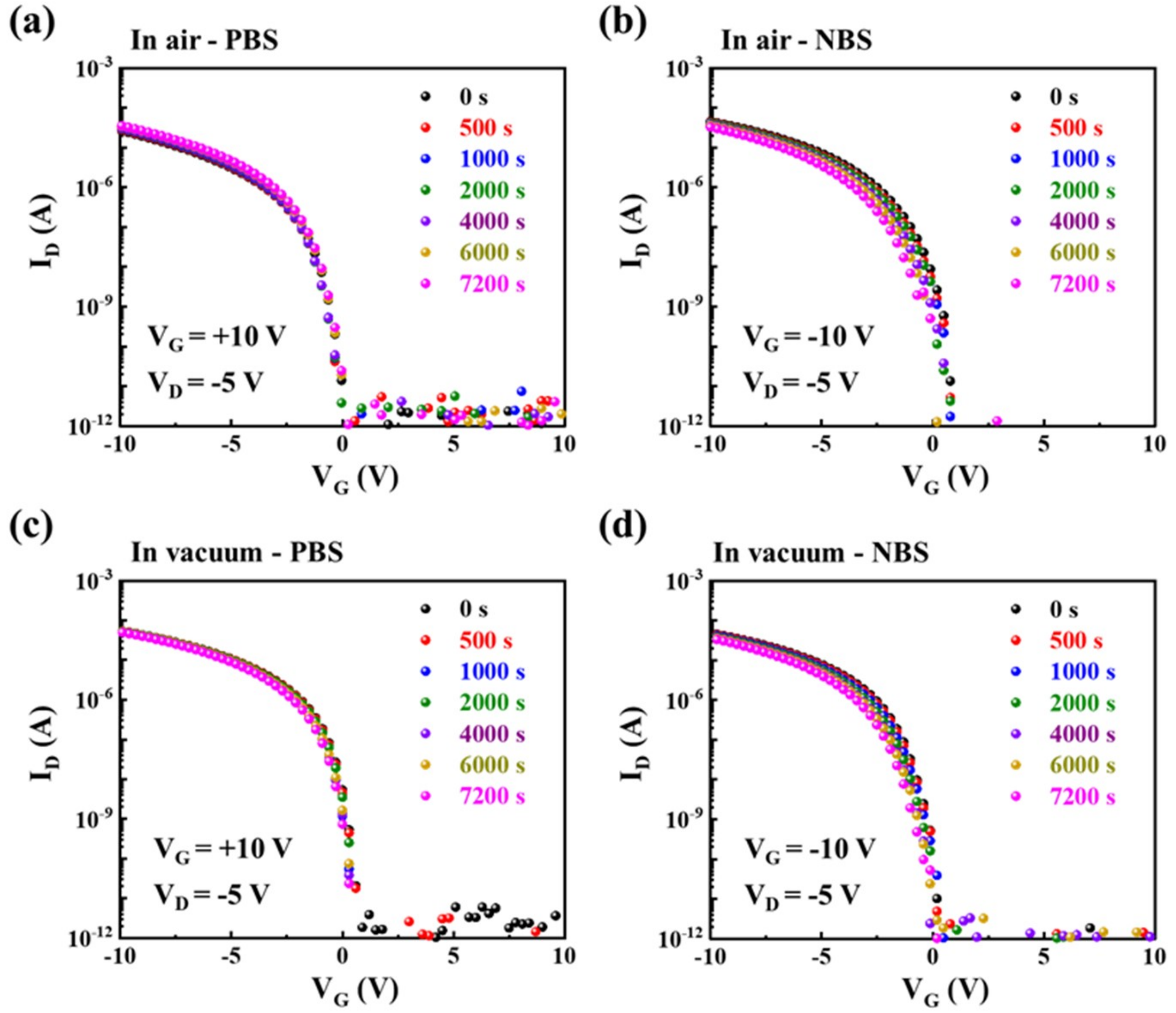


Figure S5. Shows stability tests performance for the Sb doped Cu_2O transistor in air and vacuum environment, (a) positive bias test in air environment, (b) negative bias test in air environment, (c) positive bias test in vacuum environment, and (d) negative bias stress test vacuum environment.

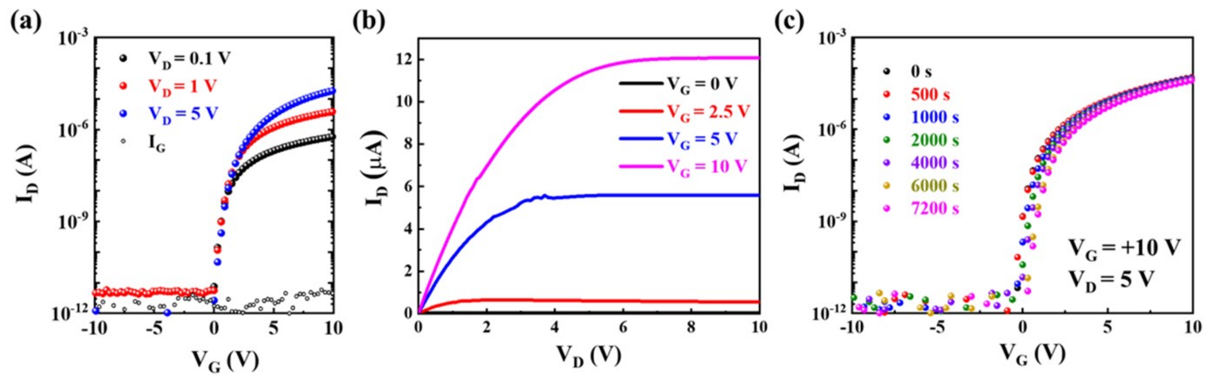


Figure S6. Electrical properties of *n*-type IGZO TFTs: (a) transfer curve, (b) output curve, and (c) positive bias stability tests at V_G = 10 V and V_D = 5 V for 2 h in air atmosphere.

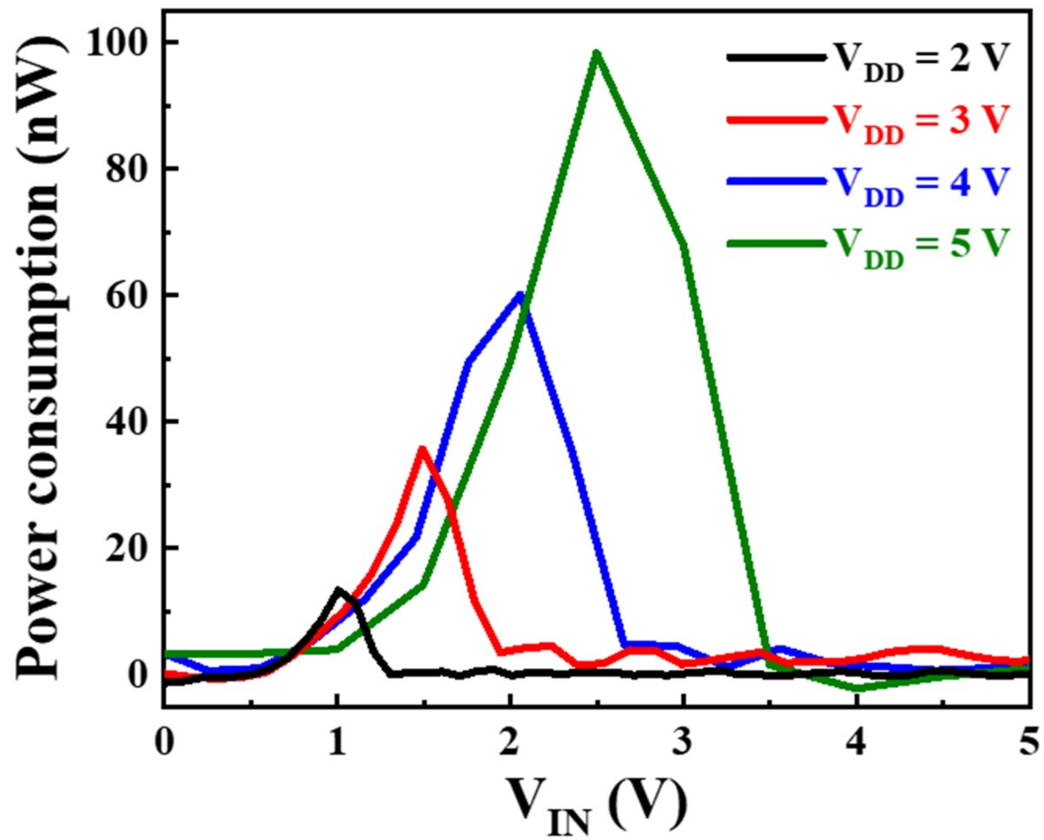


Figure S7. Power consumption characteristics of the CMOS inverter for V_{DD} = 2, 3, 4, and 5 V.

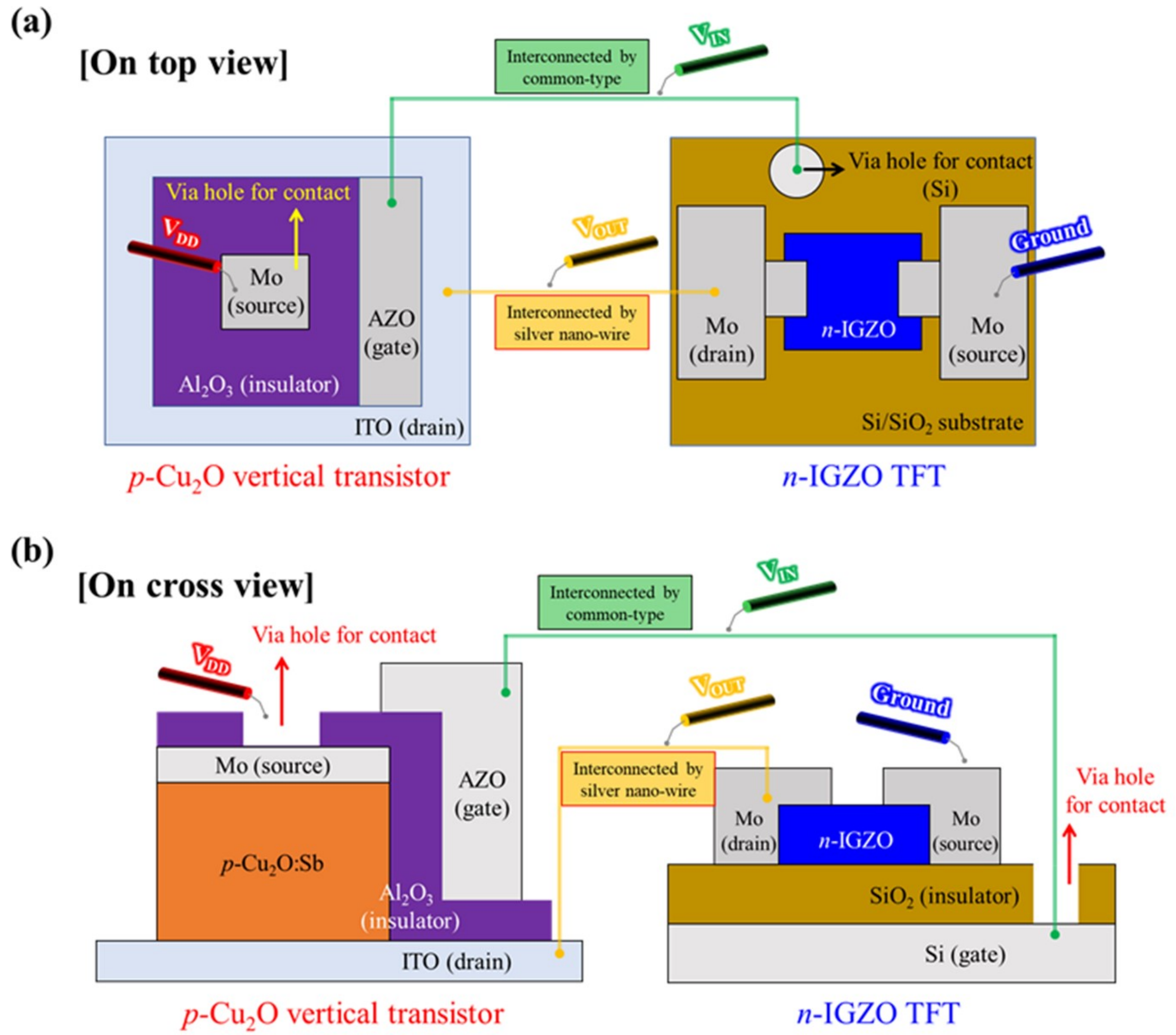


Figure S8. Schematic of our CMOS inverter using *p*-Cu_2O vertical TFT and *n*-IGZO TFT. (a) Top-view and (b) cross-view of the structure.

Table S1. Comparative electrical properties of thin film transistor using *p*-type oxide semiconductors.

Material	V_{th} (V)	S.S (V/dec)	μ_{FE} (cm^2/Vs)	I_{on}/I_{off}	Ref.
Cu_2O	**0.4**	**0.24**	**8**	**2×10^8**	**Our work**
SnO_x	-1.3	1.7	0.8	8.1×10^3	1
Ga:Cu_2O	-4.56	7.72	0.74	1.06×10^3	2
Cu_xO	-	0.11	0.75	2.81×10^8	3
SnO	~1.2	~10	~1.4 - 1.8	10^5	4
Cu_2O	-8.83 ± 1.99	2.35 ± 1.22	-	4.1×10^6	5
Cu_2O	-13.0	29.2	1.5×10^{-3}	5×10^3	6
Cu_2O	0.3	0.137	2.7	1.5×10^6	7
SnO	-1	-	6.75	6×10^3	8
SnO	-0.71	0.143	6.54	$> 10^5$	9
Cu_2O	-1.88	0.75	5.64	1.79×10^5	10
Cu_2O	-	0.19	2.7	2×10^5	11
SnO	-	0.14	7.6	3×10^4	12

Reference in supporting information

1. H.-S. Jeong, M.-J. Park, S.-H. Kwon, H.-J. Joo and H.-I. Kwon, Sens. *Actuators B Chem*., 2019, **288**, 625-633.
2. J. H. Bae, J. H. Lee, S. P. Park, T. S. Jung, H. J. Kim, D. Kim, S.-W. Lee, K.-S. Park, S. Y. Yoon, I. B. Kang and H. J. Kim, *ACS Appl. Mater. Interfaces*., 2020, **12**, 38350-38356.
3. W. K. Min, S. P. Park, H. J. Kim, J. H. Lee, K. Park, D. Kim, K. W. Kim and H. J. Kim, *ACS Appl. Mater. Interfaces*., 2020, **12**, 24929-24939.
4. A. W. Lee, D. Le, K. Matsuzaki and K. Nomura, *ACS Appl. Electron. Mater*., 2020, **2**, 1162-1168.
5. H. Chang, C. -H. Huang, K. Matsuzaki and K. Nomura, *ACS Appl. Mater. Interfaces*., 2020, **12**, 51581-51588.
6. M. Napari, T. N. Huq, D. J. Meeth, M. J. Heikkila, K. M. Niang, H. Wang, T. Iivonen, H. Wang, M. Leskela, M. Ritala, A. J. Flewitt, R. L. Z. Hoye and J. L. MacManus-Driscoll, *ACS Appl. Mater. Interfaces*., 2021, **13**, 4156-4164.
7. X. Zou, G. Fang, J. Wan, X. He, H. Wang, N. Liu, H. Long and X. Zhao, *IEEE Trans Electron Devices*., 2011, **58**, 2003-2007.
8. J. A. Caraveo-Frescas, P. K. Nayak, H. A. Al-Jawhari, D. B. Granato, U. Schwingenschlogl and H. N. Alshareef, *ACS Nano*., 2013, **7**, 5160-5167.
9. C.-W. Zhong, H.-C. Lin, K.-C. Liu and T.-Y. Huang, *IEEE Electron Device Lett*., 2015, **36**, 1053-1055.
10. W. Maeng, S.-H. Lee, J.-D. Kwon, J. Park and J.-S. Park, *Ceram*., 2016, **42**, 5517-5522.

11. A. Liu, S. Nie, G. Liu, H. Zhu, C. Zhu, B. Shin, E. Fortunato, R. Martinse and F. Shan, *J. Mater. Chem. C.*, 2017, **5**, 2524-2530.
12. C. W. Shih, A. Chin, C. F. Lu and W. F. Su, *Sci.*, 2018, **8**, 889.