Electronic Supplementary Material (ESI) for Nanoscale Horizons.

Supporting Information

Versatile Memristor for Memory and Neuromorphic Computing

Tao Guo,[a] Kangqiang Pan,[b] Yixuan Jiao,[a] ,Bai Sun,[c] Cheng Du,[a] Joel P. Mills,[a] Zuolong Chen,[a] Xiaoye Zhao,[a,d] Lan Wei,[b] Y. Norman Zhou,[a,*] and Yimin A. Wu [a,*]

[a]Department of Mechanical and Mechatronics Engineering, Waterloo Institute of Nanotechnology, University of Waterloo, Waterloo, Ontario N2L 3G1, Canada
[b]Department of Electrical and Computer Engineering, University of Waterloo, Waterloo, Ontario N2L 3G1, Canada
[c]School of Physical Science and Technology, Key Laboratory of Advanced Technology of Materials (Ministry of Education of China), Southwest Jiaotong University, Chengdu, Sichuan 610031, China
[d]State Key Laboratory of Advanced Welding and Joining, Harbin Institute of Technology, Harbin 150001, China
* Corresponding authors.
yimin.wu@uwaterloo.ca; nzhou@uwaterloo.ca

Experimental section

1.1 Device fabrication

The proposed devices were fabricated by magnetron sputtering and electrodeposition methods. The fabrication flow chart is shown in Fig. S1. Note, substrates with similar characteristics are all practicable for the fabrication process, including the silicon wafer covered by SiO_2 oxide film and some flexible substrates. The bottom Mo electrode was deposited by direct current (DC) sputtering. The patterned Mo electrode was obtained with the help of a shadow mask. The width of the strip Mo electrode was 50 μm. Then, the electrodeposition was used to deposit the CIS thin film as an active layer. For the solution preparation, 2.5 mM $CuCl_2 \cdot 2H_2O$, 240 mM LiCl, 2.4 mM $InCl_3$, 4.5 mM H_2SeO_3 were dissolved in deionized water. Chemicals were purchased from Sigma-Aldrich. The electrolytic bath was buffered with a pHydrion buffer (pH 3.00). HCl drops were used to tune the solution pH to 2 - 3.

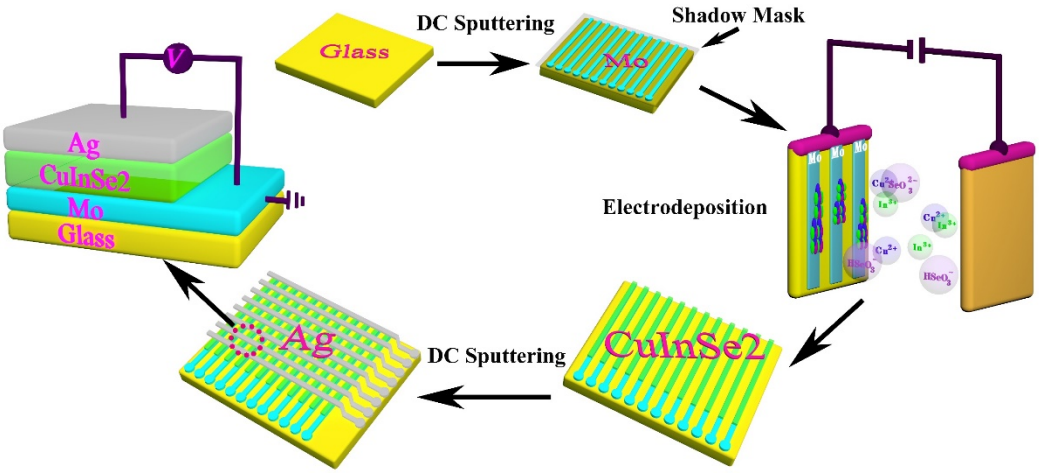

Fig. S1. The fabrication process of the Ag/CIS/Mo memristor with a crossbar configuration.

Electrodeposition was carried out using an electrochemical workstation (CHI Model 660E Series Electrochemical Analyzer/Workstation) with a conventional 3-electrode setup. During the

depositing process, a constant cathodic potential was applied to the working electrode. The deposition of compound $CuInSe_2$ (CIS) thin films is related to the individual chemical reactions, as shown in the following Nernst equations [1].

$$M^{n+} + ne^- \rightarrow M(s) \quad \text{(S1)}$$

$$Cu^{2+} + 2e^- \rightarrow Cu(s) \quad \text{(S2)}$$

$$E = E_{Cu}^0 + {}^{RT}/_{2F} \times \ln [Cu^{2+}] = 0.337 + 0.0295 \times log[Cu^{2+}] \quad \text{(S3)}$$

$$In^{3+} + 3e^- \rightarrow In(s) \quad \text{(S4)}$$

$$E = E_{In}^0 + {}^{RT}/_{3F} \times \ln [In^{3+}] = -0.342 + 0.0197 \times log[In^{3+}] \quad \text{(S5)}$$

$$H_2SeO_3 + 4H^+ + 4e^- \rightarrow Se + 3H_2O \quad \text{(S6)}$$

$$E = 0.741 - 0.0591 \times pH + 0.0148 \times log[H_2SeO_3] \quad \text{(S7)}$$

$$HSeO_3^- + 5H^+ + 4e^- \rightarrow Se + 3H_2O \quad \text{(S8)}$$

$$E = 0.778 - 0.0739 \times pH + 0.0148 \times log[HSeO_3^-] \quad \text{(S9)}$$

$$SeO_3^{2-} + 6H^+ + 4e^- \rightarrow Se + 3H_2O \quad \text{(S10)}$$

$$E = 0.875 - 0.0886 \times pH + 0.0148 \times log[SeO_3^{2-}] \quad \text{(S11)}$$

$$xM + ySe \rightarrow M_xSe_y \quad \text{(S12)}$$

Where *E* represents the electrode equilibrium potential respecting the standard hydrogen electrode. E_{Cu}^0 and E_{In}^0 are standard electrode potentials of Cu and In, respectively. *F* represents Faraday's constant that equals 96,485 C/mol. The concentration of H^+ shown in the equations is represented in a pH scale. It can be found that the electrode equilibrium is tunable by the concentrations of chemical species. Selenide compounds can directly occur due to large formation energies (△G: e.g., -386 kJ/mol for In_2Se_3, -104 kJ/mol for Cu_2Se). Generally, it is very hard to directly electrodeposit In metal from a single-bath solution. However, it is easy to co-deposit compounds, such as Cu_2Se, In_2Se_3, and $CuInSe_2$ [2].

$$2Cu^{2+} + Se + 4e^{-} \rightarrow Cu_2Se \quad \text{(S13)}$$

$$2In^{3+} + 3Se + 6e^{-} \rightarrow In_2Se_3 \quad \text{(S14)}$$

$$Cu^{2+} + In^{3+} + 2Se + 5e^{-} \rightarrow CuInSe_2 \quad \text{(S15)}$$

The cyclic voltammetry (CV) test over the range of 0 V to -1 V was carried out to study the chemical reactions in the bath. CV curves in the electrolytic bath are shown in Fig. S2. For the first cycle, the small peak at approximately -0.1 V was attributed to the reaction of Se. Then, strong peaks corresponding to the generation of Cu, CIS, and H_2 were showed up. From the second cycle to the tenth cycle, the intensity of reduction peaks was decreased, especially for the reduction of Cu and H_2. This phenomenon is because the deposited film covering the work electrodes increased the resistance [3]. Under the same potential, higher resistance corresponds to smaller current intensities. The hydrogen evolution was suppressed after the first cycle, which benefits the adhesiveness of the deposited thin film on substrates [4]. The CIS film was formed after the negative potential of -0.66 V (vs. Ag/AgCl). Therefore, the potential was set at -0.66 V for the CIS deposition.

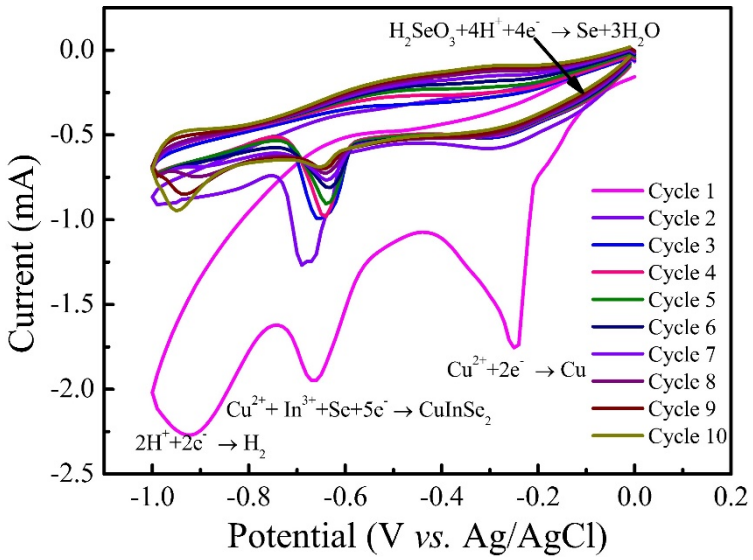

Fig. S2. Cyclic voltammetry (CV) curves in electrolytic bath for $CuInSe_2$ (CIS) deposition. The scan rate was 20 mV/s.

Since the CIS can be obtained under the negative potential of about -0.66 V (*vs*. Ag/AgCl). This voltage was used to deposit the CIS film under the model of constant cathodic potential. A representative current-time (I-t) curve is shown in Fig. S3. At the very beginning of the deposition, the absolute value of current sharply decreased from about 6 mA to 0.7 mA within 50 s. This phenomenon is due to the forming of CIS on the surface of the Mo electrode, which significantly increased the overall resistance [5]. Notably, the current remained almost constant after the first 50 s. The small current variance indicates stable electrochemical reactions and film growth. During the electrodeposition, two phases contribute to the interface that film growth occurs [6]. One phase is the solution carrying ions towards the working electrode. Another phase is the boundary of the substrate covering conductive coating that carries electrons. When the potential of the working electrode shifts from the equilibrium values to negative potentials. The reduction reactions of ions conveyed by the solution occur if a suitable potential is provided [7]. This working mechanism determines that only the areas covered by Mo electrodes can grow CIS film, enabling the direct construction of active layers on specific patterns [8]. The deposition rate was approximately 23 nm/min. CIS film only grew on the patterned bottom electrode. Decreasing manufacturing costs and materials consumption are crucial for practical large-scale production. Expensive vacuum-based film deposition techniques are used to fabricate memristor devices, such as magnetron sputtering, atomic layer deposition (ALD), and thermal evaporation. The expensive equipment significantly increases manufacturing costs. Regarding materials utilization in vacuum-based deposition techniques, most of the materials are deposited on the surface of chambers instead of wafers. To address the issues, the electrodeposition endows remarkable advantages in terms of costs, deposition rates, morphology control, film uniformity, and template-based structure fabrication [6]. Moreover, this method enables high utilization efficiency of materials because all reacted elements are utilized to form films. This technique paves a way to construct integration

arrays with high materials utilization efficiency and low manufacturing costs.

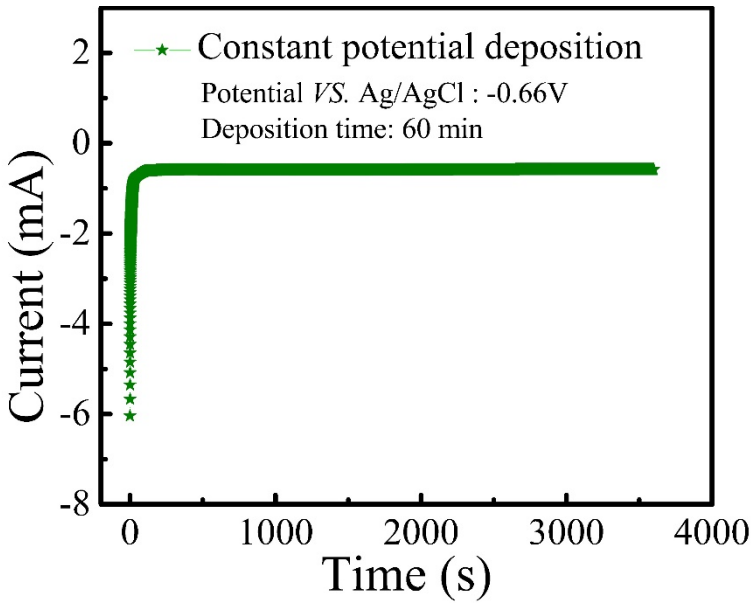

Fig. S3. Electrodeposition current versus time during the depositing process. This is one of the typical I-t curves. The deposition time is 60 min. The potential VS. Ag/AgCl was -0.66V. The current remains almost constant after 50 s. This small current variance indicates stable electrochemical reactions and film growth.

After the deposition of CIS active layer, Ag strip electrodes were deposited with the help of a shadow mask to form a crossbar configuration.

1.2 Materials and device characterization

The optical micrograph was taken by an Oxford BX51M optical microscope and measurements were carried out by the ImageJ software. The morphology of CIS films was examined by Scanning Electron Microscopy (SEM, UltraPlus FESEMs) at the acceleration voltage of 10 kV. The composition of the thin film was measured by Energy Disperse Spectroscopy (EDS, UltraPlus FESEMs). To analyze the crystal structure of deposited films, Raman spectrum analysis was carried

out by a Renishaw micro-Raman spectrometer with a laser wavelength of 633nm (red, He-Ne). Grazing Incidence Xray Diffraction (GIXRD) on the CIS thin film was carried out using PANalytical X'Pert PRO system ($Cu_{K\alpha}$ irradiation, λ = 1.5406 Å). The surface valence states of the CIS thin film were measured by X-ray photoelectron spectroscopy (XPS, Thermo-VG Scientific ESCALab 250). The electrical characterization of the prepared devices was performed with a 4200A-SCS Parameter Analyzer equipped with the probe station of MPI TS150. The test diagram can be found in Fig. S1.

1.3 Simulation method

Simulation method for LIF neuron: The circuit was designed to demonstrate the functionalities of the leaky integrate-and-fire (LIF) neurons based on the Ag/CIS/Mo device. The theoretical model of the Ag/CIS/Mo device was developed in Verilog-A based on experimental data under the volatile model. The key parameters were extracted from experimental data, including HRS, LRS, V_{SET}, V_{RESET}. The model can capture the resistive switching and volatile features of the actual device. The simulation and experimental results are shown in Fig. S4. The code script for Verilog-A is shown in Fig. S5. The volatile memristor model was used in the leaky integrate-and-fire (LIF) neuron circuit built up in the Cadence Virtuoso platform. The neuron circuit design is shown in Fig. S6. Three artificial synapses were integrated into the circuit. A capacitor, a resistor, and an Ag/CIS/Mo memristor were used to mimic the function of neurons. The specifications of components employed in the circuit are listed in Table S2.

Based on the experimental data of the volatile model, an electrical model of the Ag/CIS/Mo device is developed in Verilog-A. The key parameters were extracted from experimental data. The HRS and LRS were 300 GΩ and 2 MΩ, respectively. The V_{SET} and V_{RESET} were 0.8 V and 0.2 V, respectively. The resistance of the memristor switches to LRS when the voltage across the memristor reaches 0.8 V (V_{SET}). The device switches from LRS to HRS when the applied voltage is

lower than 0.2 V (V_{RESET}). When the device is at the HRS, it is assumed that the resistance of the device does not change until the applied voltage reaches the V_{SET}. Therefore, the resistance increased linearly with the increase of the applied voltage (0 V → V_{SET}). Similarly, the resistance of the device at the LRS does not change until the applied voltage is lower than the V_{RESET} (threshold voltage). The resistance decreased linearly with the decrease of the applied voltage (1 V → V_{RESET}). The switching speed is 400 μs, which is negligible in the circuit simulation implemented in this paper. Therefore, the transition time was ignored to simplify the model and circuit. The goal of this model is to describe the I-V curve of the device mathematically, which is valid in the circuit simulation executed in the Cadence Virtuoso platform. As shown in Fig. S4, the model captured the resistive switching and volatile features of the actual device, which was used in the simulation of the leaky integrate-and-fire (LIF) neuron circuit.

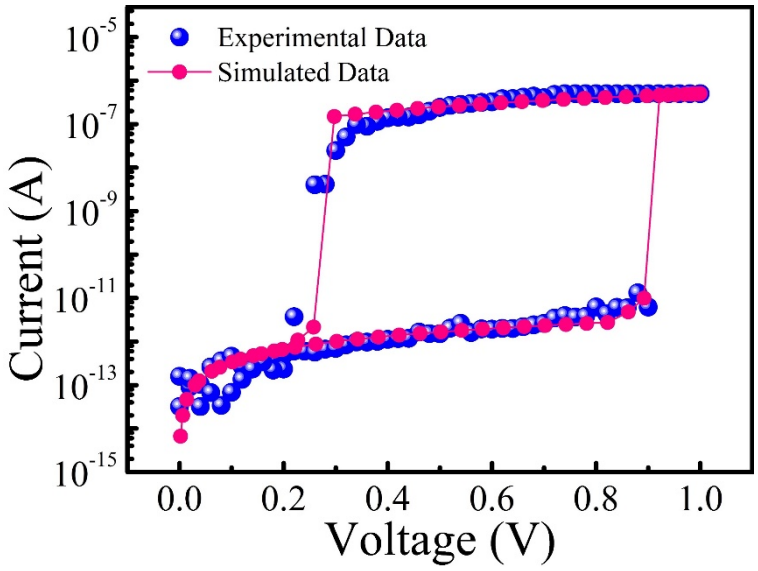

Fig. S4. Experimental and simulated I-V curve of the device under the volatile model. The I-V curves of simulation and experiment match well, indicating that the theoretical model can effectively describe the electronic performance of the Ag/CIS/Mo device.

Fig. S5 shows the Verilog-A code of the volatile memristor behavioural model. By default,

the device is at HRS without the external voltage bias. As the forward bias voltage exceeds the V_{SET} defined in the model, the device enters LRS and remains in this state if the external voltage bias stays above the V_{RESET} (the threshold voltage). On the other hand, if the external voltage bias drops below the V_{RESET} (the threshold voltage), the memristor returns to HRS. This method can mathematically present the electronic behaviours of the device Ag/CIS/Mo.

```
// VerilogA for rram, Ag-CIS-Mo, veriloga

`include "constants.vams"
`include "disciplines.vams"

module rram (a, c);

    inout a, c;
    electrical a, c;

    parameter real r_lrs = 2e6    from (0:inf); // Resistance in LRS
    parameter real r_hrs = 3e11   from (0:inf); // Resistance in HRS
    parameter real v_on  = 0.8    from (0:inf); // SET voltage
    parameter real v_off = 0.2    from (0:inf); // RESET voltage
    parameter real t_on  = 10e-6     from (0:inf); // HRS --> LRS Transition
    parameter real t_off = 200e-6     from (0:inf); // LRS --> HRS Transition
    parameter real t_hold = 200e-6     from (0:inf); // State holding time

    real prev_v;
    real r;
    real r_target;
    real t_tran;
    real t_delay;

    analog begin
        @(initial_step)  begin
            prev_v = 0;
            r = r_hrs;
            r_target = r_hrs;
            t_tran = t_off;
        end

        if ( V(a,c)>=0.8 && V(a,c)>=prev_v && r==r_hrs)
            begin
                r_target = r_lrs;
                t_tran  = t_on;
                t_delay = 0;
            end

        else if ( V(a,c)<=0.3 && V(a,c)<=prev_v && r==r_lrs )
            begin
                r_target = r_hrs;
                t_tran = t_off;
                t_delay = t_hold;
            end

        r = transition(r_target,t_delay,t_tran,t_tran);

        I(a,c) <+ V(a,c)/r;
        prev_v = V(a,c);
    end

endmodule
```

Fig. S5. Verilog-A code modelling the volatile memristive behaviour of the Ag/CIS/Mo device.

The neuron circuit design is shown in Fig. S6. Three artificial synapses are attached to the circuit. To model inputs with tunable synaptic weights to neurons, the values of V_{IN} (V_{IN1}, V_{IN2}, V_{IN3}) and corresponding R (R_1, R_2, R_3) can be adjusted. Here, to simplify the operation model, the value of R (*R1*, *R2*, *R3*) was fixed, and the value of V_{IN} (V_{IN1}, V_{IN2}, V_{IN3}) was adjusted. Ideal switches (*SW1*, *SW2*, *SW3*) were used in the simulation. The switches are closed only if the corresponding input V_{IN} > 0 V, which can avoid interference between different inputs. The specifications of components employed in the circuit are listed in Table S2.

In the neural network, neurons receive synaptic inputs with various frequencies (2.5 KHz to 10 KHz) and amplitudes (0.8 V to 1.2 V). By default, the volatile memristor *M1* was at HRS and *SW4*

was open. During this period, the received inputs are stored and accumulated in the capacitor, resulting in the increased potential (V_C) stored on the capacitor and (local graded potential) LGP that reflects the dynamics of the neural membrane potential. V_C can be calculated by Eq. (S16).

$$V_C = \frac{1}{C}\int I\,dt \quad \text{(S16)}$$

Where *I* represents input currents, *C* is the capacitance of the capacitor *C1.* Meanwhile, the charge stored in the capacitor slowly leaks through a conductive path consisting of *M1* and *R4*. The leakage *RC* time constant (τ), is determined by *C1, M1*, and *R4,* according to Eq. (S17) [9].

$$\tau = C \times (R_{M1} + R_4) \quad \text{(S17)}$$

Where R_{M1} is the resistance of the *M1*. V_{OUT} can be calculated from V_C using Eq. S18 [10].

$$V_{OUT} = V_C \times \frac{R_4}{R_{M1} + R_4} \quad \text{(S18)}$$

V_{OUT} is the voltage on the R_4. The voltage on the memristor (*M1*) can be obtained with Eq. S19.

$$V_{memristor} = V_C - V_{OUT} \quad \text{(S19)}$$

Where $V_{memristor}$ is the voltage applied on the memristor (*M1*). *R4* has a resistance of 4 MΩ that is much smaller than that of *M1* at HRS with a resistance of 300 GΩ. V_{out} ≈ 0V when *M1* is at HRS according to Eq. S18. As more and more electrons are stored in the capacitor, V_C and $V_{memristor}$ keep increasing provided that the charging speed is faster than the leaky speed. When the $V_{memristor}$ is high enough, the *M1* will be switched from HRS to LRS, which will induce the abrupt increase of the V_{OUT}. As M1 enters LRS and a non-zero V_{OUT} is generated, *C1* is rapidly discharged, and the V_C decreases to 0 V. As the V_C drops below the RESET voltage of 0.2 V, *M1* resumes to HRS due to the volatile property. As a result, V_{OUT} returns to 0 V as *C1* starts to accumulate charges from input signal again. Notice that during the period when M1 stays in LRS, any incoming signals stored in *C1*

is rapidly discharged immediately. This feature can mimic the refractory period in biosystems.

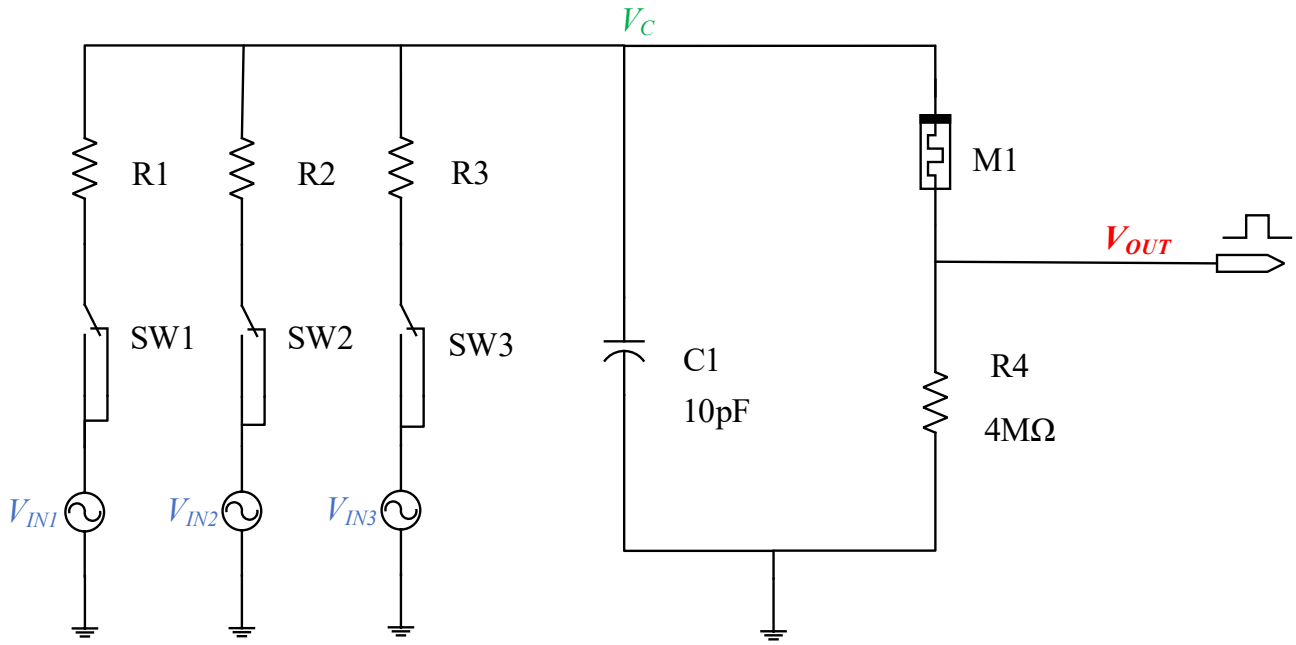

Fig. S6. Circuit design for the simulation of artificial leaky integrate-and-fire (LIF) neurons. The simulation was carried out in the Cadence Virtuoso platform. *SW1-4* are switches. *R1-4* are resistors. *M1* is a threshold switching (TS) memristor.

Pattern recognition simulation The recognition simulation was carried out on the CrossSim platform written with Python.[11–13] The numerical weights in the network were mapped onto the tested device conductance states. The non-linearity and asymmetry of potentiation/depression curves were taken into account. The cycle-to-cycle variability was considered as Gaussian noise during the simulation process. The conductance (weight) updating was based on the average value of conductance change (under a single pulse) with different initial conductance (G_0). A neural network with the size of 64 × 40 × 10 was constructed to implement a backpropagation algorithm. The UCI small images were used as data set for training and testing processes[14]. The neural network was trained for 30 epochs to get a saturated accuracy.

Supplementary Figures:

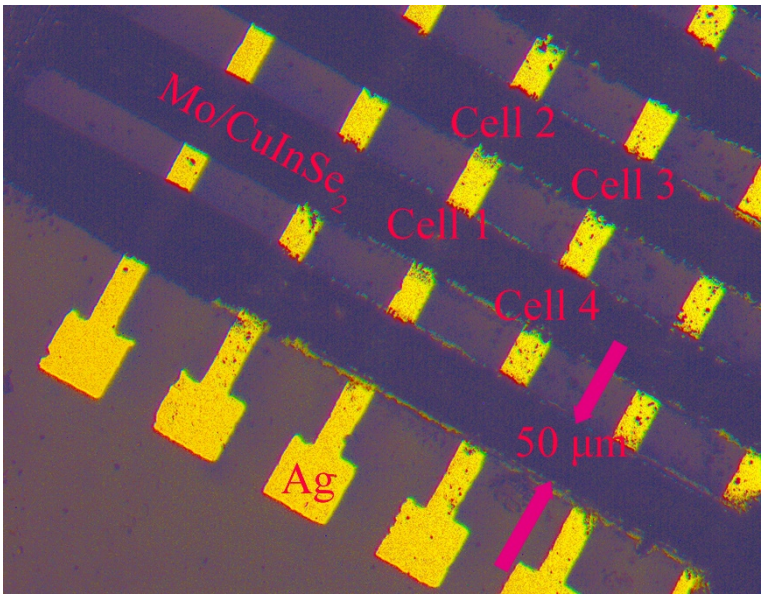

Fig. S7. Optical micrograph of the device with a crossbar array configuration.

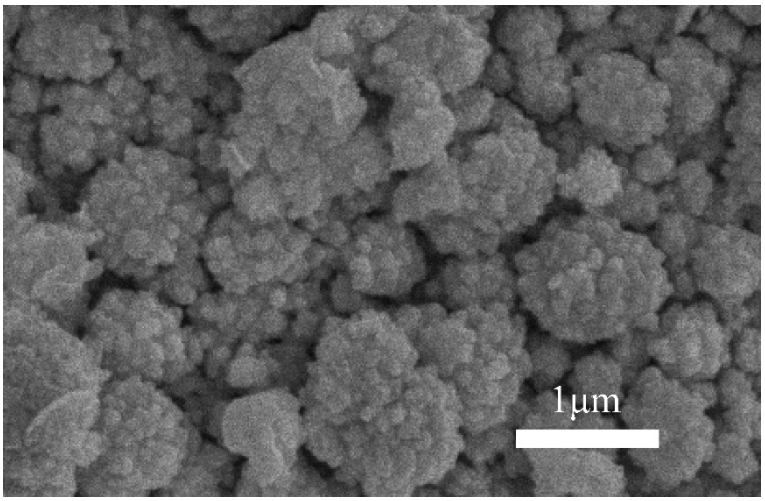

Fig. S8. Scanning electron microscope (SEM) image of the $CuInSe_2$ surface topography. The CIS grains grew into a follower-like shape consisting of small grain particles with a size of about 100 nm [2].

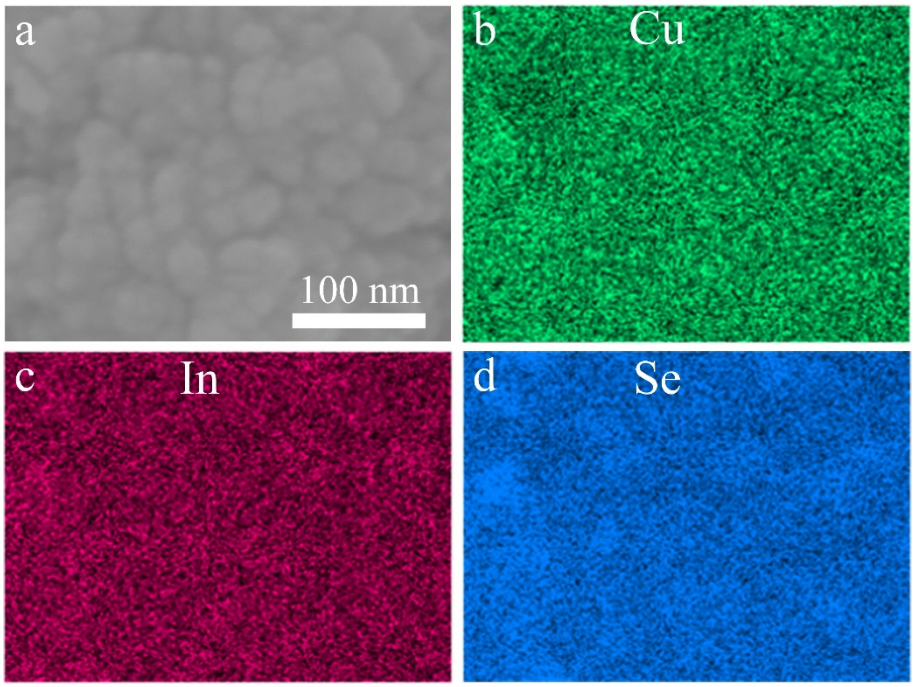

Fig. S9. (a) High-resolution SEM image of the $CuInSe_2$. (b-d) Surface composition EDX mapping corresponding to Cu, In, Se elements respectively.

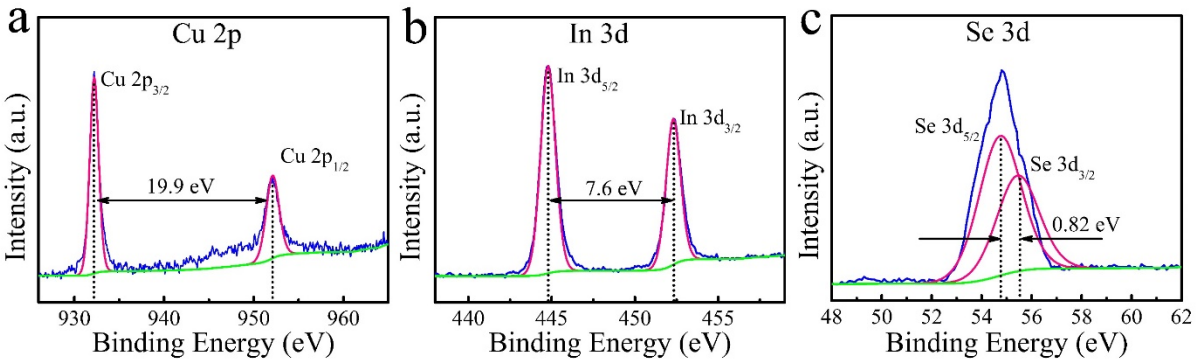

Fig. S10. High-resolution XPS spectra of different regions: (a) Cu 2p region; (b) In 3d region; (c) Se 3d region. The results confirm the chemical states of Cu, In, Se are +1, +3, -2, respectively [15].

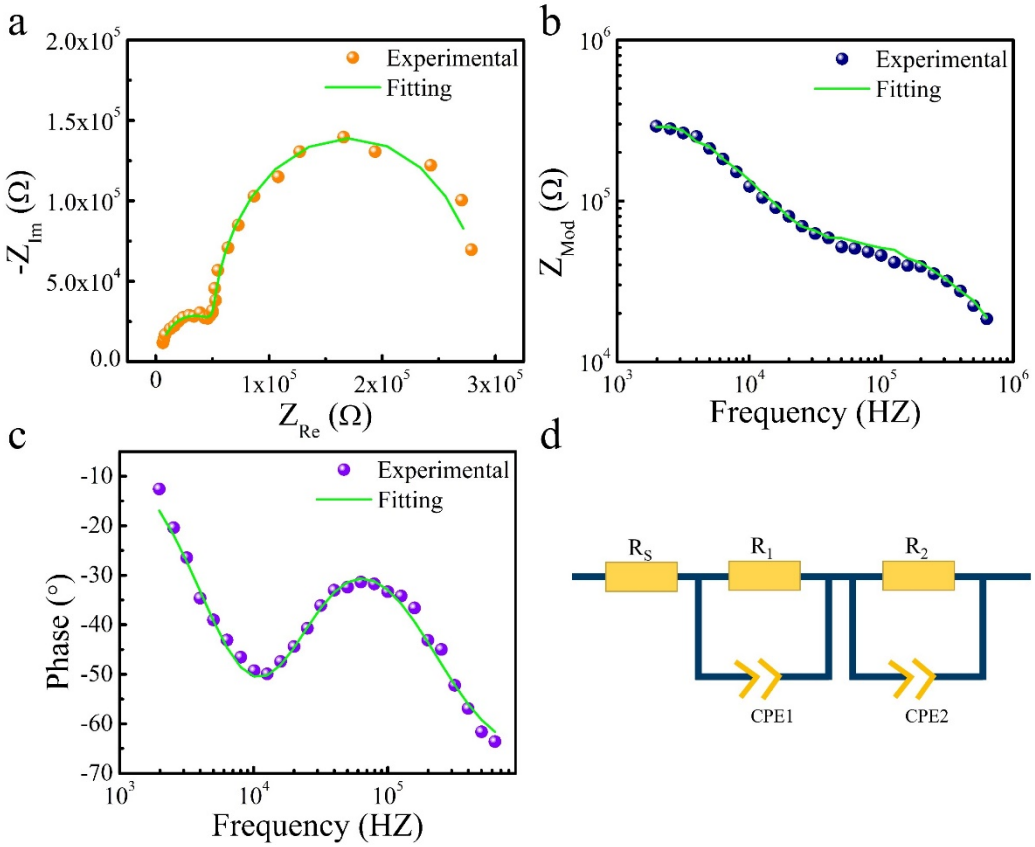

Fig. S11. Impedance analysis of the fabricated CIS. (a) Nyquist plot of CIS at room temperature. (b) The plot of the Modulus *vs* Frequency. (c) The plot of the Phase vs Frequency. (d) The equivalent circuit for fitting.

We measured the permittivity ε of CIS deposited by the electrodeposition process. The permittivity ε was 7.9. The value slightly deviated from the reported result of 13.6 ± 0.8[16]. Notably, the electronic properties, such as permittivity, conductance, are determined by the composition, crystallinity, and fabrication process of CIS. The reported permittivity of CIS was based on fabricated ingots by a horizontal zone-melting technique. The difference in the status of material can result in slightly differential permittivity values.

To get the permittivity ε of CIS, the electrochemical impedance spectroscopy (EIS) of the CIS was measured based on the Mo/CIS/Mo device. The Nyquist plot and the fitting curve are shown in Fig. S11a. The Bode plots and fitting curves of modulus (|Z|) *vs.* frequency (*f*) and phase *vs.* frequency (*f*) are shown in Fig. S11b and c. According to the Nyquist plot (Fig. S11a), two separated semicircles were observed, corresponding to the bulk capacitor and the grain boundary capacitor.[17] The equivalent circuit for fitting is shown in Fig. S11d. The constant-phase elements (CPE) are

described with Equation S20:[18]

$$Z_{CPE} = \frac{1}{Q(j\omega)^n} \qquad \text{(S20)}$$

Where Z_{CPE} is the impedance of the CPE. Q is a constant. *j* represents the imaginary number. ω represents the angular frequency (ω = 2 *πf*, *f* is the frequency). *n* represents a constant relating to the angle of a capacitive line's rotation on complex plane plots. Rs is the series resistor that corresponds to the series resistance on electrodes. The fitting process was executed on the ZView2 software. The solid lines shown in Fig. S11 are the fitting curves that match well with experimental results. According to the fitting results, the capacitance can be calculated by the following Equation S21:[19]

$$C = (R^{1-n}Q)^{\frac{1}{n}} \qquad \text{(S21)}$$

Where *C* is capacitance, *R* is the resistance value of parallel resistance. n and Q are fitting parameters from Equation S21. The assignment of the two semicircles was based on the magnitude of the capacitance.[17] According to the "brickwork" model, the capacitance value derived from bulk (grain) falls in the order of 10^{-10}F (i.e *l*/*A*=1 m^{-1}, where *l* is the thickness of the dielectric materials sandwiched by metal electrodes, A is the device area. The typical permittivity is ~ 10). Meanwhile, the capacitance value derived from grain boundary ranges from 10^{-9} F to 10^{-6} F. According to the fitting parameters, the C1 (based on R1//CPE1) was 6.0 × 10^{-11} F that corresponds to the bulk (grain) capacitor. The C2 (based on R2//CPE2) was 2.3× 10^{-9} F that corresponds to the grain boundary capacitor. The permittivity is calculated with Equation S22:[20]

$$\varepsilon = \frac{4\pi KdC}{S} \qquad \text{(S22)}$$

Where ε is permittivity. K is electrostatic constant. d is the thickness. S is the area.

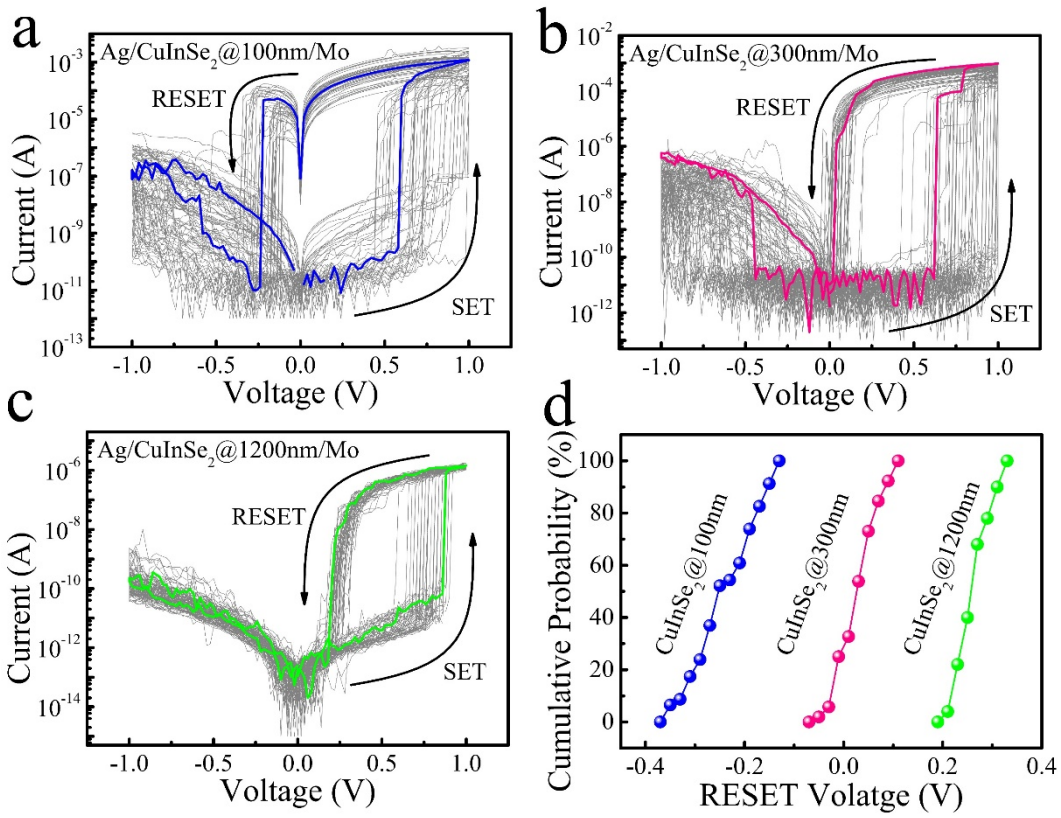

Fig. S12. I-V curves and RESET voltage change over different thicknesses of CIS layers. Each device operated 50 cycles. (a) I-V curves of the device Ag/CIS@100nm/Mo. (b) I-V curves of the device Ag/CIS@300nm/Mo. (c) I-V curves of the device Ag/CIS@1200nm/Mo. (d) The cumulative probabilities of the RESET voltages for the devices with different CIS thicknesses.

Under the same voltage stress, the devices evolved from non-volatile to volatile characteristics gradually when increasing the thickness of CIS [21]. To further investigate the evolution from the volatile to non-volatile performance, the devices with different thicknesses of CIS were fabricated and tested under the same voltage stress (-1 V to 1 V) as shown in Fig. S12. The device with CIS@100nm showed a non-volatile characteristic since a negative voltage was required to switch the device to HRS, as shown in Fig. S12a. In comparison, the device with CIS@300nm and CIS@1200nm showed volatile characteristics, devices RESET to HRS spontaneously when the voltage was near to zero, as shown in Fig. S12 b and c. Note, the device with CIS@1200nm showed

a higher RESET voltage comparing to that of the device CIS@300nm, which means that the device with CIS@1200nm was easier to RESET to HRS and the conductive filaments are less stable. Fig. S12d presented that the RESET voltages moved to the positive direction with the increase of the CIS thickness, demonstrating an evolution from non-volatile to volatile characteristics [21].

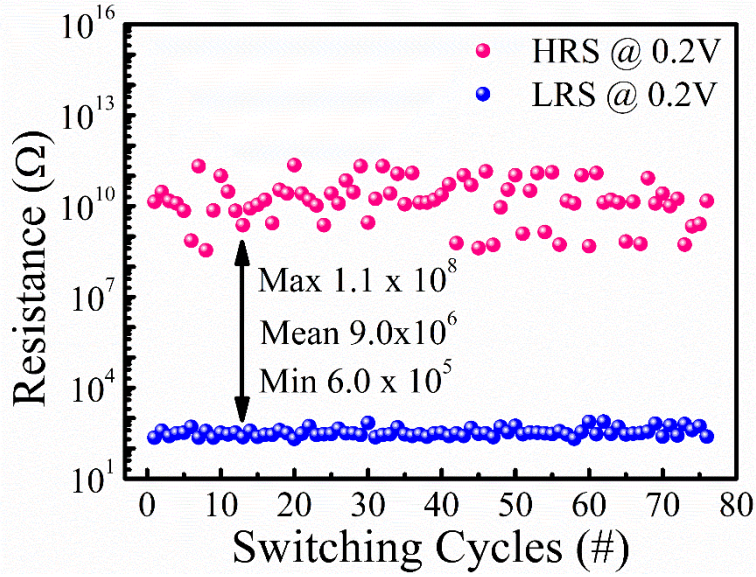

Fig. S13. HRS and LRS resistance distributions over 400 switching cycles.

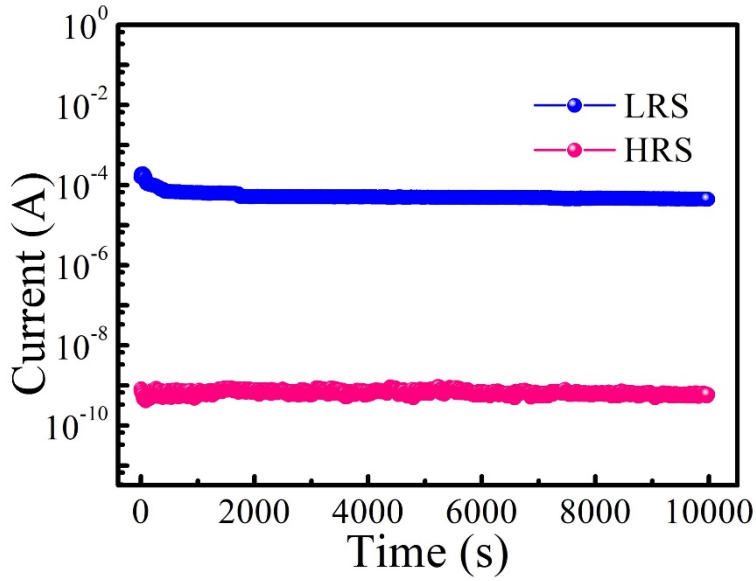

Fig. S14. Non-volatile memory behavior, the voltage amplitude was 3 V, the pulse duration was 1s. The LRS can be maintained for over 10,000 s, demonstrating non-volatile performance. The device

can be used to develop non-volatile data storage devices.

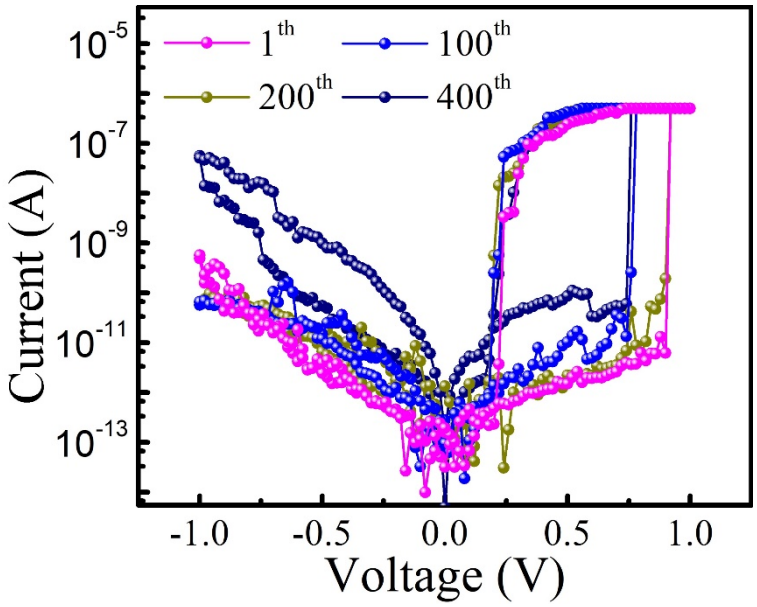

Fig. S15. I-V curve reproducibility of the device over 400 switching cycles.

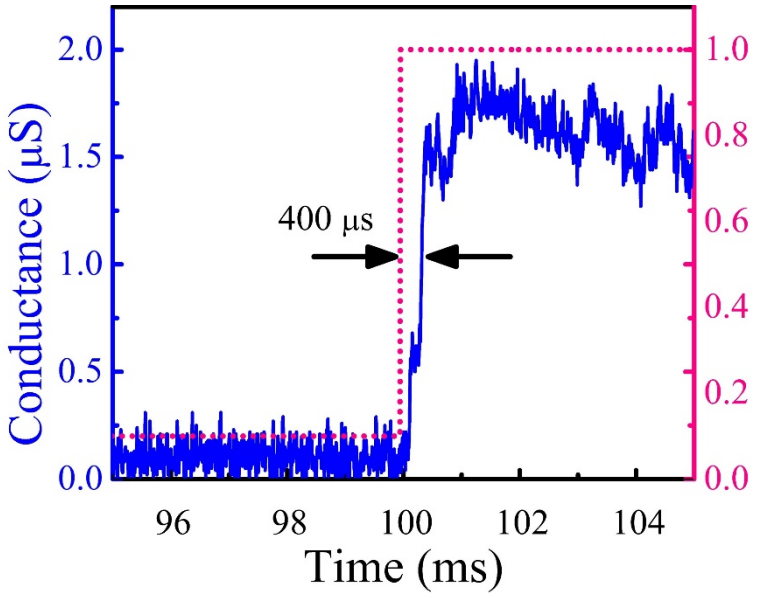

Fig. S16. The switching speed characterization of the device. A short voltage pulse with an amplitude of 1 V was applied to the device. The current flowing through the device was monitored. The sharp increase of conductance indicates a switching speed of 400 μs was obtained.

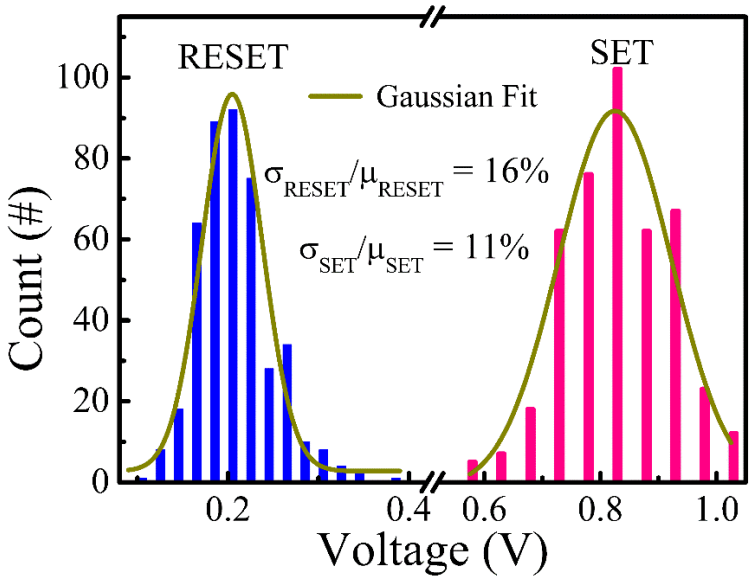

Fig. S17. The distribution of SET and RESET voltages. The σ_{SET} (and σ_{RESET}) and μ_{SET} (and μ_{RESET}) are the standard deviation and the mean value, respectively. The σ_{SET}/μ_{SET} and $\sigma_{RESET}/\mu_{RESET}$ are 11 % and 16 %, respectively. The small variability of the operation voltages will benefit the stability and reliability of the systems based on the proposed device.

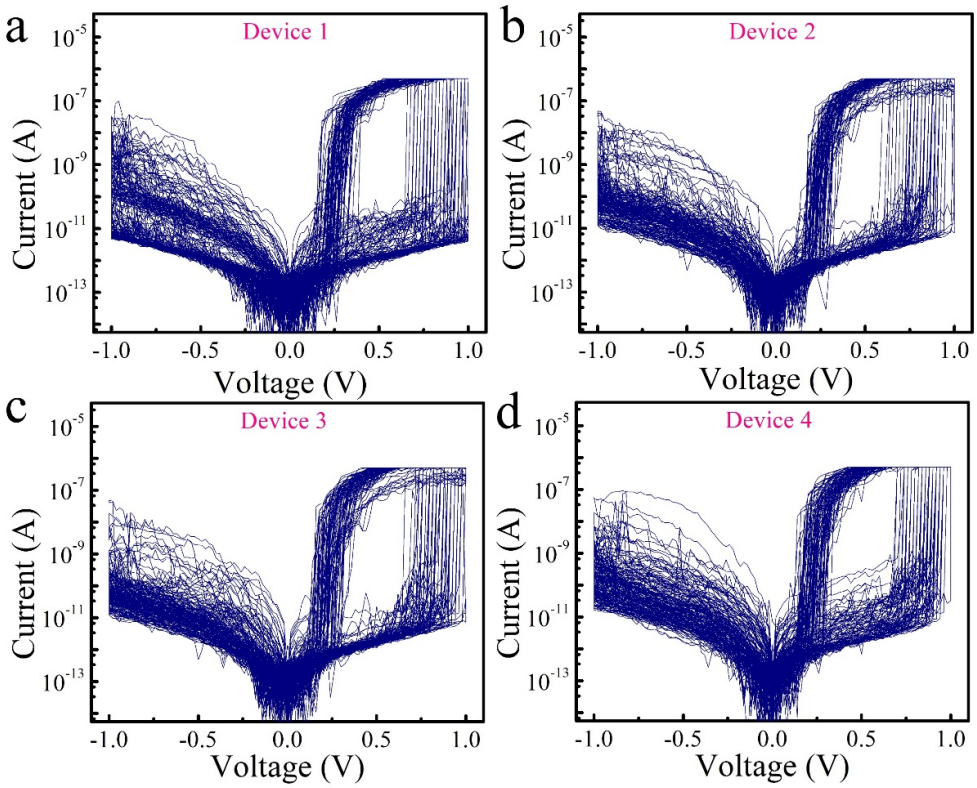

Fig. S18. (a-d) The I-V curve reproducibility of four different devices over 100 switching cycles.

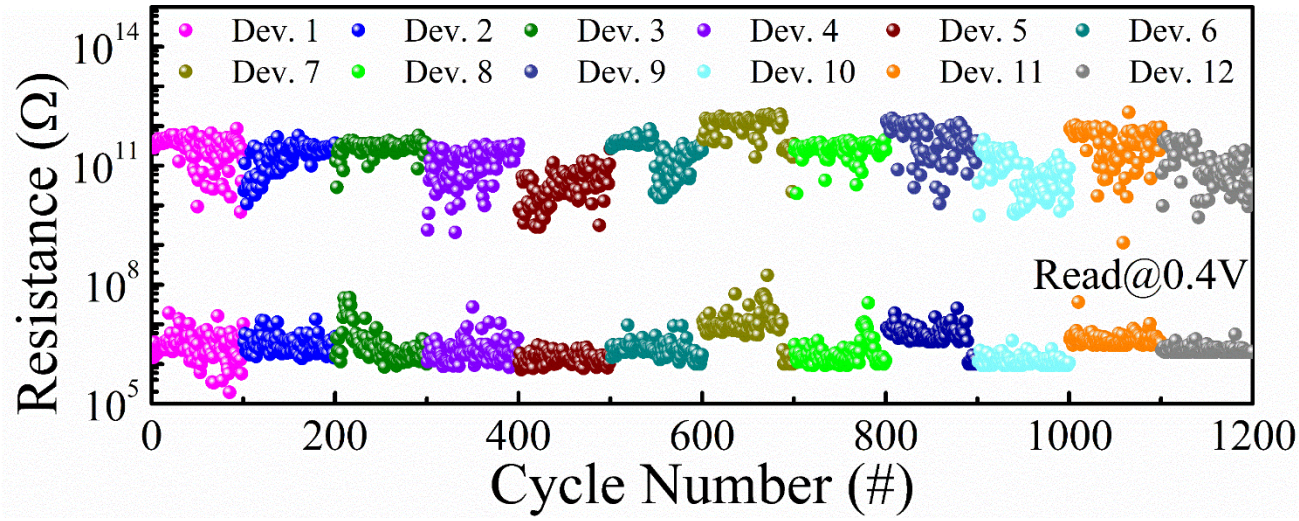

Fig. S19. (a) Device-to-device variability of HRS and LRS. The mean ratio of HRS/LRS varies between 3.4×10^4 and 1.7×10^5.

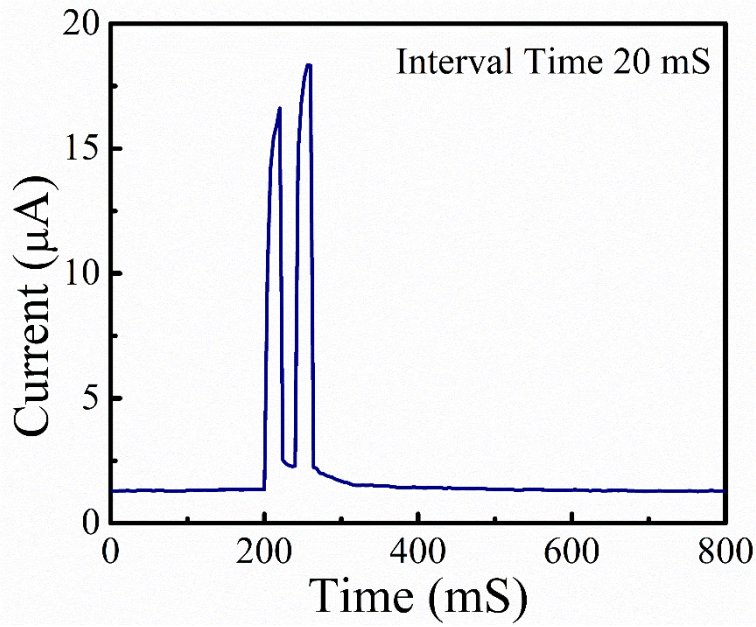

Fig. S20. The typical current curve under two consecutive pulses. The second pulse induced a larger conductance increase. Besides, the conductance returned to its original state gradually after the pulsed excitation, which is consistent with the reported result.[11]

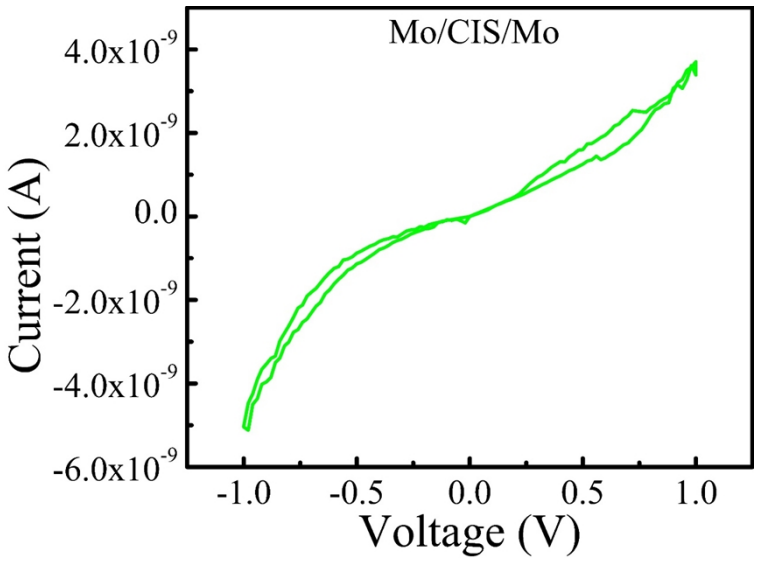

Fig. S21. Typical I-V curve of the Mo/CIS/Mo device with the size of 50 μm × 50 μm. The electrical performance of the device with inert top Mo electrodes was measured. Almost no resistive switching phenomenon was found, which is significantly different from the device with the Ag electrode. The result confirms that Ag is essential for resistive switching.

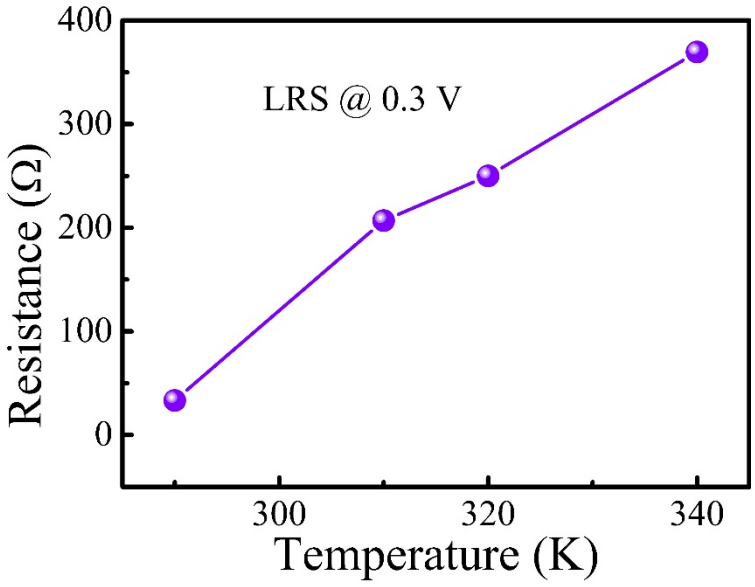

Fig. S22. The values of LRS at different temperatures for the Ag/CIS/Mo device. The resistance of LRS increased with the increase of temperature. This phenomenon is the signature feature of metallic conducting, claiming that the metallic Ag conductive filaments formed in the active layer at LRS [22].

The distribution of the RESET voltages with different thicknesses of CIS layers is shown in Fig. S23. The mean values of RESET voltage were -0.21 V, 0.04 V, and 0.26 V for the devices with CIS thicknesses of 100 nm, 300 nm, and 1200 nm, respectively. The diffusion of Ag atoms can be described by the overdamped Langevin Eq. (S23) [23].

$$\eta\frac{dx_i}{dt} = \alpha\frac{V(t)}{L} - \frac{\partial U(x_i)}{\partial x_i} + \sqrt{2\eta k_B T}\xi_i \quad \text{(S23)}$$

where η represents the viscosity of Ag nanoparticles in the system. The first term on the right-hand side is the drift term determined by applied voltages *V(t)* and the thickness of active layers L. α is the charge induced by voltages, which can be treated as a constant. *V(t)* is the applied voltage at the time of *t*. The second term on the right-hand side describes the diffusion of Ag atoms from conductive filaments due to the surface energy minimization. $\partial U(x_i)$ is the potential profile that drives the dynamic diffusion of Ag atoms. x_i is the location of Ag nanoparticles. The third term describes the random force driven by instantaneous temperatures. k_B represents Boltzmann's constant. *T* is the temperature. ξ_i is a Gaussian white noise generator describing the temperature fluctuation. In the same materials system with different CIS thicknesses, the Ag atoms diffusion speed is mainly affected by the term $\alpha \times V(t)/L$. For the thinner CIS, the value of V(t)/L is larger, indicating a higher speed of Ag atom diffusion, and more Ag atoms are pumped into the active layers [24]. Moreover, a shorter conductive filament is needed to connect the top and bottom electrodes since the active layer is thinner. Therefore, a thicker conductive is more likely induced in the device with thin active layers, demonstrating better stability and a longer lifetime. This theory can explain the evolution phenomenon of non-volatile/volatile characteristics in devices with different CIS thicknesses. The thickness-modulated volatile/non-volatile memristor has also been reported in the HfO_2-based material system [25].

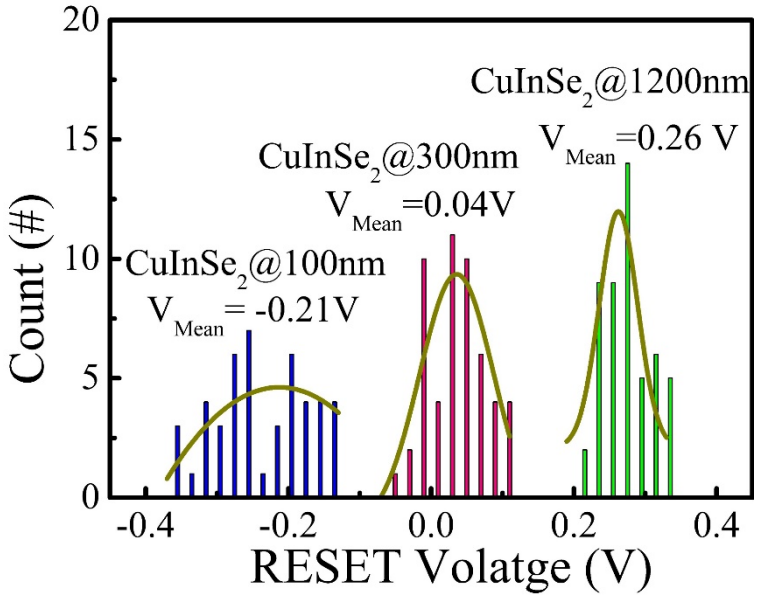

Fig. S23. Distribution of the RESET voltages of the device with different CIS thicknesses. The RESET voltage evolved to the negative direction as the CIS thickness was decreased. The values of RESET voltages changed from -0.21 V to 0.26 V when the CIS thickness increased from 100 nm to 1200 nm.

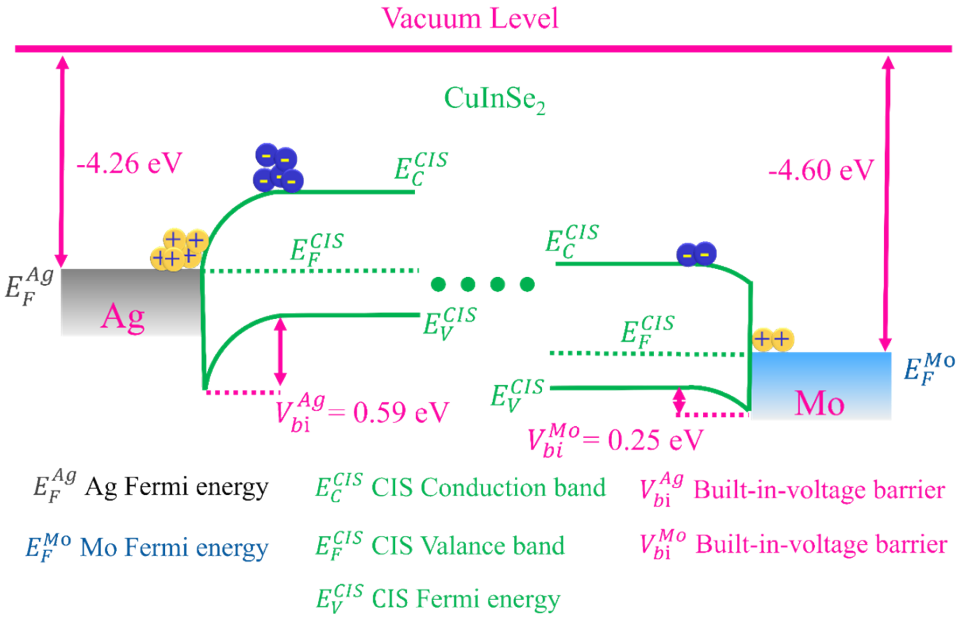

Fig. S24. Schematic diagram of energy band alignment of the Ag/CIS/Mo device. A relatively high Schottky barrier height (0.59 eV) was formed at the interface of Ag/CIS, demonstrating a Schottky contact. In comparison, an Ohmic contact occurred at the interface of Mo/CIS due to a small barrier of 0.25 eV [26,27].

Supplementary Tables:

Table S1. The statistics summary of the HRS/LRS Ratio of the Ag/CIS/Mo device.

Device Number	HRS/LRS Ratio Mean value	HRS/LRS Ratio Maximum value	HRS/LRS Ratio Minimum value	HRS/LRS Ratio Higher than 10^4 (%)
Device 1	1.7×10^5	1.7×10^6	2.5×10^3	95 %
Device 2	8.0×10^4	2.1×10^5	2.2×10^3	95 %
Device 3	1.3×10^5	4.8×10^5	5.0×10^3	96 %
Device 4	8.7×10^4	3.4×10^5	1.6×10^3	93 %
Device 5	3.4×10^4	1.6×10^5	1.5×10^3	76 %
Device 6	1.6×10^5	2.7×10^5	7.4×10^3	97 %
Device 7	1.3×10^5	2.7×10^5	7.1×10^3	98 %
Device 8	1.7×10^5	4.0×10^5	7.0×10^3	98 %
Device 9	1.2×10^5	4.2×10^5	2.5×10^3	93 %
Device 10	8.1×10^4	4.9×10^5	4.3×10^3	90 %
Device 11	1.3×10^5	6.2×10^5	3.8×10^2	94 %
Device 12	7.1×10^4	2.7×10^5	2.5×10^3	89 %

Table S2. Component parameters used in the LIF neuron simulation.

Component parameter	Frequency Simulation	Amplitude simulation
V_{IN1}	Amplitude = 1 V Period = 400 µs (2.5 KHz) Pulse width = 3 µs Delay = 0.3 ms	Amplitude = 0.8 V Period = 100 µs (10 KHz) Pulse width = 3 µs Delay = 0.3 ms
V_{IN1}	Amplitude = 1V Period = 200 µs (5 KHz) Pulse width = 3 µs Delay = 6.7 ms	Amplitude = 1V Period = 100 µs (10 KHz) Pulse width = 3 µs Delay = 3.3 ms
V_{IN3}	Amplitude = 1 V Period = 100 µs (10 KHz) Pulse width = 3 µs Delay = 13.1 ms	Amplitude = 1.2 V Period = 100 µs (10 KHz) Pulse width = 3 µs Delay = 6.3 ms
R1, R2, R3	140 MΩ	150 MΩ
M1	LRS resistance = 2 MΩ with V_{SET} = 0.8V HRS resistance = 300 GΩ Transition time from LRS to HRS, 400 µs Transition time from HRS to LRS, 10 µs	
SW1, SW2, SW3	Ideal switches that are closed only if the corresponding V_{IN} is not at 0 V. They are used for simulating a current injection.	

Reference

1 R. N. Bhattacharya, M.-K. Oh and Y. Kim, *Sol. Energy Mater Sol. Cells*, 2012, **98**, 198–202.
2 R. N. Bhattacharya, *J. Electrochem. Soc.*, 2010, **157**, D406.
3 M. A. Contreras-Ruiz, A. Mendez-Blas and Ma. E. Calixto, *J. Solid State Electrochem.*, 2021, 25, 591-601
4 P. U. Londhe, A. B. Rohom, R. Fernandes, D. C. Kothari and N. B. Chaure, *ACS Sustainable Chem. Eng.*, 2018, **6**, 4987–4995.
5 B. Lara-Lara and A. M. Fernández, *J Mater. Sci: Mater. Electron.*, 2016, **27**, 5099–5106.
6 W. Schwarzacher, *Electrochem. Soc. Interface*, 2006, **15**, 32–33.
7 C. Hubert, N. Naghavi, O. Roussel, A. Etcheberry, D. Hariskos, R. Menner, M. Powalla, O. Kerrec and D. Lincot, *Prog. Photovolt.: Res. Appl.* 2009, **17**, 470–478.
8 Y. Chen, W. He, X. Chen, C. Wang, Z. Tao, S. Wang, G. Zhou and M. Moshrefi-Torbati, *Electrochim. Acta*, 2014, **120**, 293–301.
9 S. Westerlund and L. Ekstam, *IEEE Trans. Dielectr. Electr. Insul.*, 1994, **1**, 826–839.

10 N. Kipnis, *Sci & Educ*, 2009, **18**, 349–382.
11 Y. van de Burgt, E. Lubberman, E. J. Fuller, S. T. Keene, G. C. Faria, S. Agarwal, M. J. Marinella, A. A. Talin and A. Salleo, *Nat. Mater.*, 2017, **16**, 6.
12 E. J. Fuller, F. E. Gabaly, F. Léonard, S. Agarwal, S. J. Plimpton, R. B. Jacobs-Gedrim, C. D. James, M. J. Marinella and A. A. Talin, *Adv. Mater.*, 2017, **29**, 1604310.
13 S. Agarwal, R. B. Jacobs Gedrim, A. H. Hsia, D. R. Hughart, E. J. Fuller, A. A. Talin, C. D. James, S. J. Plimpton and M. J. Marinella, in *2017 Symposium on VLSI Technology*, 2017, pp. T174–T175.
14 Dua, D. and Graff, C. (2019). UCI Machine Learning Repository [http://archive.ics.uci.edu/ml]. Irvine, CA: University of California, School of Information and Computer Science.
15 Y. Zhao, S. Yuan, D. Kou, Z. Zhou, X. Wang, H. Xiao, Y. Deng, C. Cui, Q. Chang and S. Wu, *ACS Appl. Mater. Interfaces*, 2020, 10.
16 P. W. LI, R. A. Anderson and R. H. Plovnick. *J. Phys. Chem. Solids*, 1979, 40, 333-334.
17 J. T. S. Irvine, D. C. Sinclair and A. R. West, *Adv. Mater.*, 1990, **2**, 132–138.
18 J.-B. Jorcin, M. E. Orazem, N. Pébère and B. Tribollet, *Electrochimica Acta*, 2006, **51**, 1473–1479.
19 R. Bouferra, G. Marín, S. Amhil, S. M. Wasim and L. Essaleh, *Physica B: Condens. Matter.*, 2019, **565**, 14–17.
20 S. K. Patil, M. Y. Koledintseva, R. W. Schwartz and W. Huebner, *J. Appl. Phys.*, 2008, **104**, 074108.
21 W. Wang, M. Wang, E. Ambrosi, A. Bricalli, M. Laudato, Z. Sun, X. Chen and D. Ielmini, *Nat. Commun.*, 2019, **10**, 81.
22 Y. Zhang, N. Deng, H. Wu, Z. Yu, J. Zhang and H. Qian, *Appl. Phys. Lett.*, 2014, **105**, 063508.
23 H. Jiang, D. Belkin, S. E. Savel'ev, S. Lin, Z. Wang, Y. Li, S. Joshi, R. Midya, C. Li, M. Rao, M. Barnell, Q. Wu, J. J. Yang and Q. Xia, *Nat. Commun.*, 2017, **8**, 882.
24 Z. Wang, S. Joshi, S. E. Savel'ev, H. Jiang, R. Midya, P. Lin, M. Hu, N. Ge, J. P. Strachan, Z. Li, Q. Wu, M. Barnell, G.-L. Li, H. L. Xin, R. S. Williams, Q. Xia and J. J. Yang, *Nat. Mater.*, 2017, **16**, 101–108.
25 H. Abbas, Y. Abbas, G. Hassan, A. Sergeevich Sokolov, Y.-R. Jeon, B. Ku, C. Jung Kang and C. Choi, *Nanoscale*, 2020, **12**, 14120–14134.
26 T. Maeda, W. Gong and T. Wada, *Jpn. J. Appl. Phys.*, 2016, **55**, 04ES15.
27 R. T. Tung, *Appl. Phys. Rev.*, 2014, **1**, 011304.