Electronic Supplementary Material (ESI) for Nanoscale Horizons.

Supplementary Information: GaAs Nanowires on Si Nanopillars : Towards Large Scale, Phase-engineered Arrays.

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Atomic Force Microscopy of Spin-coated Pillars

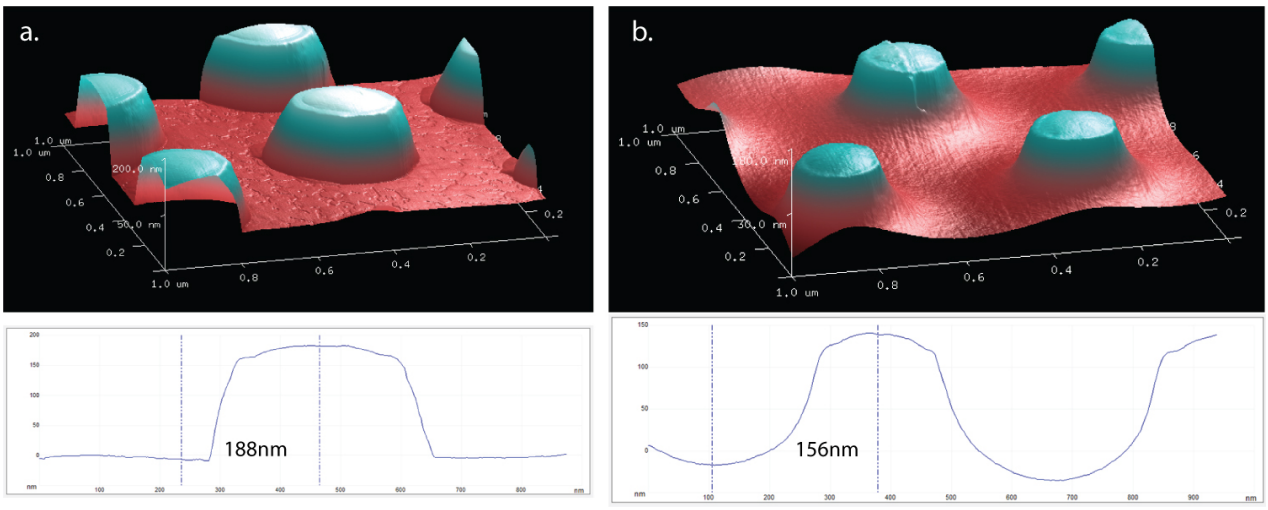

Figure 1: *AFM data of a. bare SiO_2/Si pillars and b. after ZEP spin-coating.*

Figure 1 Shows phase-shift lithography (PSL) SiO_2/Si pillars before (a.) and after (b.) spin-coating of ZEP 20% dilution in Anisole at 2500rpm. This step appears to be important for the correct opening of the SiO_2/Si pillars : In fact, the observed meniscus prevents the exposure of the sidewalls to the reactive ion etching (RIE) plasma, permitting to obtain a flat and directional etching. Nevertheless this was observed to be true only for relatively short etchings (<5min). For long etchings, i.e long enough to etch the ZEP on the side-walls, we found that spin-coating a thick layer of poly methyl methacrylate (thicker than the SiO_2/Si pillars height) and etching down with two RIEs : a first O_2 plasma for the top PMMA and a second CHF_3/Ar plasma for the oxide etching, yields better results.

Knowing the pillars height from subfigure a. and measuring the step height in subfigure b. we can extrapolate the spin-coated ZEP thickness. For those spin-coating parameters the value is close to 30nm.

Characterization of Ga predeposition droplets on 10nm Oxide.

The following SEM images were used, along with the software Dropsnake(tm) to obtain an estimation of the Ga droplet's contact angles. This Ga pre-deposition follows the same Ga flux and substrate temperature than the NW growths performed in the main study, for the sake of comparison. The measurement accuracy is ± 5°.

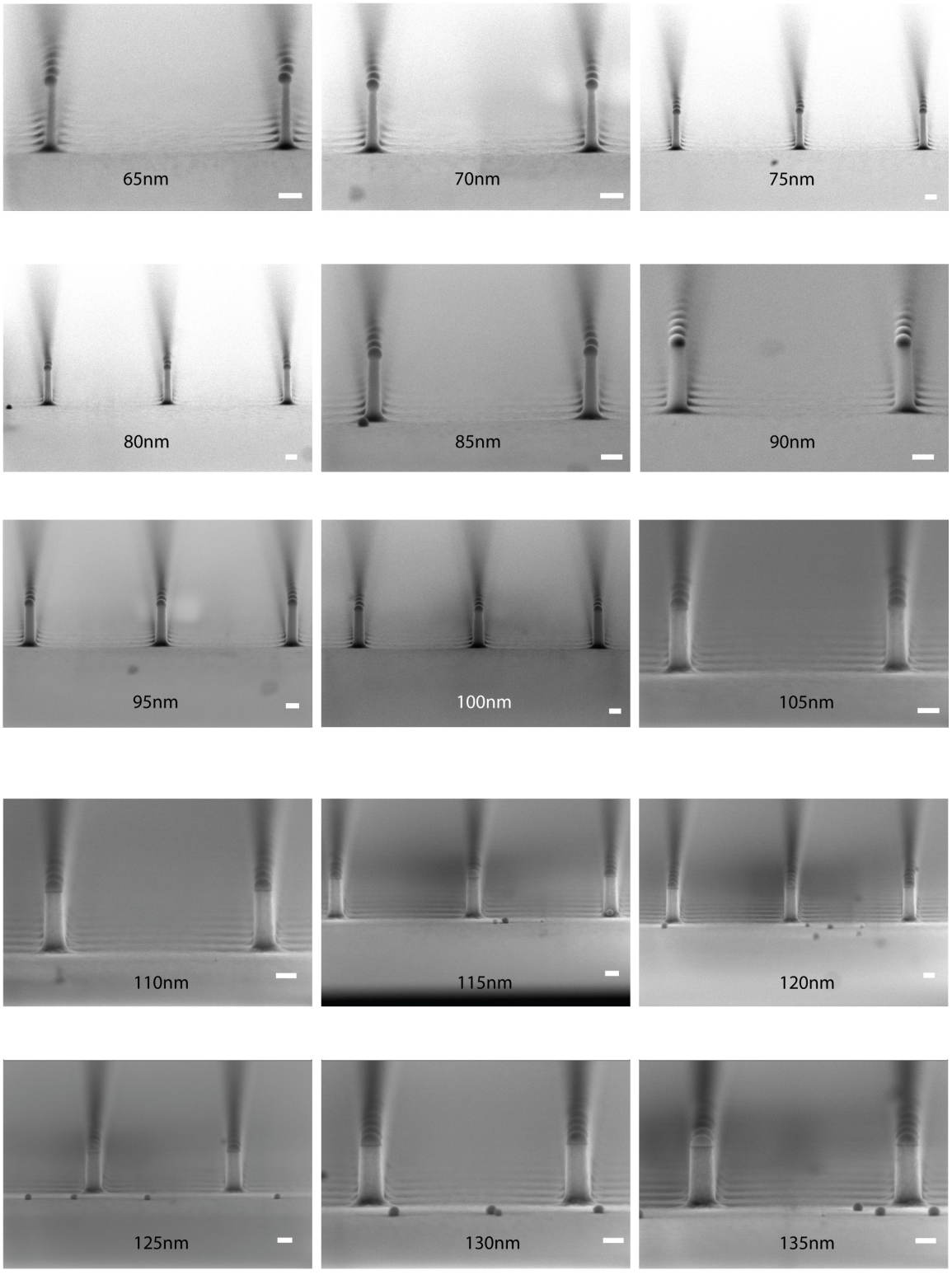

Figure 2: *Exemplary SEM crossection images of the 10nm predeposition sample for Figure 2d of the main study. Scale bar is 100nm.*

DUV Stepper Lithography of SiO_2/Si Pillars

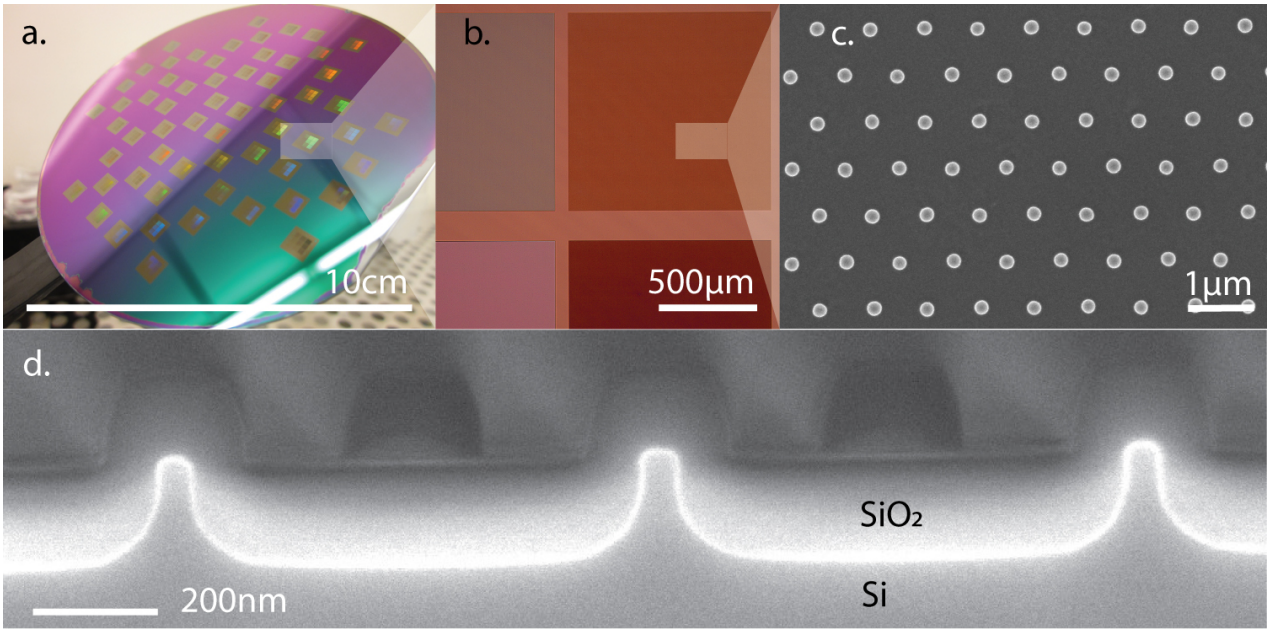

Figure 3: *Overview of the SiO_2/Si pillars fabricated by DUV stepper lithography. a.Photography of the wafer, b.optical microscope image of an array,c. Top view SEM image of a pillar array and d. cross-section of the oxidised SiO_2/Si pillars.*

Figure 3 shows an overview of the SiO_2/Si pillars fabrication using deep-ultraviolet stepper lithography (DUVSL). They are exposed using an ASML^{tm} PAS 5500/350C system and developed using a Süss Microtech^{tm} ACS200 gen3 system. The resin used is M108Y to a thickness of 140nm with a buffered anti-reflective coating (BARC) of 40nm. The dose used is 14.5$\mu C/cm^2$ at a z = -0.2μm focus. Sample is then introduced in an SPTS APS plasma etcher where a plasma of CHF_3/O_2 of 34sec is done for BARC etching. The wafer is then introduced in an Alcatel^{TM} AMS200 DSE RIE, where a customized recipe using SF_6 and C_4F_8 is used for creating the pillars. An oxygen plasma is performed in a Tepla^{tm} Giga-Batch system for stripping the resist/BARC. A buffered hydrofluoric acid (7:1) bath is then used for 2 minutes to remove any trace of resist/BARC. A thermal oxidation is then done at 900°C for a variable amount of time depending on the wanted oxide thickness.

Subfigure a. shows the full 100mm wafer after exposure. Each square represents sev-

eral mm-scale arrays of different diameters and pitches. Subfigure b. is a microscope image showing four different arrays which periodicity changes, altering their colours. Subfigure c. is an SEM image of 190nm Si pillars after RIE. Subfigure d. shows an SEM cross-section of a cleaved SiO_2/Si pillar array. As seen the arrays are highly uniform and suitable for VLS growth of GaAs NWs. Moreover the freedom in design open perspectives for fabricating non-periodic arrays, contrarily to phase-shift lithography (PSL) techniques presented in our main study.

Wurtzite Nanowire Array from SiO_2/Si Pillars

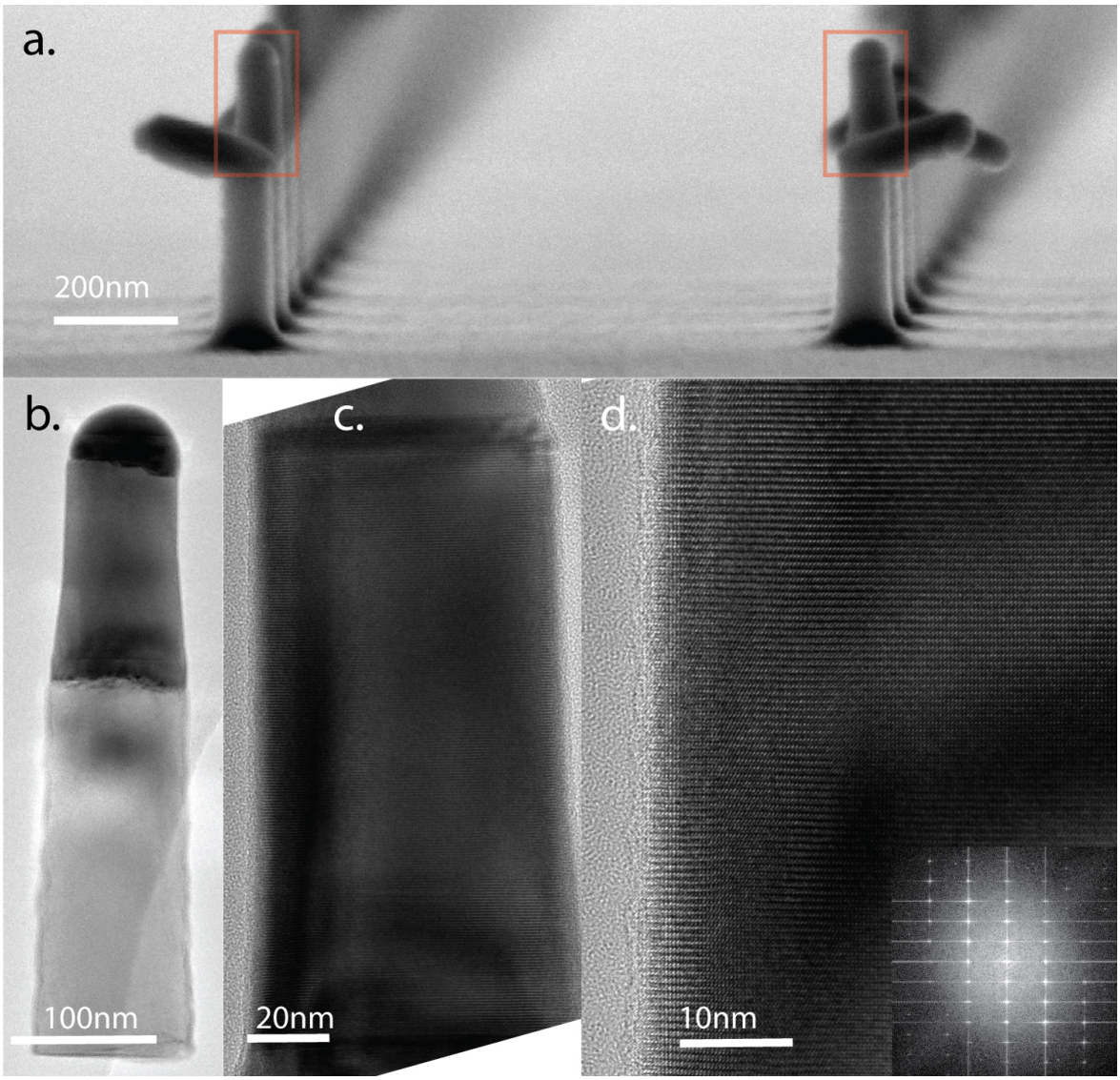

Figure 4: *SEM and TEM images showing self-catalyzed VLS GaAs NW growth on SiO_2/Si 10nm oxidised. a. SEM crossection image shows the 105nm nominal diameter array with tilted and vertical NWs. b. TEM BF image of a GaAs NW along with the SiO_2/Si pillar it grew from. c. and d. HRTEM images of a vertical NW on a SiO_2/Si pillar showing pure defect-free WZ structure. The FFt confirms the WZ phase.*

Figure 4 shows an overview of MBE growth on 10nm nominally-oxidized SiO_2/Si EBL pillars. The NWs shown here are from 105nm nominal diameter pillars array. The growth parameters are analog to growth 1 presented in our main study. Subfigure a. Shows a cross-section view of the 105nm nominal diameter array after GaAs VLS NW growth. We can see

that we have tilted and vertical nanowires. The contact angle appears to be close to the wurtzite (WZ) stable one during growth. Subfigure b. shows a TEM micrograph of a transferred GaAs NW with its base SiO_2/Si pillar. The oxide is hard to see given its very low thickness. subfigure c. and d. show HRTEM images of a vertical NW on Si pillar, showing a defect-free WZ crystal structure. Subfigure d. also shows the image FFT confirming the WN crystal structure.

From SEM characterization, all the vertical NWs were exhibiting morphological characteristics analogue to the ones observed by TEM. This leads us to think that all vertical NW from this growth are WZ, confirming the phase-engineering potential of the SiO_2/Si pillar patterning method.