

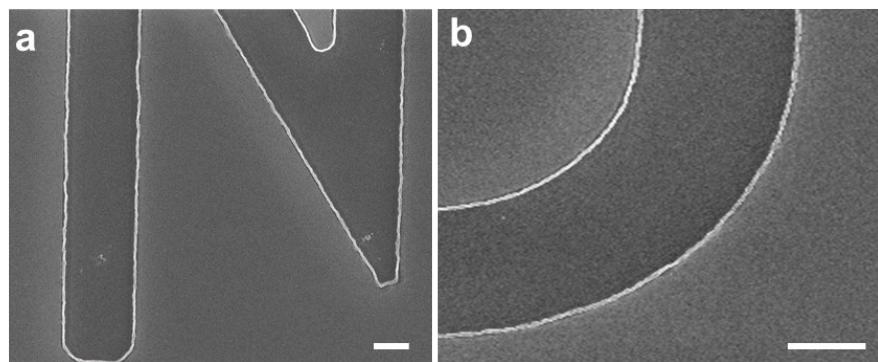
*Supplementary Information to*

**Unexpected phosphorus doping routine of planar silicon  
nanowires for integrating CMOS logics**

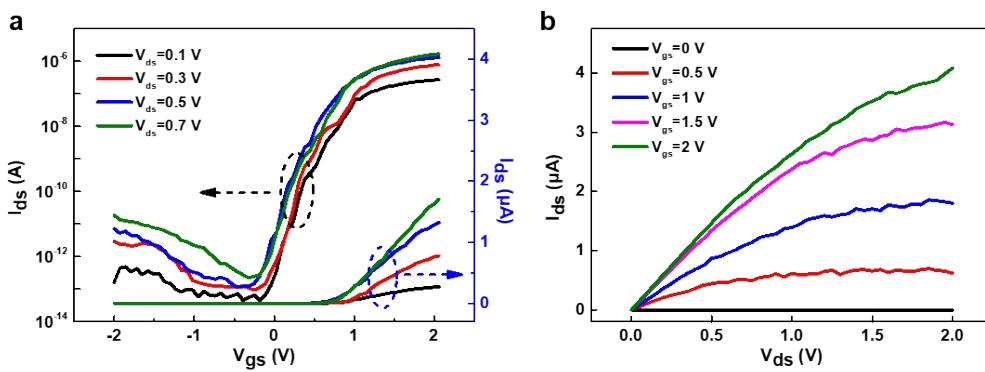
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**Fig. S1.** Close SEM images of the ultralong n-type SiNWs grown along the curved or straight guiding edge lines. Scale bars are both for 2  $\mu\text{m}$ .



**Fig. S2.** Electrical properties of the n-type SiNW FETs. (a) presents the transfer curves under different  $V_{ds}$  biases, while the different output curves are shown in (b).