Electronic Supplementary Material (ESI) for Nanoscale.

Supplementary Information for

Title: Layer-dependent interface reconstruction and strain modulation in twisted WSe_2

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Contents:

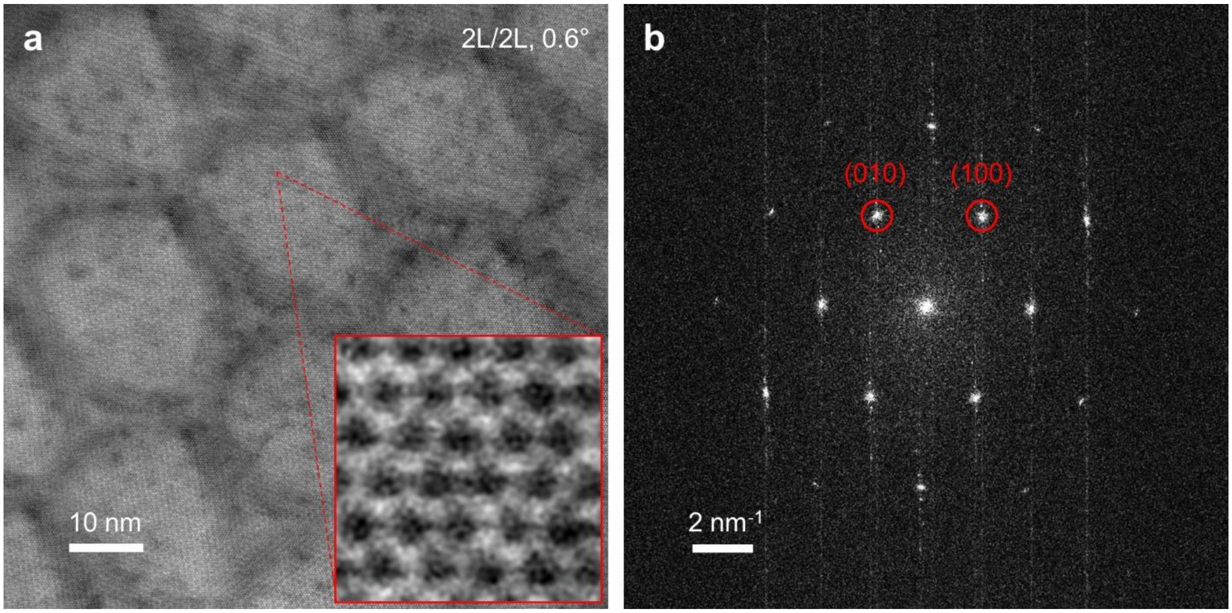

Figure S1: Processing details of geometric phase analysis (GPA). (a) The real-space image of 0.6°-twisted 2L/2L WSe_2 with the inset of an enlarged area to demonstrate the reliable atomic resolution achieved by adequate sampling pixels (4k x 4k x 0.2Å per pixel). **(b)** The corresponding power spectrum (zoomed in for clarity) of **(a)** showing the reflection spots used to extract strain components as marked by red circles. Since the twist angle is small and the interface reconstruction dominates, the Bragg spots from top and bottom WSe_2 cannot be distinguished apart. The reciprocal aperture size was set for a 2-nm real-space resolution and the central region of relaxed domains was chosen as the reference lattice.

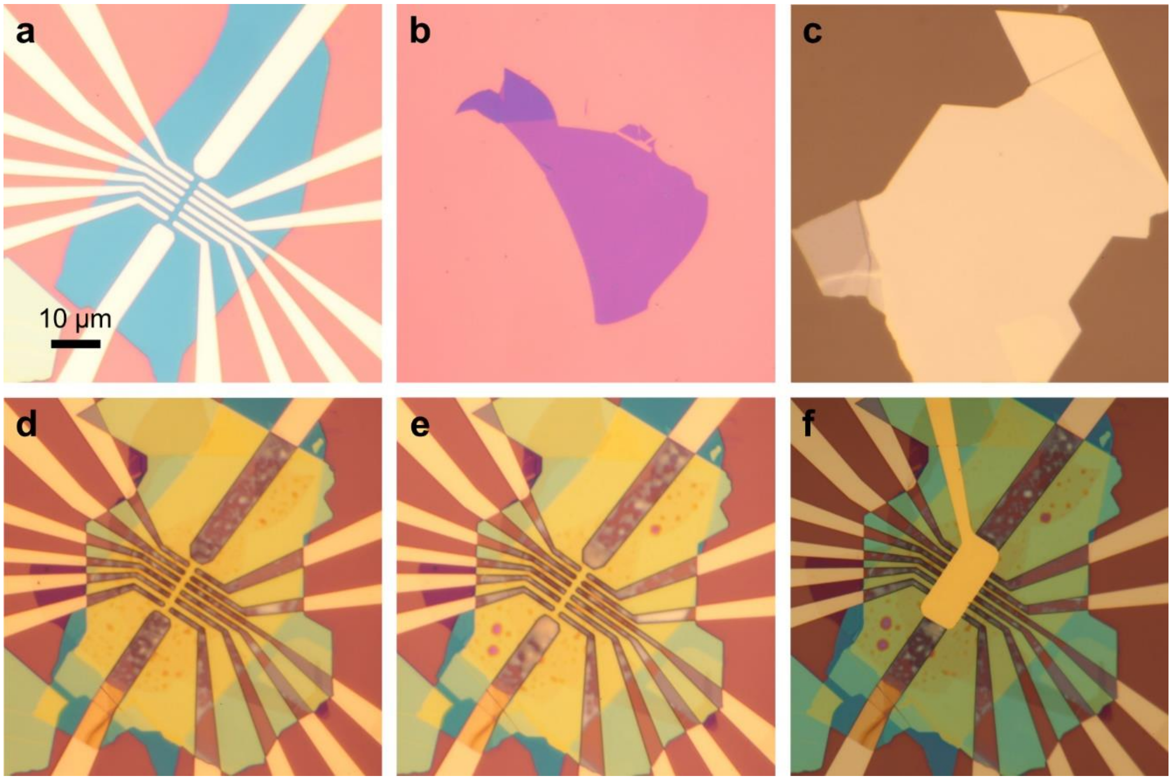

Figure S2: Process flow to fabricate the twisted WSe_2 field-effect transistors (FETs). (a) The 5/20nm Cr/Pt electrodes in a Hall-bar configuration were deposited on a ~20nm BN flake and stored in the glove box for use. **(b)** Single-crystalline WSe_2 bilayers were mechanically exfoliated onto 300nm-SiO_2/Si substrates and identified by the optical contrast. The surface cleanness and thickness of selected flakes were confirmed by the atomic force microscopy (AFM). **(c)** ~40nm BN flakes were mechanically exfoliated onto substrates and picked up using a polycarbonate (PC) coated polydimethylsiloxane (PDMS) stamp. The same 'tear-and-stack' manner as adopted in preparing TEM samples was used to tear up half of the crystal and stack onto the other part after twisting by an angle. **(d)** The twisted-WSe_2/BN heterostructure was then dropped down onto the bottom electrodes in **(a)**. **(e)** The device was annealed at 250°C in the Ar protecting gas flow for 6 hours to improve the contact between electrodes and WSe_2. The stacked van der Waals interfaces were fully relaxed during this process. **(f)** Finally, a top gate was defined by e-beam lithography and deposited as 5/60nm Ti/Au.