Electronic Supplementary Material (ESI) for Nanoscale.

SUPPLEMENTARY INFORMATION

Ferroelectric transistors with asymmetric double gate for memory window exceeding 12 V and disturb-free read

Halid Mulaosmanovic[1*], Dominik Kleimaier[2], Stefan Dünkel[2], Sven Beyer[2], Thomas Mikolajick[1,3] and Stefan Slesazeck[1]

[1] NaMLab gGmbH, 01187 Dresden, Germany
[2] GlobalFoundries, Dresden Module One LLC & Co. KG, 01109 Dresden, Germany
[3]Chair of Nanoelectronics, TU Dresden, 01062 Dresden, Germany

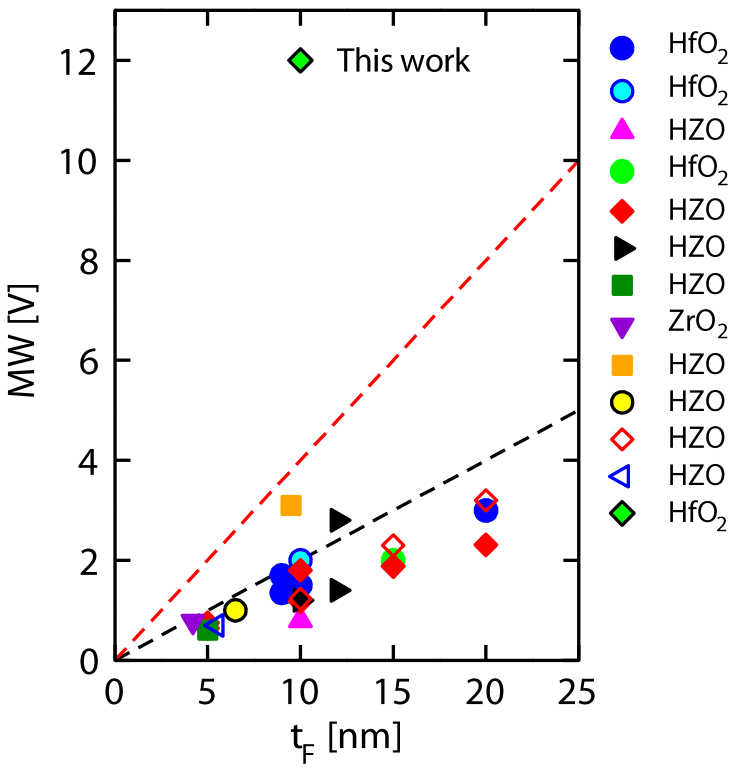

Fig. S1 MW as a function of thickness of the FE layer (t_F). The plot shows the collection of the MW values reported across the literature for MFIS FeFETs and plotted as a function of t_F for different variants of hafnia and zirconia based FE materials. Each color/symbol corresponds to a different device/material type. The dotted lines indicate the maximum theoretical value expected from Eq. (1) for E_C = 1 MV/cm and 2 MV/cm. Adapted from Ref. [1].

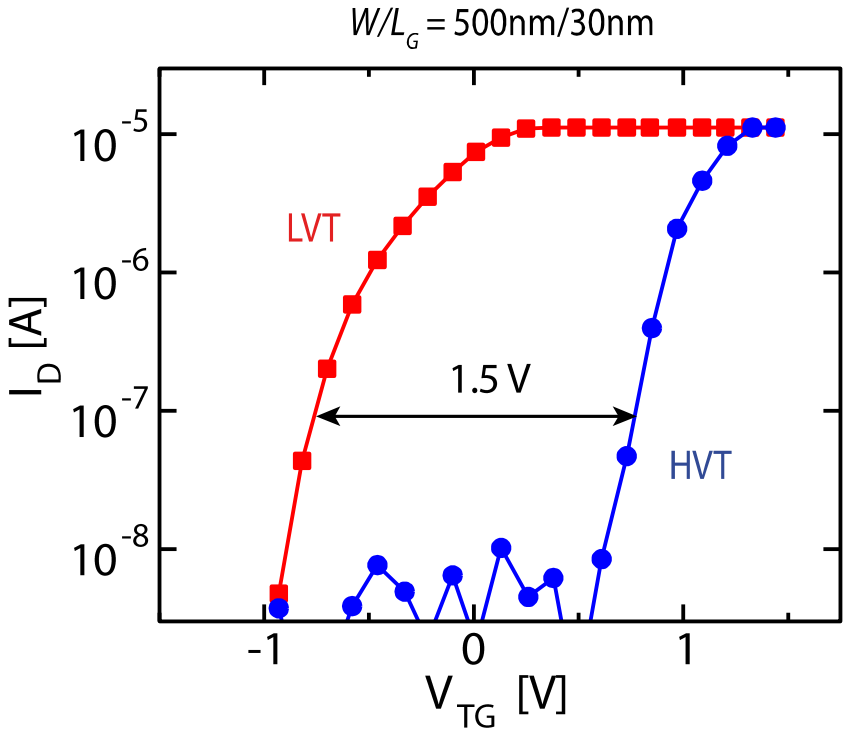

Fig. S2 $I_D - V_{TG}$ curves (top transistor) for LVT and HVT states of a device with $W = 500$ nm and $L_G = 30$ nm with a memory window of around 1.5 V. The corresponding $I_D - V_{BG}$ curves are shown in Fig. 2(g) in the main text.

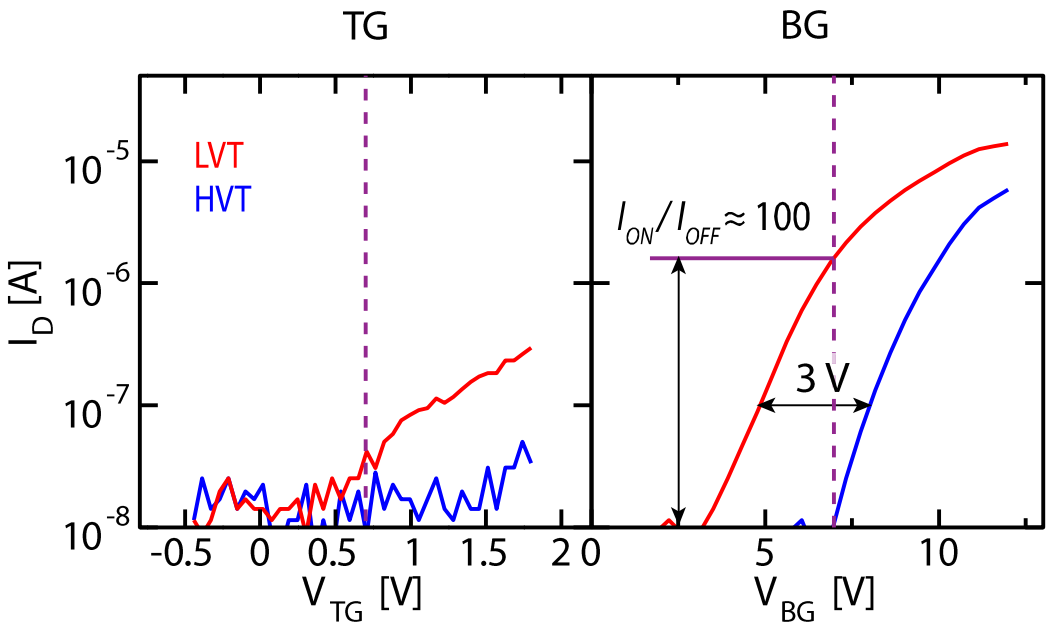

Fig. S3 $I_D - V_{TG}$ (left) and (e) $I_D - V_{BG}$ (right) curves after 10^5 write cycles (taken from Fig. 3(c) in the main text). Vertical dashed lines indicate the V_{TG} and V_{BG} points at which I_{ON} and I_{OFF} in Fig. 3(d) in the main text were sampled to achieve the largest I_{ON}/I_{OFF} prior to degradation.